

A New Multilevel Inverter Topology for DC-AC Conversion

Premananth.P, Chitrapreyanka.S.B

PG Scholar, Department of Electrical and Electronics Engineering, K.S.R. College of Engineering (Autonomous), Tiruchengode, Tamil Nadu, India.

Assistant Professor, Department of Electrical and Electronics Engineering, K.S.R. College of Engineering (Autonomous), Tiruchengode, Tamil Nadu, India.

Abstract - Multilevel inverters have been widely used for high power, high voltage applications. Among the existing multilevel inverter topologies Cascaded inverter topology has many advantages over Neutral point clamped and Flying capacitor inverters, but it requires isolated DC sources which is a main drawback of this topology. This work reports a new topology with a reversing-voltage component and is proposed to improve the multilevel performance by compensating the disadvantages mentioned and the total harmonic distortion is analyzed. The new topology produces a significant reduction in the number of power devices and capacitors required to implement a multilevel output. This topology requires fewer components compared to existing inverters (particularly in higher levels) and requires fewer carrier signals and gate drives. A nine level PWM inverter configuration with DC sources are verified through MATLAB/SIMULINK software. Furthermore, an experimental prototype of a nine level inverter for both cascade and RV inverter has been implemented and total harmonic distortion (THD) is calculated using MATLAB/SIMULINK software. Result have been compared and validated for the same.

I. INTRODUCTION

Multilevel power conversion has been extensively researched in the past few years for high power applications [1], [2]. Many topologies have been introduced for utility and drive applications. The two level inverters require high switching frequency with various PWM strategies to get quality output which leads to high switching losses. To overcome these problems multi level inverters (MLIs) are introduced. It uses higher number of semiconductor switches to perform the power conversion in small voltage steps. The advantages of MLIs are improvement in Staircase waveform quality, reduction in Common-mode (CM) Voltage, less input current distortion [3]. MLI are extensively being used in drives, PV systems, HEV systems, automotive applications [4-8]. The various topologies of MLI are Cascade inverter, Neutral-point clamped (NPC) inverter, and Flying capacitor inverter. As the level increases, NPC require many clamping diodes, control of real power flow becomes difficult [13]. In Flying capacitor inverter as the level increases, number of storage capacitors also increases hence becomes bulky and costly; the switching losses are also more [14]. The cascaded multilevel inverter has more advantages than other two topologies [9], [10], since it does not require any balancing capacitors and diodes. Cascaded inverter needs separate DC sources for each H-Bridge, hence there is no voltage balancing problem, but isolated DC sources are not readily available, this could be main drawback of this topology [15][16]. Cascaded topology requires more switches. These disadvantages are overcome by a new topology known as Reversing Voltage Component [10].

In this method it is not necessary to utilize all the switches for generating bi-polar levels and separates the output voltage into two parts [10][12]. RV requires less number of switches and components, needs only half of the conventional carriers for SPWM controller [12][17], the complexity of control is also minimized when compared with other topologies.

II. CASCADED H-BRIDGE (CHB) AND REVERSE VOLTAGE (RV) MULTILEVEL TOPOLOGIES

A. Cascaded H-Bridge Inverter Topology

The concept of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. The number of output voltage levels are $2n+1$, where n is the number of cells. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. It needs less number of components comparative to the Diode clamped or the flying capacitor [16], so the price and the weight of the inverter is less.

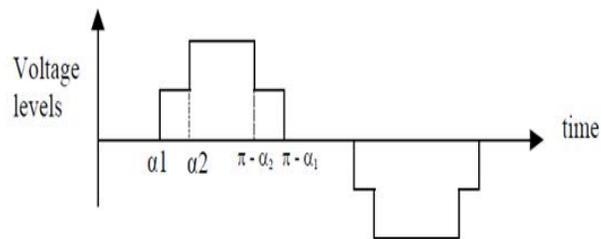


Figure 1 Two level voltage waveform

B. Reverse Voltage Topology.

In conventional multilevel inverters, the power semiconductor switches are combined to produce a high frequency waveform in positive and negative polarities. However, there is no need to utilize all the switches for generating bipolar levels. This idea has been put into practice by the new topology. This topology is a hybrid multilevel topology which separates the output voltage into two parts. One part is named level generation part and is responsible for level generating in positive polarity. This part requires high frequency switches to generate the required levels. The switches in this part should have high-switching-frequency capability. The other part is called polarity generation part and is responsible for generating the polarity of the output voltage, which is the low-frequency part operating at line frequency.

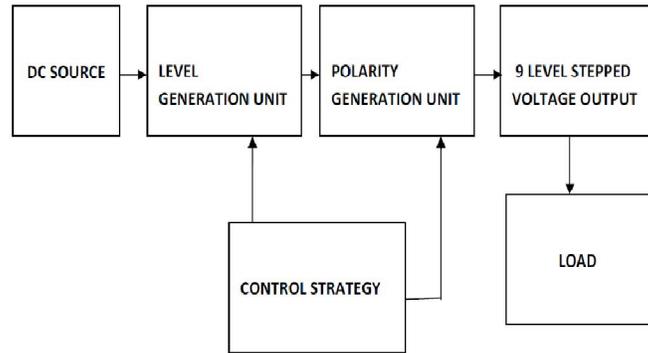


Figure 2 General block diagram of 1Φ RV inverter

This topology easily extends to higher voltage levels by duplicating the middle stage as shown in Fig.3. Therefore; this topology is modular and can be easily increased to higher voltage levels by adding the middle stage in Fig.3. This requires fewer components in comparison to conventional inverters. It just requires half of the conventional carriers for SPWM controller. SPWM for seven-level conventional converters consists of six carriers, but here, three carriers are sufficient. The reason is that, according to Fig.3, the multilevel converter works only in positive polarity and does not generate negative polarities. In comparison with a cascade topology, it requires just one-third of isolated power supplies used in a cascade-type inverter.

c. Total Harmonic Distortion

The power quality of distribution systems has a drastic effect on power regulation and Consumption. Power sources act as non-linear loads, drawing a distorted waveform that contains harmonics. These harmonics can cause problems ranging from telephone transmission Interference to degradation of conductors and insulating material in motors and Transformers. Therefore it is important to gauge the total effect of these harmonics. The summation of all harmonics in a system is known as total harmonic distortion (THD).

Total harmonic distortion, or THD, is the summation of all harmonic components of the voltage or current waveform compared against the fundamental component of the voltage or current wave

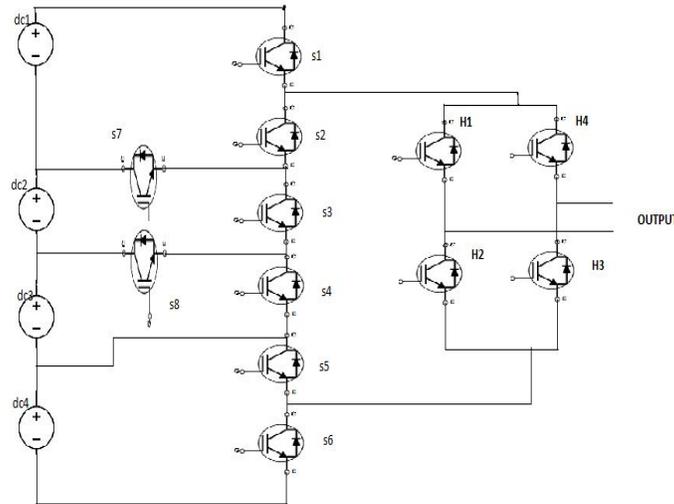


Figure 3 Schematic diagram of 1Φ 9 level RV inverter

D. Modes of Operation

Switching sequences in this converter are easier than its counter parts. According to its inherent advantages, it does not need to generate negative pulses for negative cycle control. Thus, there is no need for extra conditions for controlling the negative voltage. Instead, the reversing full-bridge converter performs this task, and the required level is produced by the high-switching-frequency component of the inverter. Then, this level is translated to negative or positive according to output voltage requirements.

As seen from Table I, there are six possible switching patterns to control the inverter. In order to avoid unwanted voltage levels during switching cycles, the switching modes should be selected so that the switching transitions become minimal during each mode transfer, hence it will reduce switching power dissipation. The sequence of switches (2-3-4-5), (2-3-4-6), (2-3-8-6), (2-7-6), and (1-6) are chosen for levels 0 up to 4, respectively. The output voltage level is the sum of voltage sources, which are included in the current path that is shown in the following fig. 4

TABLE I
SWITCHING MODES FOR GENERATING 9 LEVEL RV INVERTER

Level \ Mode	0	1	2	3	4
1	2,3,4,5	2,3,4,6	2,7,5	2,7,6	1,6
2		2,7,8,4,5	2,3,8,6		

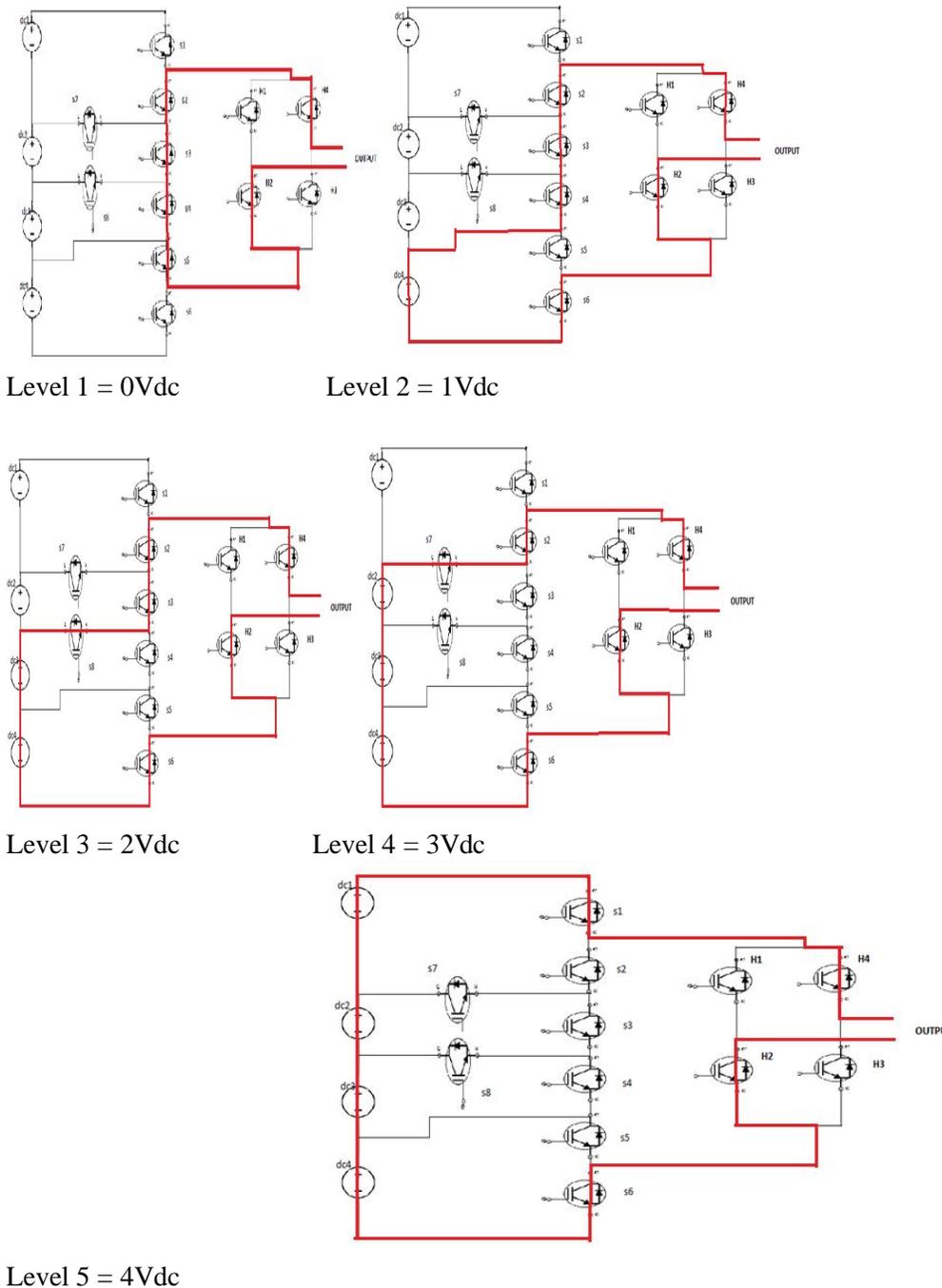


Figure 4 Switching levels of 1Φ nine level inverter

E. Number Of Components

The reliability of a system is indirectly proportional to the number of its components. As the number of high-frequency switches is increased, the reliability of the converter is decreased. From Table I it is cleared that RV requires very less number of switches than other topologies.

TABLE II

NUMBER OF COMPONENTS FOR THREE PHASE INVERTER

Inverter Type	NPC	Flying capacitor	Cascade	Proposed
Main switches	$6(N-1)$	$6(N-1)$	$6(N-1)$	$3((N-1)+4)$
Main diodes	$6(N-1)$	$6(N-1)$	$6(N-1)$	$3((N-1)+4)$
Clamping diodes	$3(N-1)(N-2)$	0	0	0
DC bus capacitors/isolated supplies	$(N-1)$	$(N-1)$	$3(N-1)/2$	$(N-1)/2$
Flying capacitors	0	$3/2(N-1)(N-2)$	0	0
Total numbers	$(N-1)(3N+7)$	$1/2(N-1)(3N+20)$	$27/2(N-1)$	$(13N+35)/2$

The N in the comparison table indicates the number of levels. As shown in the table, the number of components for proposed topology is less compared to other topologies.

The clamping diodes are used in NPC topology only. The remaining topologies do not use clamping diodes. The flying capacitor is also used only in flying capacitor topology only.

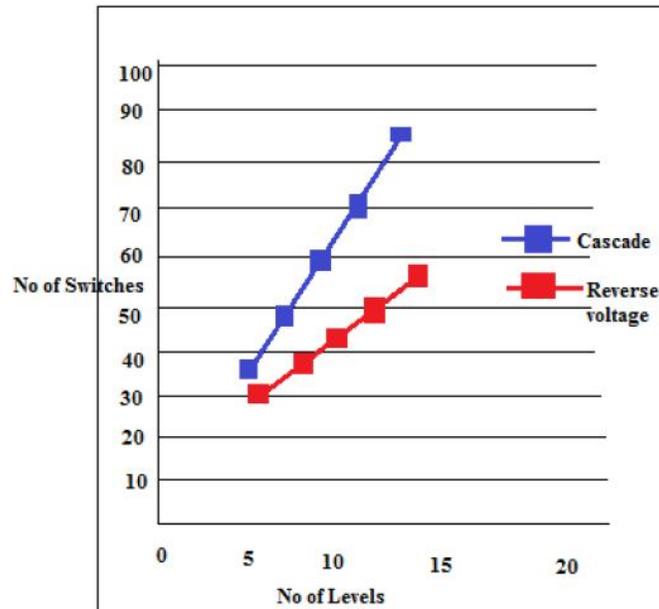


Figure 5 Number of switches required for three phase Inverter.

II CONTROL STRATEGIES

A. Fundamental Frequency

PWM method and SVM technique will cause extra losses due to high switching frequencies. For this reason, low-switching frequency control methods, such as selective harmonic elimination method, fundamental frequency switching method or active harmonic elimination method, can be used for the MLI control.

B. Sinusoidal Pulse Width Modulation

It is desired that the ac output voltage $V_O = V_{an}$ follow a given waveform (e.g., sinusoidal) on a continuous basis by properly switching the power valves. The carrier based PWM technique fulfils such a requirement as it defines the on and off states of the switches of one leg of a VSI by comparing a modulating signal V_A (desired ac output voltage) and a triangular waveform V_C (carrier signal). In practice, when $V_A > V_C$ the switch S_+ is on and the switch S_- is off; similarly, when $V_A < V_C$ the switch S_+ is off and the switch S_- is on.

A special case is when the modulating signal V_A is a sinusoidal at frequency F_C and amplitude V^A and the triangular signal V_C is at frequency F_C and amplitude V^C . This is the sinusoidal PWM (SPWM) scheme. In this case, the modulation index m_a (also known as the amplitude-modulation ratio) is defined as $m_a = V_C/V_A$ and the normalized carrier frequency m_f (also known as the frequency-modulation ratio) is $m_f = F_C/F_A$.

The simulated output of the proposed inverter circuit. Contains both current and voltage waveform. The Total Harmonic Distortion (THD) of both output voltage and output current is calculated using powergui FFT analysis. The harmonic distortion of cascade circuit and existing seven level circuits is compared with proposed

inverter circuit. The comparison result of both circuits is displayed in Table III and the FFT analysis of the simulated output is displayed in figure 6 and 7.

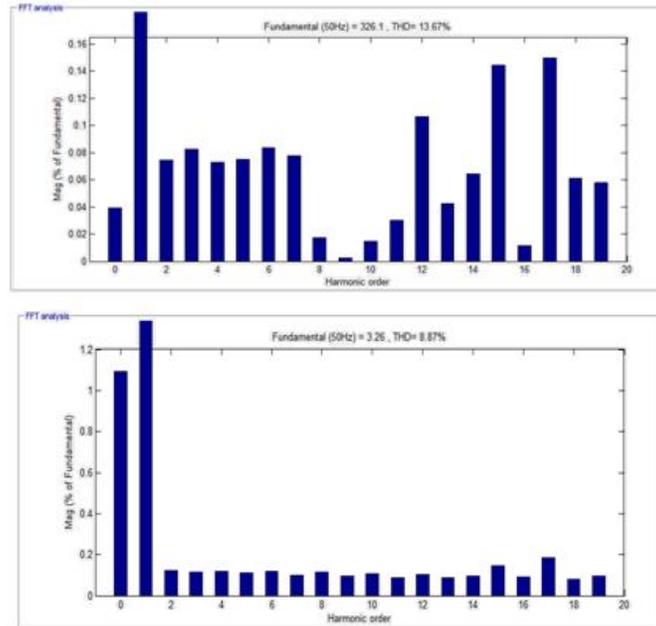


Figure 6 FFT Analysis of output voltage Figure 7 FFT analysis of output current

TABLE III

COMPARISON OF THD VALUES

Topology	%THD(o/p voltage)	%THD(o/p current)
Cascade	21.46%	-
Proposed(nine level)	13.67 %	8.87 %
Proposed(seven level)	21.27%	16.57%

Among these topologies, it has been found that, proposed topology is better than all those structures in terms of THD and provides better spectral quality and reduced THD.

III RESULTS AND DISCUSSION

From the table III it is shown that the proposed inverter topology has less THD compared to existing cascade inverter topology. So the proposed topology can produce better result compared to cascade topology.

IV CONCLUSION

The proposed multilevel inverter implementation was tested using MATLAB/SIMULINK. From the simulation results it is observed that the quality of the output waveform increases with increase in output level. Further the THD of the simulated output is calculated using power gui FFT analysis tool. The THD of the proposed output is compared with cascade topology. From the results it is observed that the THD of the proposed topology is less compared to the cascade topology. So the proposed topology produce better results when compared with available topologies. Therefore the percentage of EMI is drastically reduced.

REFERENCES

- [1] J.S. Lai and F.Z. Peng, "Multilevel Converters - A New Breed of Power Converters," IEEEIAS' 95 Conference Proceedings, pp. 2348-2356, 1995.
- [2] B.S. Suh, G. Sinha, M.D. Manjrekar, T.A. Lipo, "Multilevel Power Conversion – An Overview of Topologies and Modulation Strategies", OPTIM'98 Conference Proceedings, pp. AD-11-AD-24, 1998.
- [3] "Eliminating Harmonics in a Cascaded H-Bridges Multilevel Inverter Using Resultant Theory, Symmetric Polynomials, and Power Sums", Keith Jeremy McKenzie, Thesis for Master of Science, The University of Tennessee, Knoxville, May 2004.
- [4] Chun.T.W.; Q.V.Tran; H.H. Lee; H.G.Kim; E.C. Nho; "A simple capacitor voltage balancing scheme For the cascaded five-level inverter fed ac Machine drive", IEEE Transaction, 2010.
- [5] Tolbert.M.; Peng.Z.;Habetler.G.; "Multilevel Converters for Large Electric Drives", IEEE Transaction ,Industry Applications, Vol:35, issue no.1, Jan 1999.
- [6] José Rodríguez, , Steffen Bernet, BinWu, Jorge O. Pontt, Samir Kouro," Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives ", IEEE Transactions On Industrial Electronics, Vol. 54, No. 6, December 2007.
- [7] E. Ozdemir1, S. Ozdemir1, L. M. Tolbert2,3, B. Ozpineci3 ,"Fundamental Frequency Modulated Multilevel Inverter for Three-Phase Stand-Alone Photovoltaic Application", IEEE Trans, 2009.
- [8] Tolbert.M.; Peng.Z.; "Multilevel Converters for Electric Vehicle Applications", IEEE Trans, 2006.
- [9] P. K. Chaturvedi, Shailendra K Jain, PramodAgrawal Member IEEE, and P. K. Modi "Investigations on Different Multilevel Inverter Control Techniques by Simulation".
- [10] Andreas Nordvall "Multilevel Inverter Topology Survey" Master of Science Thesis in Electric Power Engineering Department of Energy and Environment Division of Electric Power Engineering Chalmers University Of Technology Göteborg, Sweden, 2011.
- [11] P. Barbosa, P. Steimer, J. Steinke, L. Meysenc, M. Winkelnkemper, and N. Celanovic, "Active neutral-point-clamped multilevel converters," in Proc. IEEE 36th Power Electron Spec.Conf., 2005, pp. 2296–2301.
- [12] EhsanNajafi, and Abdul Halim Mohamed Yatim, Senior Member, IEEE "Design and Implementation of a New Multilevel Inverter Topology" IEEE Trans .Indl. Electron, vol. 59, no. 11, Nov2012.
- [13] S. Srikanthan, Mahesh Kumar Mishra, "DC Capacitor Voltage Equalization in Neutral Clamped Inverters for DSTATCOM Application", IEEE Trans, Industrial Electronics, Vol. 57, No. 8, August 2010.
- [14] AnshumanShukla, ArindamGhosh, AvinashJoshi,"Improved Multilevel Hysteresis Current Regulation and Capacitor Voltage Balancing Schemes for Flying Capacitor Multilevel Inverter" IEEE Trans, Power Electronics, Vol. 23, No. 2, March 2008.
- [15] Robert Stala, "Application of Balancing Circuit for DC-Link Voltages Balance in a Single-Phase Diode-Clamped Inverter With Two Three-Level Legs", IEEE Trans, Industrial Electronics, Vol. 58, No. 9, September 2011 4185
- [16] MohammadrzaDerakhshanfar " Analysis off different topologies of multi level inverters" Master of science thesis. Chalmers University of technology, Goteborg, Sweden, 2010.
- [17] 1Hemant Joshi, 2P. N. Tekwani, 3Amar Hinduja "Implementation Of A Five-Level Inverter Using Reversing Voltage Topology: A Competitive Solution For High-Power IM Drive.
- [18] Babar R. (2010) "Optimal topologies for cascaded sub-multilevel converters," Power Electron, Vol. 10, No. 3, pp. 251–261.
- [19] Beser, E., Arifoglu, B., Camur, S., and Beser, E., "Design and application of a single phase multilevel inverter suitable for using as a voltage harmonic source," Power Electron., Vol. 10, No. 2, pp. 138–145.
- [20] Cecati, C., Ciancetta, F. and Siano, P. (2010) "A multilevel inverter for photovoltaic systems with fuzzy logic control," IEEE Transaction, Vol. 57, No. 12, pp. 4115–4125.
- [21] Lezana, P and Rodriguez, J. (2007) "Mixed multicell cascaded multilevel inverter," IEEE ISIE, pp. 509–514.