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# Designing of MIPS R2000 Processor on spartan3E

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**ABSTRACT**: In this paper, we analyze the Processor designed in this project was based on the MIPS R2000. The Objective of the design is to run all Instructions in One cycle. It uses the separate Harvard architecture, it increase the speed of processor. Previews RISK MIPS pipeline design consists 3stage pipeline design, but MIPS R2000 consists 5stage design. MIPS R2000 modules are implemented by pipeline and simulated successfully on Xilinx ise.

**Keywords**: XILINX ise, R2000, 5stage pipeline architecture, risk.

## I. INTRODUCTION

One of the primary goals of computer architects is to design computers that are more cost-effective than their processors. Cost-effectiveness includes the cost of hardware to manufacture the machine, the cost of programming, and costs incurred related to the architecture in debugging both the initial hardware and subsequent programs. If we review the history of computer families we find that the most common architectural change is the trend toward ever more complex machines. Presumably this additional complexity has a positive trade-off with regard to the cost-effectiveness of newer models. This paper will argue that the next generation of VLSI computers may be more effectively implemented as RISC's than CISC's. Early in the project a study on the existing RISC implementations was conducted. It was found that all RISC implementations are based on the same “commandments”.

## II. IMPLEMENTATION OF MIPS R2000

The Processor designed in this project was based on the MIPS R2000.The Objective of the design is to run all Instructions in One cycle. Most of the MIPS instructions are supported except multiply, division and floating point instructions. This design is based on Harvard architecture which uses separate memory unit for both instructions and data. The Harvard architecture will increase the speed of the processor. The design has 5-stage pipelining. All instructions are single cycle executable. It has 32-bit general-purpose registers. In the below figure R2000 includes the major blocks like CPU, Memory, Floating point unit (FPU) and coprocessor (traps and memory).The main component of the arithmetic unit is ALU which performs arithmetic operations like add, subtraction, logical operations like and/or. Multiplication and division operations are not considered for architecture simplicity. The floating point unit is the co processor to the CPU, which perform the floating-point operations. It contains special purpose registers like cause, EPC (exception program counter), status and bad virtual address. This RISC system satisfies the following properties are Single-cycle execution of all (over 80 percent) instructions, single-word standard length of all instructions, small number of instructions, not to exceed about 128, Small number of instruction formats, not to exceed about 4, small number of addressing modes, not to exceed about 4, memory accesses by load and store instructions only and all operations, except load and store, are register-to-register, within the CPU.

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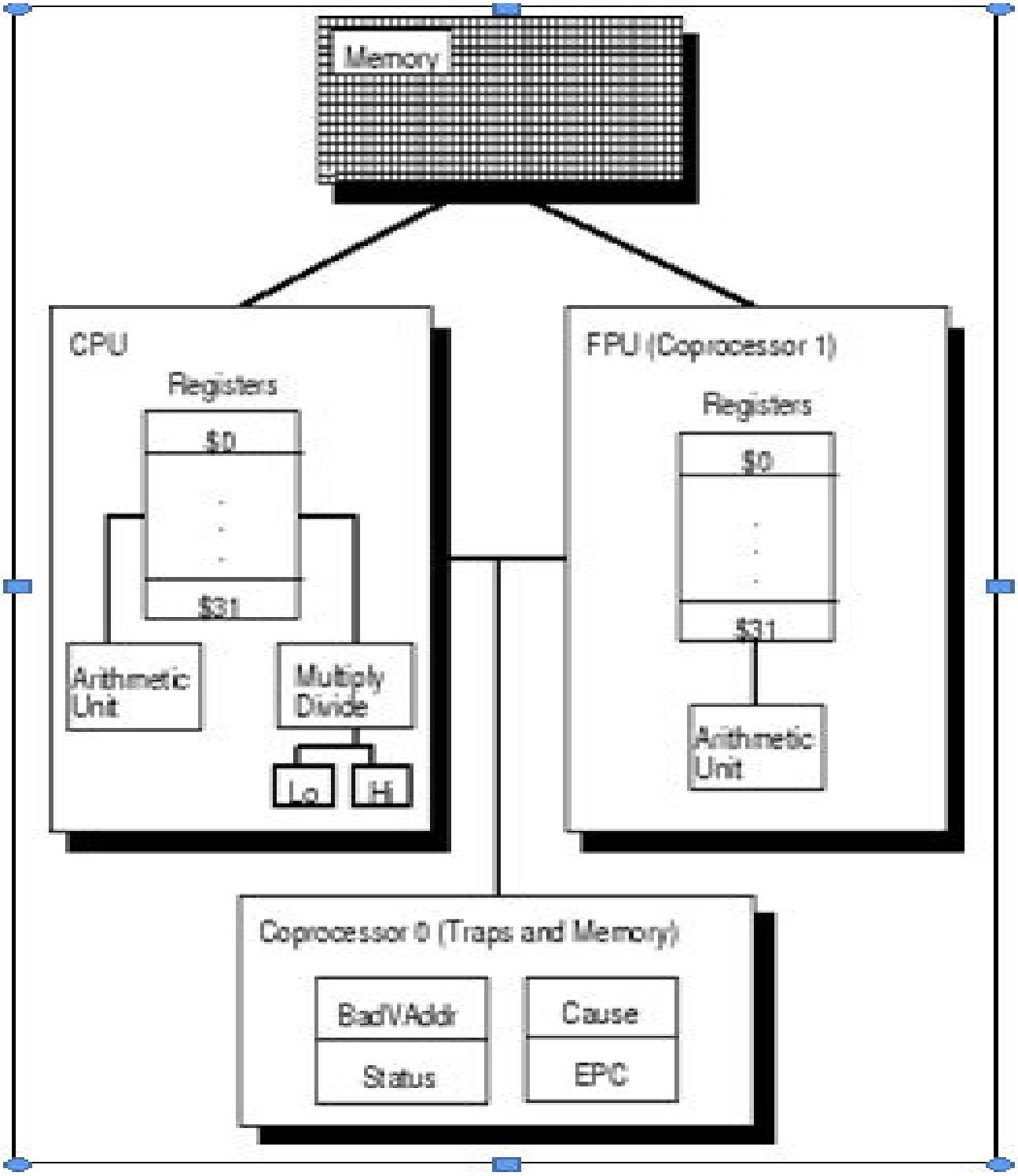


Fig.1. Block Diagram of MIPS R2000

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III. RESULTS

Implementation is done using XILINX 11.1. RTL schematic shown in Fig.3 and Simulation snap is shown in Fig.2.

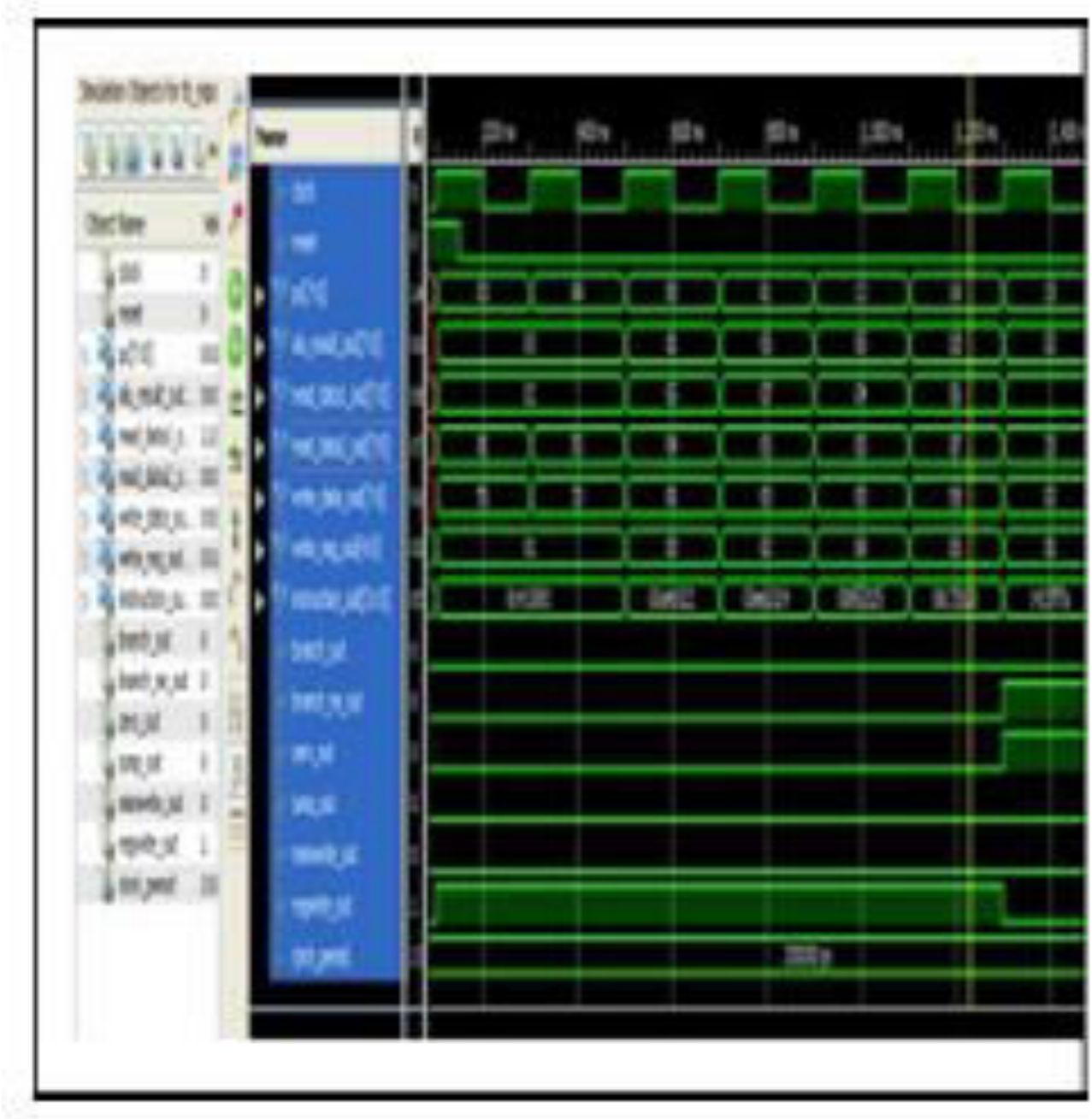

Fig.2. Functional simulation

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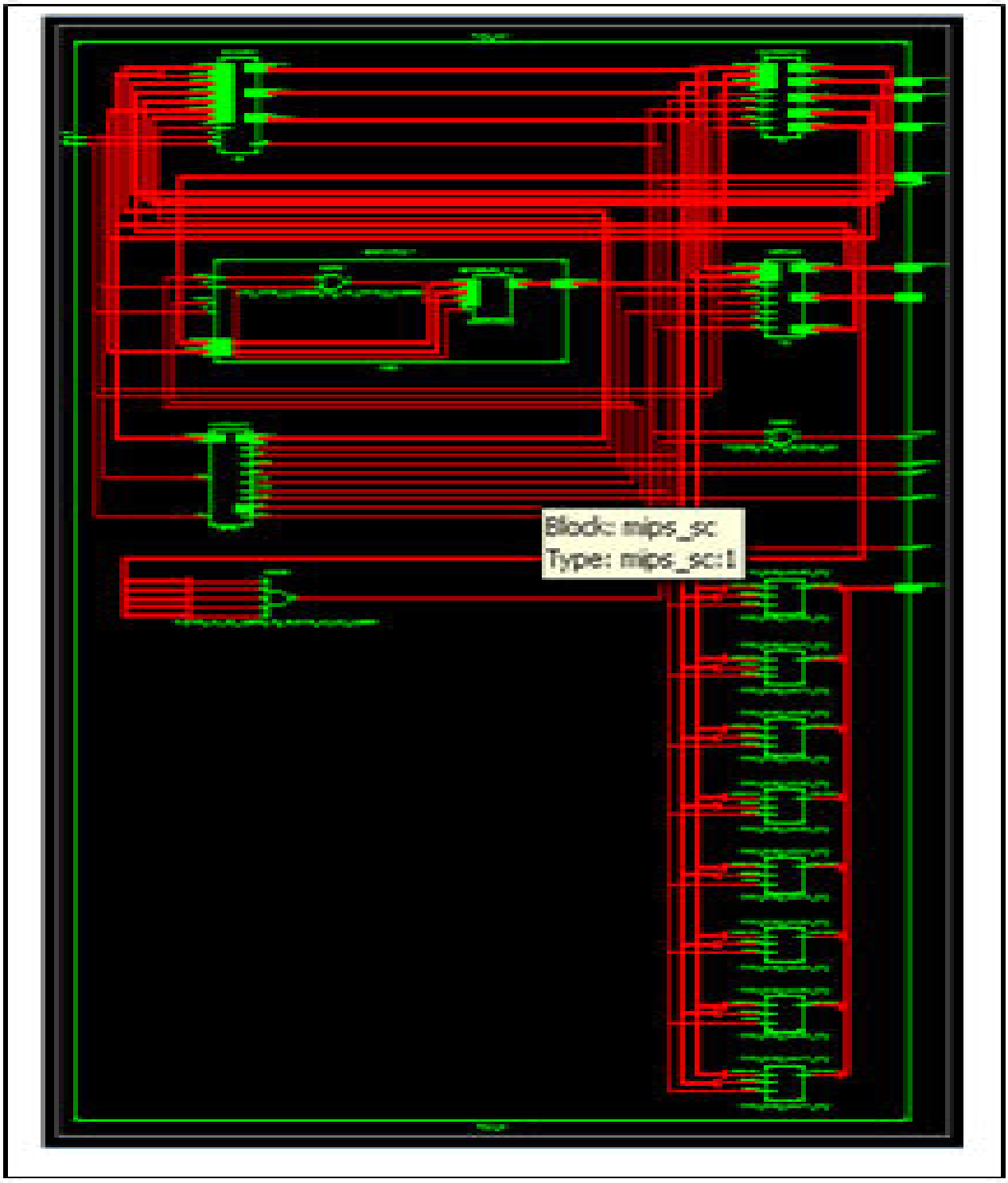


Fig.3. RTL Schematic

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## IV. CONCLUSION

In this paper, MIPS R2000 architecture is design using HDL language, this Harvard architecture is very faster than the other architectures. It is verified by using of XILINX ISE tool, all the simulations, RTL schematics are shown on part.3.

## REFERENCCES

[1] Zheng-WeiMin, Tang-ZhiZhong. Computer System Structure (The second edition), Tsinghua University Press, 2006.

[2] A VHDL Primer 3rd edition by J. Bhasker.

[3] MIPS Technologies, Inc. MIPS32™ Architecture For Programmers Volume II: The MIPS32™ Instruction Set June 9, 2003.

[4] Pan-Song, Huang-JiYe, SOPC Technology Utility Tutorial, Tsinghua University Press, 2006.

[5] MIPS32 4KTMProcessor Core Family Software User's Manual, MIPS Technologies Inc. [M]. BeiJing, Engine Industry Press. 2003.

[6] Yi-Kui, Ding-YueHua, Application of AMCCS5933 Controller in PCI BUS, DCABES2007, 2007.7.759

[7] Rapid Prototyping of digital Systems, a tutorial approach —By – James O. Hamblen and Michael D.Furman.

[8] [8] www.carlstedt.se/hyldo/datorarkitektur/tidigare

[9] [9] www.cs.berkely.edu/

## BIOGRAPHY

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