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Dual Dynamic Node Flip-Flop Design with an Embedded Logic Design

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ABSTRACT: In this paper, we present another dual dynamic node hybrid flip-flop (DDFF) and a novel embedded logic module (DDFF-ELM) focused around DDFF. The proposed designs dispense with the extensive capacitance display in the precharge node of a several state-of-the-art-designs by split dynamic node structure to independently drive the output pull up and pull down transistors. The aim of the DDFF-ELM is to decrease pipeline overhead. It shows an area, power, and speed effective system to join complex logic functions into the flip-flop. The execution examinations made in a 90 nm technology when contrasted with the Semi dynamic flip-flop, with no degradation in speed execution. The leakage power and process voltage-temperature variations of different designs are contemplated in subtle element and are contrasted with the proposed designs.

KEYWORDS: Embedded logic, Latches, Flip-Flops, Low-Power, Split-Dynamic, and Leakage-Power.

I. INTRODUCTION

The enormous advancements in VLSI technologies in the past few years have fuelled the requirement for complicated tradeoffs among, speed power dissipation and area. With gigahertz range microchips getting to be regular place along with the perennial additions in power dissipation, the emphasis is considerably all the more on pushing the speeds to their great while minimizing power dissipation and die on area. The tremendous advancements in VLSI innovations in the recent years have fuelled the requirement for perplexing tradeoffs among speed, power dissipation and area. With gigahertz range microchips getting to be normal place alongside the perennial additions in power dissipation, the attention is considerably all the more on pushing the speeds to their extreme while minimizing power dissipation and die area. The advancements has made speed area unit consistently making forward, from low scale integration to enormous and VLSI and from (MHz) to speed (GHz). The system necessities are ascending with this persistent technique for technology and speed of operation. In synchronous systems, fast has been accomplished speed achieved exploitation advanced pipelining procedures. In stylish deep pipelined architectures, pushing the speed additional demands a lower pipeline overhead. This overhead is that the latency related to the pipeline components, in the same way as the flip-flops and latches. Escalated work has been devoted to enhance the execution of the flip-flops inside the recent decades. Latches and flip-flops are the essential components for putting away data. One latch or flip-flop can store one bit of data. The primary contrast in the middle of latches and flip-flops is that for latches, their outputs are continually influenced by their inputs as long as the enable signal is declared. As such, when they are enabled, their content changes quickly when their inputs change. Flip-flops, then again, have their content change just either at the rising or falling edge of the enable signal. This enable signal is normally the controlling clock signal. After the rising then again falling edge of the clock, the flip-flop content stays steady regardless of the fact that the data changes. There are essentially four principle sorts of latches and flip-flops: SR, D, JK, and T. the real contrasts in these flip-flop sorts are the number of inputs they have and how they change state. For each one sort, there are additionally distinctive variations that upgrade their operations .to have the output change just at the rising or falling edge of the enable signal. This enable signal is generally the controlling clock signal. In this manner, we can have all progressions synchronized to the rising or falling edge of the clock. There have been numerous systems proposed to kill the disadvantage of power consumption and latency. The system requirements prerequisites are likewise ascending with this nonstop propelling technology and speed of operation. Very large extensive work has been dedicated to enhance the execution of the flip-flops in the recent decades. Hybrid latch flip-flop (HLFF) and semi dynamic flip-flop (SDFF) are considered as the exemplary classic high-performance flip-flops. Flip-flop architecture named cross charge control flip flop (XCFF),

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which has extensive favourable circumstances over SDFF and HLFF in both power, area and speed. It utilizes a split-dynamic progressive node to lessen the pre-charge capacitance, which is a standout amongst the most imperative explanations behind the large power utilization in the vast majority of the conventional designs. Repetitive power scattering that comes about when the information does not switch for more than one clock (CLK) cycles. It has expansive hold-time necessity makes the configuration of timing-discriminating systems with XCFF. At long last, regardless of having a single data-driven transistor, embedding logic to XCFF is not extremely effective because of the powerlessness to charge imparting at the inward dynamic nodes. In this paper, we propose another double dynamic node hybrid flip-flop (DDFF) and a novel installed embedded logic module (DDFFELM). Both of them dispense with the downsides of XCFF.

II.STATIC FLIP FLOP

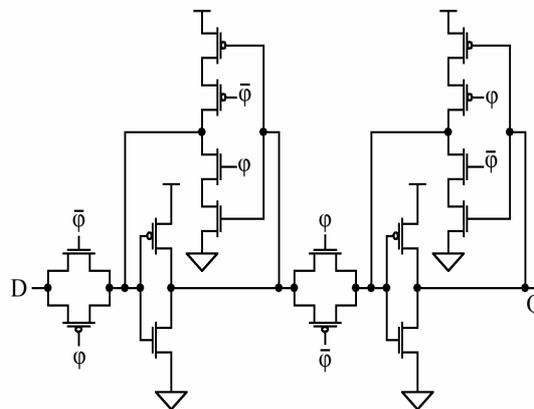


FIGURE-1

Keeping in mind the end goal to beat the issue of circulating a few clock signals and dodge the genuine issues brought about by clock skew, an advancement of NORA-CMOS method presented True Single Phase clock (TSPC) CMOS circuit system TSPC flip-flops have the focal point of single clock dissemination, little territory for clock lines, high speed and no clock skew. The essential TSPC latches could be gotten from numerous points of view to actualize all essential sequential components. It indicate usage of eight-transistor positive edge-triggered D flip-flop utilizing split output TSPC latches Although this structure appears to have more modest territory than 9t TSPC flip-flop and less clocked transistors, it hasn't been utilized for simulations. The primary reason is that there are a few nodes in this structure which are not completely driven to VDD or GND.

III.DYNAMIC FLIPFLOP

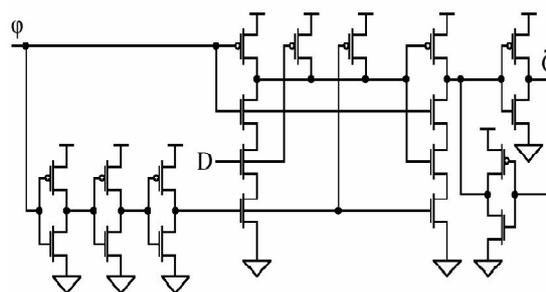


FIGURE-2

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This structure is essentially a level sensitive latch which is clocked with an inside produced sharp pulse. This sharp pulse is created at the positive edge of the clock utilizing clock and postponed form of clock. Transistor level execution of this flip-flop is demonstrated in figure.

IV.XCFF

Cross charge control flip flop XCFF

The vast precharge-capacitance in a wide variety of designs results from the way that both the output pull-up and the pull-down transistor are driven by this precharge node. These transistors being driving vast output loads help the majority of the capacitance at this node. This normal disadvantage of conventional designs was considered in the outline of XCFF. It diminishes the power dissipation by splitting the dynamic node into two, every one independently driving the output pull-up and pull-down transistors. Since stand out of the two dynamic nodes is exchanged amid one CLK cycle, the total power utilization is impressively lessened without any degradation in speed. Likewise XCFF has a nearly lower CLK driving load. One of the significant downsides of this configuration is the redundant precharge at node X2 and X1 for information examples holding more 0 s and 1 s, separately. In addition to the vast hold time prerequisite coming about because of the conditional shutoff mechanism, a low to high move in the CLK when the information is held low can result in charge sharing at node X1. This can trigger mistaken move at the output unless the inverter pair Inv1-2 is precisely skewed. This impact of charge sharing gets to be wildly vast when complex capacities are inserted into the design.

Dual Dynamic Hybrid Flip Flop

Dual Dynamic Hybrid Flip-Flop (DDFF) which has additional inv4 involves an extra territory to flip flop and after that its obliges more power. QB in the output is inverted by inv3, gets output as Q. So the output Q is again inverted and it's not needed. A standout amongst the most downside of DDFF is huge area and more power. Inv4 which causes.

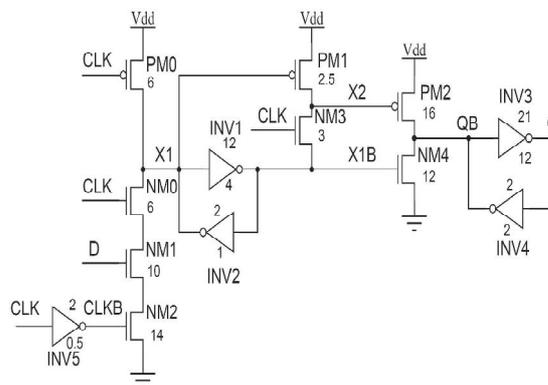


FIGURE-3

V.DDFF

In the DDFF architecture, Nodex1 is pseudo-dynamic, with a Weak inverter going about as a keeper, whereas, contrasted with the XCFF, in the new architecture node X2 is purely dynamic. An unconditional shutoff mechanism is given at the frontend rather than the conditional one in XCFF. The operation of the flip-flop could be partitioned into two stages: 1) the evaluation stage, when CLK is high, and 2) the precharge stage, at the point when CLK is low. The genuine latching happens amid the 1-1 overlap of CLK and CLKB amid the evaluation stage. On the off chance that D is high preceding this overlap period, node X1 is discharged through Nm0-2. This switches the state of the cross coupled inverter pair Inv1-2 bringing about node X1b to go high and output QB to discharge through Nm4. The low level at the nodex1 is held by the inverter pair Inv1-2 for whatever is left of the evaluation stage where no latching

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happens. Accordingly, node x_2 is held high all through the evaluation period by the PMOS transistor p_m1 . As the CLK falls low, the circuit enters the precharge stage and node X1 is pulled high through P_m0 , switching the state of Inv1-2. Amid this period node X2 is not energetically driven by any transistor, it stores the charge dynamically. The outputs at node QB and keep up their voltage levels through Inv3-4. In the event that D is zero preceding the overlap period, node X1 stays high and node x_2 is pulled low through n_m3 as the CLK goes high. Along these lines, node QB is charged high through P_m2 and n_m4 is held off. At the end of the evaluation stage, as the CLK falls low, node X1 stays high and x_2 stores the charge dynamically. The architecture shows negative setup time since the short transparency period characterized by the 1–1 overlap CLK of and CLKB permits the information to be sampled significantly after the rising edge of the CLK before CLKB falls low. Node x_1 experiences charge sharing when the CLK makes a low to high transition while D is held low. These results in a transient fall in voltage at node x_1 , yet the inverter pair Inv1-2 is skewed legitimately such that it has a switching limit well beneath the most detrimental possibility voltage drop at node x_1 because of charge sharing. The timing graph demonstrates that node X2 holds the charge level amid the precharge stage when it is not driven by any transistor. Note that the temporary pull-down at node X2 when sampling a “one” is because of the delay between X1 and X1B.

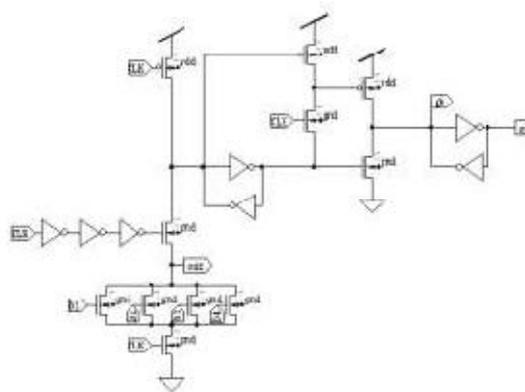


FIGURE-4

Dual dynamic node hybrid flip-flop with embedding logic ability (DDFF-ELM) transistor driven by the information data is supplanted by the PDN and the clocking plan in the frontend is changed. The purpose behind this in timing is the charge sharing, which gets to be wild as the number of NMOS transistors in the stack builds. The same reason makes XCFF additionally unequipped for embedding complex logic functions. With a specific end goal to get an acceptable picture of the charge sharing in XCFF, it was re-enacted with distinctive installed capacities and the measure of most pessimistic scenario charge sharing was figured.

VLSIMULATION

These circuits are simulated in Tanner using TSMC025

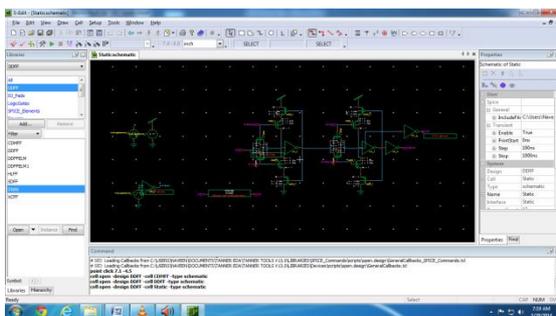


FIGURE-5: STATIC FLIP-FLOP DESIGN

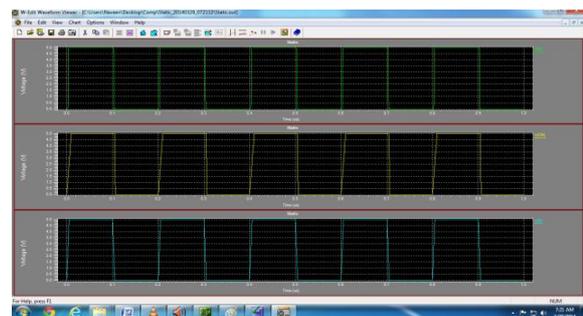


FIGURE-6: STATIC FLIP-FLOP DESIGN SIMULATION

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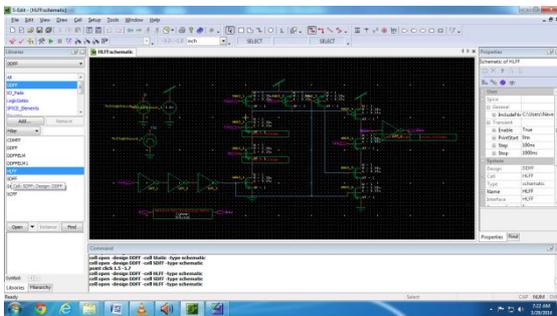


FIGURE-7: HLFF FLIP-FLOP DESIGN

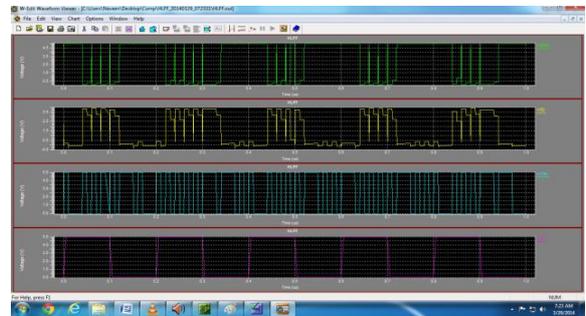


FIGURE-8 HLFF FLIP-FLOP DESIGN SIMULATION

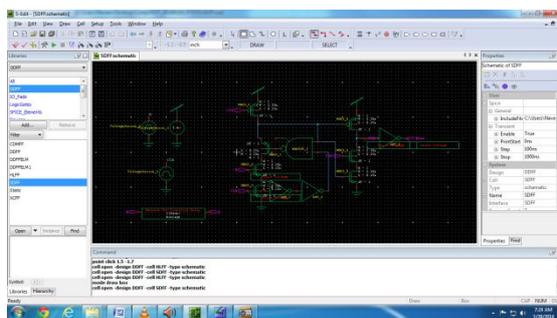


FIGURE-9-SDF FLIP-FLOP DESIGN

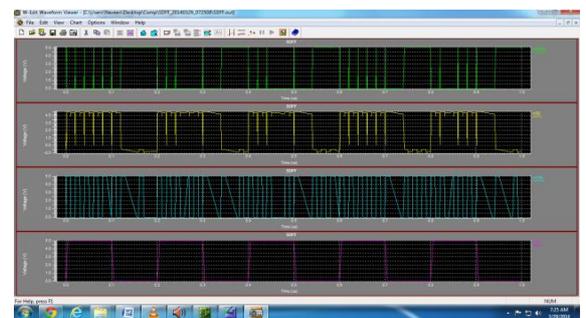


FIGURE-10 SDF FLIP-FLOP DESIGN SIMULATION

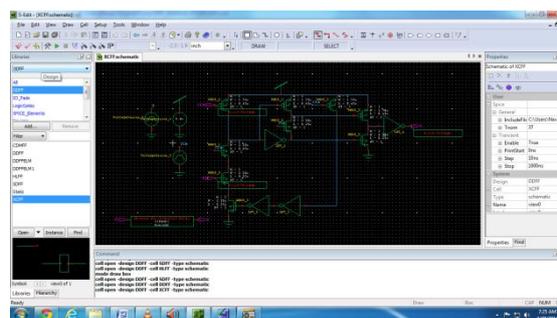


FIGURE-11 XCFF FLIP-FLOP DESIGN

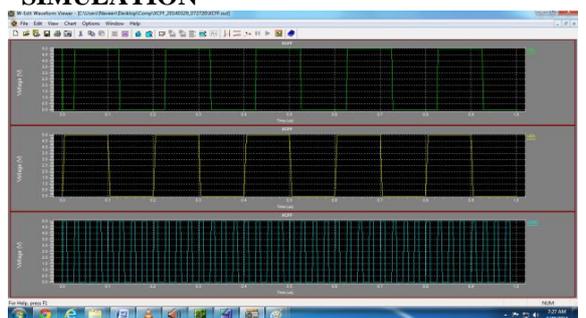


FIGURE-12 XCFF FLIP-FLOP DESIGN SIMULATION

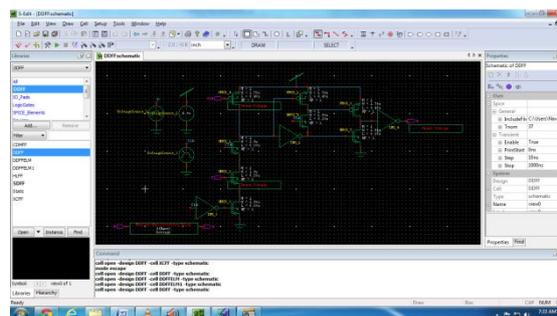


FIGURE-13- DDFF FLIP-FLOP DESIGN

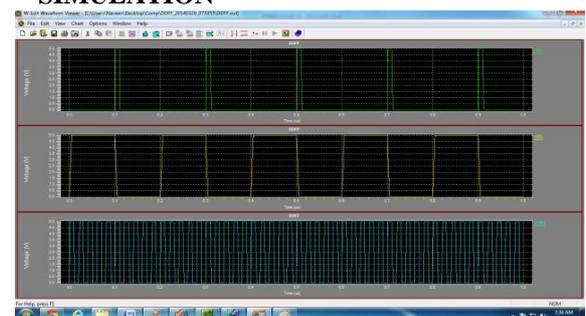


FIGURE-14DDFF FLIP-FLOP DESIGN SIMULATION

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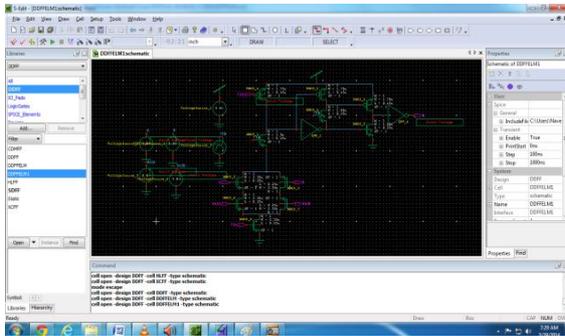


FIGURE-16 DFF FLIP FLOP DESIGN WITH NAND AS ELM NAND AS ELM

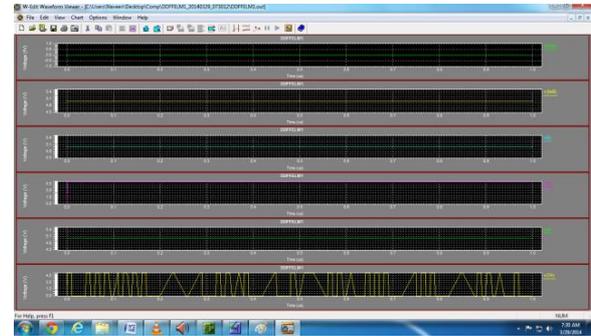


FIGURE-17 DFF FLIP FLOP DESIGN WITH SIMULATION

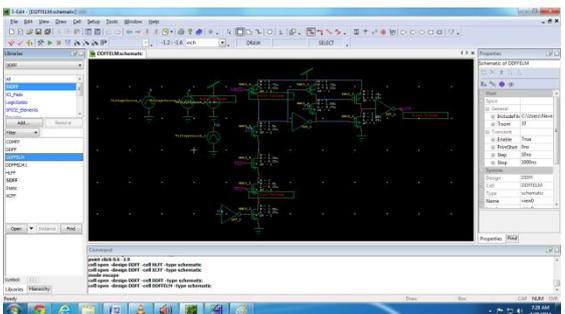


FIGURE-18 DFF FLIP FLOP DESIGN WITH MUX AS ELM MUX AS ELM

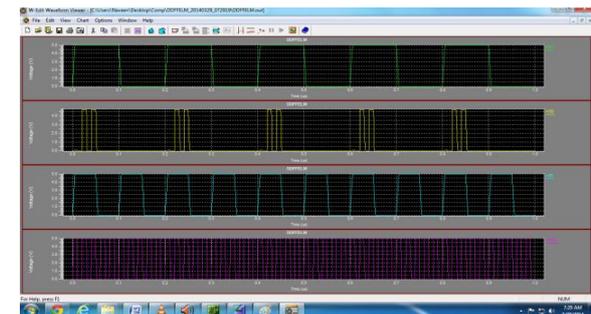


FIGURE-19 DFF FLIP-FLOP DESIGN WITH SIMULATION

TABULATION

The below table shows the power dissipation of individual circuit.

Circuits	Power Pc	HLFF	Sdff	XcFF	DDFF
Power Dissipation	$2.269 \times 10^{-4} \text{W}$	$8.57 \times 10^{-4} \text{W}$	$7.58 \times 10^{-4} \text{W}$	$2.4 \times 10^{-4} \text{W}$	$2.31 \times 10^{-4} \text{W}$

VII. CONCLUSION

The results are compared with the current Technique. The classification of performance execution examination of existing and proposed methods is appeared. The active device has impressively expanded when contrasted with the proposed techniques. In this paper, a new low power DDFF and a novel DDFFELM were proposed. An investigation of the overlap period needed to choose proper pulse width was given keeping in mind the end goal to make the configuration process easier.



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BIOGRAPHY

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