

# Improving Voltage and Frequency of DC –DC Converter using ZCS and ZVS for Low Power and High Power Applications

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**Abstract:** In the phase shifted full bridge (PSFB) pulse width modulation (PWM) converter, external snubber capacitors are connected in parallel to insulated gate bipolar transistors (IGBTs) in order to decrease turn-off losses. The zero voltage transition (ZVT) condition is not provided at light loads, thus the parallel capacitors discharge through IGBTs at turn on which causes switching losses and failure risk of the IGBTs. Capacitor discharge through IGBT restricts the use of high-value snubber capacitors, and turnoff loss of the IGBT increases at high currents. This problematic condition occurs especially at the lagging leg. In this study, a new technique enabling the use of high-value snubber capacitors with the lagging leg of the PSFB PWM converter is proposed. As advantages of the proposed technique, high-capacitive discharge current through IGBT is prevented at light loads, the turn-off switching losses of the IGBTs are decreased, and the performance of the converter is improved at high currents. The proposed PSFB PWM converter includes an auxiliary circuit, and it has a simple structure, low cost, and ease of control as well. The operation principle and detailed design procedure of the converter are presented. The theoretical analysis is verified exactly by a prototype of 75 kHz and 10kW converter. The implementation results are presented.

## I. INTRODUCTION

NEW techniques are proposed in order to decrease switching losses and to increase power density in dc–dc converters at high power and frequencies [1]–[4]. The applications of soft-switching methods are expanding. The most remarkable method in high-power isolated applications is Phase Shifted (PS) Zero Voltage Switching (ZVS) method, which provides all of the switches to operate with ZVS without any additional auxiliary switches. The parasitic capacitance energy is discharged

by the leakage inductance, and the MOSFET turns on with zero voltage transition (ZVT). Insulated gate bipolar transistor (IGBT) is preferred over MOSFET at high voltage and high-power levels in industrial applications. Low R<sub>DS(on)</sub>MOSFETs are quite expensive compared to the IGBTs with equivalent current and voltage ratings. The choice of IGBT over MOSFET is mandatory due to nonavailability of high voltage and high-current MOSFET devices in some applications. An external snubber capacitor is connected in parallel to each IGBT in order to decrease turn-off losses, in case the IGBT is used in the phase shifted full bridge (PSFB) pulse width modulation (PWM) converter [5]–[26]. When the ZVT condition is not provided at no load and at light loads, the parallel capacitors discharge through IGBT at turn on and this causes increase in switching losses and failure risk of the IGBTs. This condition causes problems at specially the lagging leg [5]–[26]. Capacitor discharge through IGBT restricts the use of high-value capacitor in parallel to IGBT. Therefore, the election of the parallel capacitor value is very important. The parallel snubber capacitor value should be selected according to the speed and the maximum current of the IGBT [5]. The performance of the converter decreases rapidly at high-current levels because of the turn-off switching losses. At the leading leg, the required energy for discharging the parallel capacitor is supplied from the load current, so the use of high-value capacitor in the leading leg has no drawback.

In PSFB PWM dc–dc converters, some problems arises such as variation of duty cycle with load current, hard switching because of insufficient energy in leakage inductance at light loads, and high-voltage peaks and oscillations at the output diodes, and increment in the conduction losses because of the primary current flowing in the freewheeling interval. It is possible to encounter many studies in the literature about these converters and solution for the problems [5]–[26].

In [6], the required large resonant inductor is replaced with linear variable inductor (LVI) which is controlled by output current. The required energy for ZVS operation at low-current levels is obtained by means of the high value of the LVI. The value of LVI decreases approximately linearly with increasing current. The soft-switching operation range is extended and dependency of ZVS operation on the load current is decreased.

In [7], an auxiliary circuit which includes two MOSFETs and a serial inductance is proposed. The inductance current is increased before the IGBT devices on the lagging leg are turned off. The ZVS conditions of the FB converter are improved, but the losses in the auxiliary circuit reduce the efficiency. The auxiliary circuit does not operate with soft switching. Main IGBTs are subjected to the current stress before turn off and this increases the switching losses in the turn-off process. The proposed method is not preferred due to low efficiency, high cost, and control difficulty.

In [8], the ZVS operation is achieved over the entire conversion range in the PSFB PWM converter for an ohmic load. The proposed converter is suitable for the applications, where load current proportionally increases with output voltage. When

prevented, and turn-off switching losses of the IGBTs are decreased. This novel converter requires resonant inductance much less than conventional PSFB PWM converter. The proposed method decreases the turn-off switching losses at high currents and improves the performance of the converter. Besides, parasitic oscillations and conduction losses of output diodes are decreased. The theoretical analysis of the proposed converter is given and verified exactly by a prototype of 75 kHz and 10kW converter.

## II. OPERATION PRINCIPLES AND ANALYSIS

### A. Definition and Assumptions

The proposed converter is shown in Fig. 1. It consists of a conventional PSFB PWM converter and an auxiliary circuit connected to the lagging leg. The auxiliary circuit contains two IGBTs with reverse recovery diodes and two capacitors C1A, C2A. At low-output currents, converter operates as the conventional PSFB PWM converter. Low-valued snubber capacitors are connected at the lagging leg. These capacitors provide ZVS operation at light loads and improve the turn-off behavior of the IGBT until a current level.

In the proposed converter, auxiliary circuit is operated only at high-output currents. By means of the auxiliary circuit, high value capacitors are connected to the lagging leg and the turnoff performance of the lagging leg switches is improved. The IGBTs used in the auxiliary circuit operate under soft-switching conditions. The conduction loss of the auxiliary switches is very low because they conduct current for a very short time. The operation of the auxiliary circuit starts when primary current IP is larger than boundary current level Ia.

The following assumptions are made to simplify the steady state analysis of the circuit during one switching cycle:

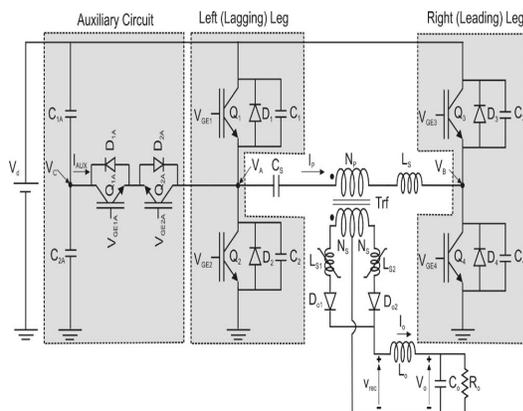


Fig. 1. Proposed PSFB PWM converter.

duty ratio is low and output current is high, soft switching is not provided.

In this study, a novel auxiliary circuit for the PSFB PWM converter using IGBTs is proposed. The proposed circuit enables the use of high-value capacitors with the lagging leg of the PSFB PWM converter without any problems. At no load, detrimental effects of the surge current to the IGBT due to the snubber capacitors are

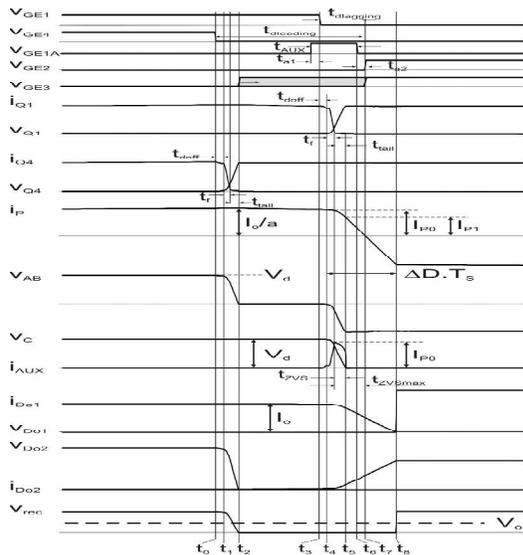


Fig. 2. Key waveforms concerning the operation stages in the proposed PSFB PWM converter.

- 1) input voltage  $V_d$  is constant;
- 2) equivalent series inductances of the parallel snubber capacitors are neglected;
- 3) the blocking capacitor  $C_S$  is large enough to be neglected at high-frequency operation;
- 4) the effect of the saturable inductors used to prevent parasitic oscillations at the secondary are neglected.

### B. Operation Stages

The basic operation of the proposed soft-switching converter has six operating stages within each half cycle. The operation waveforms are shown in Fig. 2. The equivalent circuits for each operating stage are shown in Fig. 3(a)–(f).

Stage 1 ( $[t_0 < t < t_1$  : Fig. 3(a)]: At the beginning of this stage, Q1 and Q4 are conducting, input voltage  $V_d$  is applied to the transformer's primary and power is transferred to the output. Output current flows through the diode  $D_{o1}$ . The initial voltage of  $V_C$  is equal to  $V_d$ . At  $t = t_0$ , drive signal  $V_{GE4}$  is removed and Q4 starts to turn off. At the beginning of the turn-off process there exists a delay defined as  $t_{doff}$ . In this interval  $i_{Q1} = i_{Q4} = I_P$ , Q4 is still in the on-state and current flows through the transistor.

Stage 2 ( $[t_1 < t < t_2$  : Fig. 3(b)]: In the turn-off process of Q4 two intervals occur which are defined as current fall time  $t_f$ , and tail current time  $t_{tail}$ . The current of Q4 begins to decrease after  $t_1$  and it falls to  $I_{tail}$  value at the end of  $t_f$ . In this interval, there is little increase on the voltage of Q4 because of the parallel capacitors. The

turn-off loss of the IGBT is very low in comparison to the hard switching case. In this stage, the parallel capacitor  $C_P$  is the sum of  $C_3$  and  $C_4$ . The leakage capacitor of the transformer is neglected in respect of parallel capacitor.

If  $t_{tail}$  is neglected, the parallel capacitor is assumed to charge linearly. The voltage of Q4 is given by

$$V_{Q4} = \frac{-I_P t_f}{C_P} \quad (1)$$

When the voltage of Q4 reaches to  $V_d$ , D3 starts to conduct. The turn-off loss of Q4 is approximated as

$$E_{off} = \frac{t_f^2 I_P^2}{24 C_P} \quad (2)$$

Stage 3 ( $[t_2 < t < t_3$  : Fig. 3(c)]: This interval starts at  $t = t_2$ , when D3 diode turns on. Q1 and D3 are conducting in this freewheeling interval. After the diode D3 turns on, the drive signal of Q3 can be applied. The signal should be applied before the primary current  $I_P$  becomes zero. At  $t = t_3$ , drive signal  $V_{GE1}$  is removed and this interval begins. At the beginning of the turn-off process there exists a delay defined as  $t_{doff}$ . The transistor is still in the on-state and current flows through the transistor.

Stage 4 ( $[t_4 < t < t_5$  : Fig. 3(d)]: At  $t = t_4$ , lagging leg transition begins. The initial value of primary current is  $I_P = 0$ . In this stage two different operation modes occur depending on the primary current level. If the primary current is smaller than  $I_a$ , auxiliary circuit is not activated (Mode-1). This mode of the converter would have conventional operation. Proposed converter waveforms are the same as the conventional one's except  $V_{GE1A}$ ,  $V_C$ , and  $I_{AUX}$ . In this case, the parallel capacitor,  $C_P$  is the sum of  $C_1$  and  $C_2$ . The inductance energy is enough to charge the low-valued snubber capacitors, and soft switching is obtained. If primary current is larger than  $I_a$ , auxiliary circuit is operated (Mode-2) as shown in Fig. 3(d). In this case, the parallel capacitor,  $C_P$  is the sum of  $C_1$ ,  $C_2$ ,  $C_{1A}$ , and  $C_{2A}$ . Due to additional high-valued capacitors, soft switching is obtained at high-current levels. The waveforms given in Fig. 2 are drawn for Mode-2. This interval is completed with discharge of the capacitor ( $C_2 // C_{2A}$ ) through the resonance between  $L_S$  and  $C_P$ , and primary current falls to  $I_{P1}$  level.

Stage 5 ( $[t_5 < t < t_7$  : Fig. 3(e)]: When D2 diode turns on at  $t = t_5$ , negative voltage is applied to  $L_S$ , and current falls to zero linearly. After the diode D2 turns on, the drive signal of Q2 can be applied. The auxiliary switch drive signal is removed at  $t = t_6$ . This interval is completed when the primary current falls to zero.

Stage 6 ( $t_7 < t < t_8$  : Fig. 3(f)): In this interval, primary current decreases from 0 to  $-I_o/a$ . At  $t = t_8$ , the current of Do1 falls to zero and output current is commutated to Do2. After  $t_8$ , normal PWM operation takes place and power is transferred to the output. The operation in the second half cycle is symmetrical to the first one, and a new TS period starts after the second half cycle.

energy should be sufficient to charge/discharge parallel capacitors

$$1/2LsIp^2 \geq 1/2CpVd^2 \quad (6)$$

From this equation, the minimum current level  $I_{P \text{ min}}$  required to provide ZVS is given by

$$I_{pmin} = Vd\sqrt{Cp/Ls} \quad (7)$$

### III. MAIN FEATURES AND DESIGN PROCEDURE

In this section, the design procedure of the proposed converter is given. The component values for implementing the converter are determined according to the design procedure.

#### A. Selection of the Boundary Current $I_a$

The boundary current level  $I_a$  that auxiliary circuit starts to operate is

$$I_a = Vd\sqrt{Cp/Ls} \quad (3)$$

The ZVS operation range of the lagging leg switches is increased with decreasing  $I_a$ . Low  $I_a$  value is obtained by selecting low CP value and high LS value. In the case of low CP value, the turn-off losses increases. High value of LS is not appropriate because it increases conduction and duty cycle losses. Besides, the selection of  $I_a$  also depends on the characteristics of the IGBTs, and nominal current of the converter.

#### B. Control Signals and Dead-Time Requirements

The required dead time between Q3 and Q4 Switches of the leading leg,  $td_{leading}$ , should provide

$$td_{leading} > tdoff + tf + ttail \quad (4)$$

where,  $tdoff$  is turn-off delay time,  $tf$  is fall time of the current to the tail current level, and  $ttail$  is the tail current time. The required dead time between Q1 and Q2 switches of the lagging leg,  $td_{lagging}$ , should provide following condition:

$$td_{lagging} > tdoff + tf + ttail \quad (5)$$

The required dead time between lagging leg switches varies depending on the primary current. In order to turn off lagging leg switches with ZVS, the stored inductance

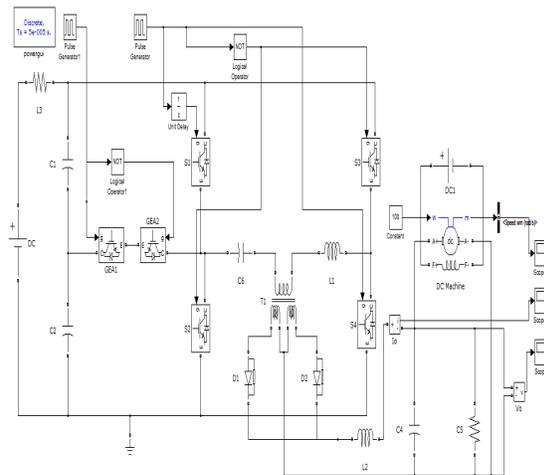
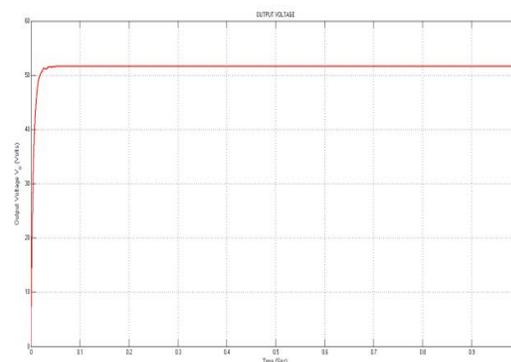
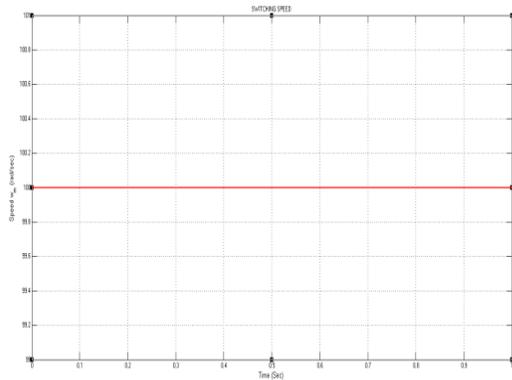


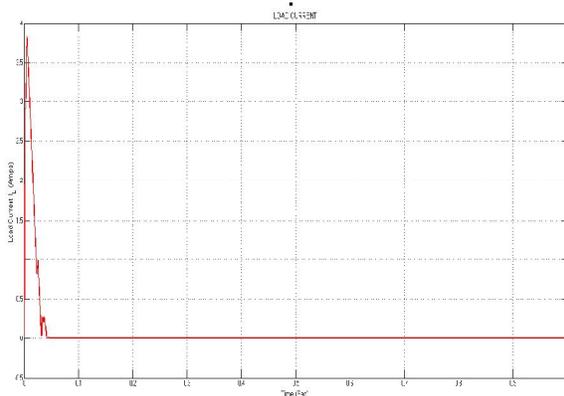
Fig.3. Simulation Circuit Diagram



(a).Output Voltage



(b).Switching Speed



(c).Output Load Current

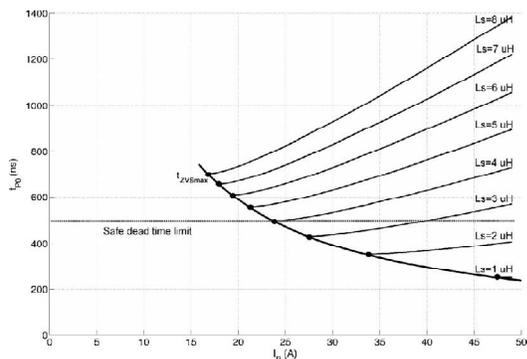


Fig. 4. Characteristics of the proposed converter for CP = 25 nF.

As seen from Fig. 6, for LS values smaller than 5  $\mu\text{H}$ , minimum dead-time requirement (500 ns) is not satisfied. As a result, LS inductance can be chosen between 5  $\mu\text{H}$  and 8  $\mu\text{H}$ . The calculated  $I_a$ ,  $t_{ZVSmax}$ ,  $t_{P0}$ , and  $\Delta D$  variables for the values of LS.

In the proposed converter, shown in Fig 3. The output voltage, output load current and witching speed are shown. The selected values of CP and LS provide ZVT operation from 8.9 to 40A primary current for the IGBTs in the lagging leg. The use of the same component values in the conventional SFBPWM converter results in ZVT operation from 21.21 A to 40A primary current. In order to start ZVT operation at the same primary current in conventional PSFB PWM converter, 25  $\mu\text{H}$  inductance value is required which results an increase in duty cycle loss as much as five times.

The proposed converter, turn-off loss of the lagging leg switches is four times lower than that of the conventional converter, at full load. If the operation frequency is higher this advantage becomes more evident.

#### IV. CONCLUSION

In this study, a new method enabling the use of high-valued snubber capacitors with the lagging leg of the PSFB PWM converter is developed. Thanks to the new method, the turnoff switching losses are decreased, and the performance of the converter is improved at high currents. In the proposed PSFB PWM converter, IGBTs are used instead of MOSFETs due to their low cost and low-conduction losses. Auxiliary circuit is operated only during charging/discharging of capacitor at the lagging leg thus conduction loss is low. The control and design principles are similar to the conventional PSFB PWM converter.

The proposed topology has the following advantages compared to the other PSFB PWM converters presented in the literature:

- 1) Turn-off losses of the lagging leg IGBTs are decreased by the use of high-valued snubber capacitors.
- 2) It is possible to select resonant inductance smaller and to decrease duty cycle loss. Auxiliary circuit is started at high currents, so the required energy for discharging high-valued snubber capacitors is available.
- 3) Transformer conversion ratio can be selected higher, thus resulting in lower conduction losses.
- 4) At no load, detrimental effects of the surge current to the IGBT and snubber capacitors are prevented, and turn-off switching losses of the IGBTs are decreased.
- 5) All semiconductor devices in the circuit are switched under soft switching at wide load range. The main switches are perfectly turned on and turn off with ZVT

and ZVS, respectively. The auxiliary switches are turned on and turn off with ZVS.

6) At very low-current levels soft switching is lost but in this case, the switching losses are negligible.

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