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Novel Digital Active Emi Filter Used In A Grid-Tied PV Microinverter Module

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ABSTRACT: This paper presents the EMI reduction by the novel digital active technique used in a grid tied PV micro inverter module. The most commonly used passive EMI filter used for EMI mitigation in power converters comes at the expense of cost, size, weight power losses, and PCB real estate. DAEF is implemented with a grid tied photovoltaic micro inverter .the inverter stability is analyzed with the DAEF by the overall transfer function. The system compensation is designed based on the direct quadrant frame control technique.

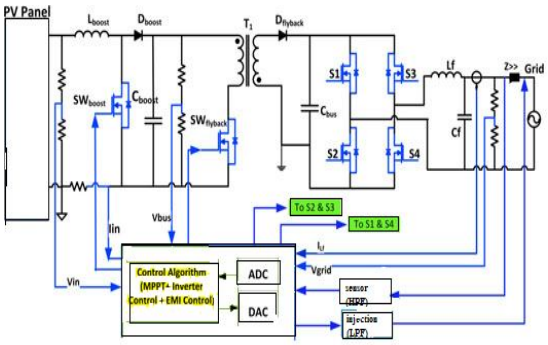
I. INTRODUCTION

The micro inverter architecture is used to connect the grid to convert the solar energy from PV panels and feed it to the grid with high efficiency and high power quality. The two main functions have done by the converter are as follows:

1. Dc/ac power conversion.
2. Tracking the maximum power delivered by the PV panel to maximize the energy throughput.

The fast dI/dt and dV/dt causes the fundamental and high frequency harmonics in the switching pulses of the inverter due to the non linear action of the switching semiconductor devices.
EMC compliance involves a series of measures to reduce conducted emission at the source. This can be done by diverting CM noise away from ground. Cost, size, and the space of the overall power inverter PCB. other EMI suppression technique
The basic noise suppression technique is a passive EMI filter which gives the better performance but the
Such as the spread spectrum frequency modulation and soft switching techniques has provide the less performance. Active analog EMI filters provides the low cost and ease of use .but it needs additional passive elements to noise attenuation of the spread spectrum .the deaf provides the best performance than the previous EMI noise suppression techniques, used in the industrial applications, the DSP program to check the stability analysis of the inverter and FPGA program to the EMI control algorithm have been used in this paper.
This paper is partitioned as follows; in Section II, general descriptions of the micro inverters architecture and its inverter circuit including power conversion stages and controllers are presented. In Section III, the output inductor current control using a direct quadrature (*DQ*) reference frame control technique is explained. The open-loop transfer function (TF) of the micro inverter is derived to investigate the stability of the inverter in Section IV. Section V presents the controller design for micro inverter compensation and stability verification. Experimental results showing the performance of the DAEF in the micro inverter are illustrated in Section VI. Finally, a conclusion is given in Section VII.

II. MICROINVERTER'S ARCHITECTURE AND CIRCUIT DESCRIPTION



The power circuit consists of micro inverter

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Two stages: dc/dc converter, and dc/ac converters. The functions. The first one is the boosting dc voltage to feed which is required by the grid .the second one is tracking the maximum power delivered by the photo voltaic panel to maximize the energy throughput. Then the second- stage dc/ac inverter converts the dc power into an instantaneous current and voltage suitable for the grid injection.

The digital control system consists of three main control functions: the maximum power point tracking (MPPT) control, the output inductor current I_{lf} control, and the EMI control.

Therefore, in the case of the two-stage micro inverter, a control algorithm is designed to keep the first stage of the inverter (dc/dc converter) operating at the maximum power, while the second - stage control algorithm is dedicated to regulate the instantaneous current or voltage to be injected into the grid.

DAEF CONTROLLER:

The rated current voltage of the power inverter depends on the size and losses of the filter. It is improved by the DAEF. It provides the maximum optimization of the inverter. The emulation of the incident CM noise signal in terms of amplitude and frequency is used for the DAEF. RF sensor senses the high frequency harmonics generated by the inverter, is used for the emulation process. The common mode interference signal is minimized by the digitally inverting the emulating signal. Then reconstruct the signal and inject back. It is generated by inverter switching circuitry.

The figure shows the digital active EMI filter with the grid side interface. The CM Noise voltage is sensed from the output of the inverter through RC high pass filter. It is input to the DAEF. it is sampled though high speed analog to digital converter. Then inverted using a binary inverter which output again converted by Digital to analog converter. The reconstructed signal is injected again back to the input lead of the power grid using a low pass filter which consist of capacitor and inductor. The low pass filter tuned to high frequency spectrum of the conducted emission standard.

C_{inject} is also used to prevent the ADC from being loaded by the power inverter. A high impedance inductor is located between the noise sensor and the grid as a decoupling network. In this process, only one control parameter is required by the digital processor in order to replicate the original sensed signal.

DC/DC two architecture consist of the

Output current controller

The DQ reference frame control technique is applied for controlling the instantaneous inductor current of single phase dc/ac inverter. In a *DQ* reference frame, the physical (Real) circuit, in conjunction with an "imaginary orthogonal circuit," is transformed from the stationary frame to the *DQ* rotating frame so that the steady-state variables, voltage or current at the fundamental frequency, in the *DQ* frame become dc variables allowing the design of controller using design techniques developed for dc/dc converters. This design approach can achieve very high control gain which results in zero steady-state error at the fundamental frequency and better dynamic performance of the system. The following section provides a detailed analysis of the dc/ac inverter control technique.

III. OUTPUT CURRENT CONTROL IN A *DQ* FRAME

The controller architecture using the *DQ* reference frame control technique of the two-stage micro inverter is depicted in Fig. 4. This controller diagram consists of three control blocks: MPPT controller, EMI controller, and the output inductor current controller. Only the last controller algorithm will be discussed in this section.

In Fig. 4, it can be seen that the real variables, which are the output inductor current I_{lf} and the grid voltage V_{grid} are used to construct the imaginary circuit variables *ID* and IQ. These later are transformed into the *DQ* rotating frame using the real– imaginary (*RI*) stationary frame. The initial phase θ of the output voltage *V*grids locked using a phase-locked loop. The initial phase is used as a phase reference at the inverse transformation stage. The proportional and integral (PI) compensator is designed in the rotating frame with constant current reference *ID* ref and *IQ* ref . This generates the duty cycle control signals *Duty_Q* and *Duty_D*. The next step is the inverse transform of the duty cycle signals from *DQ* frame to *RI* stationary frame. Finally, the duty cycle signals of the imaginary circuit are decoupled from the *RI* stationary frame and only the duty ratio of the real circuit is applied to the dc/ac inverter stage.

The decoupling process is done using the initial phase reference to discard the imaginary function being a $\cos(\omega t)$ or $\sin(\omega t)$, orthogonal at 90◦ phase shift, i.e., when the initial phase is a $\sin(\omega t)$, the $\cos(\omega t)$ of the imaginary circuit would be null, $[\cos(90^\circ)] = 0$ and $[\sin(90^\circ)] = 1$; hence, only the duty

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ratio of the real circuit is applied. Equations (1) and (2) provide the definition of the rotating transformation matrix from the stationary frame to *DQ* rotating frame. Equations (3) and (4) show the inverse transformation from the *DQ* rotating frame back to *RI* stationary frame

$$T = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} X_D \\ X_Q \end{bmatrix} = T \begin{bmatrix} X_R \\ X_I \end{bmatrix} = T \begin{bmatrix} X_m \cos(\omega t + \varphi) \\ X_m \sin(\omega t + \varphi) \end{bmatrix} = X_m \begin{bmatrix} \cos\varphi \\ \sin\varphi \end{bmatrix} \quad (2)$$

Where

XD and *XQ* represent the inductor current and the capacitor voltage in the rotating frame. *XR* and *XI* are the real and the imaginary circuit variables, respectively. *Xm* is the peak value of the sinusoidal waveform, ϕ is the initial phase, and ω is the fundamental frequency

$$T_{\text{inv}} = T^T = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} \quad (3)$$

$$\begin{bmatrix} X_R \\ X_I \end{bmatrix} = T_{\text{inv}} \begin{bmatrix} X_D \\ X_Q \end{bmatrix} = \begin{bmatrix} X_m \cos(\omega t + \varphi) \\ X_m \sin(\omega t + \varphi) \end{bmatrix}. \quad (4)$$

The circuit model in *RI* stationary frame is depicted in Fig. 5. The average model of the real and the imaginary circuits can be obtained using the inductor current and the capacitor voltage of the *LC* output filter and can be expressed in (5) and (6)

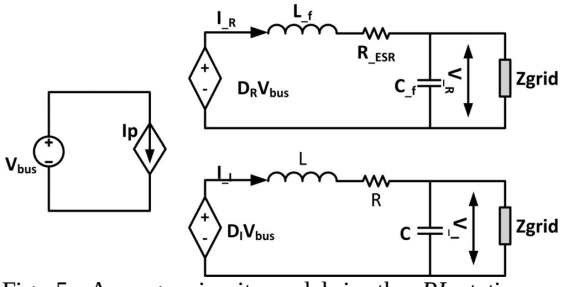

Fig. 5. Average circuit model in the *RI* stationary frame.

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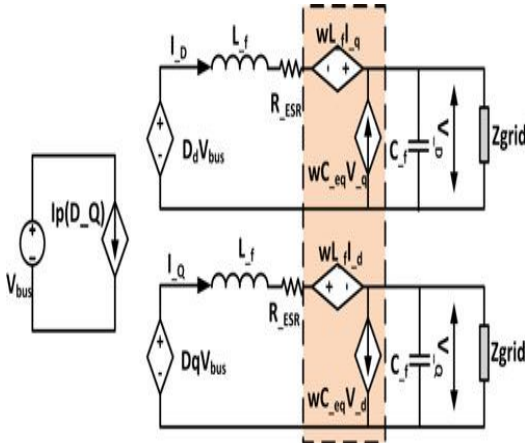

fig.6 Equivalent circuit model in the *DQ* rotating frame

By applying the *DQ* transformation stated in (1) and (2) to (5) and (6) yield a circuit model in the rotating frame which is expressed as

$$\frac{d}{dt}\begin{bmatrix} I_D \\ I_Q \end{bmatrix} = \frac{V_g}{L}\begin{bmatrix} D_D \\ D_Q \end{bmatrix} - \frac{1}{L}\begin{bmatrix} V_D \\ V_Q \end{bmatrix} + \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix}\begin{bmatrix} I_D \\ I_Q \end{bmatrix} \quad (7)$$

$$\frac{d}{dt}\begin{bmatrix} V_R \\ V_I \end{bmatrix} = \frac{1}{C}\begin{bmatrix} I_D \\ I_Q \end{bmatrix} - \frac{1}{Z-C}\begin{bmatrix} V_D \\ V_Q \end{bmatrix} + \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix}\begin{bmatrix} I_D \\ I_Q \end{bmatrix}. \quad (8)$$

The circuit model reflecting this transformation is depicted in Fig. 6. It is important to mention that the vector quantities expressed in (5) and (6) are time-variant, whereas the quantities in (7) and (8) are constant dc values. Hence, the design of the closed loop compensator to ensure the stability of the inverter system can be derived using the conventional method similar to dc/dc converters. This is realized in the next section.

IV. INVESTIGATION OF THE INVERTER STABILITY

To verify the seamless coexistence of the DAEF and the digital output current controller of the micro inverter, it is required to investigate the stability of the inverter. This can be achieved by deriving the open-loop TF of the micro inverter and using one of the stability criteria such as root-locus or gain-phase margin techniques. Furthermore, a compensator or a controller design is required to satisfy the stability conditions under different load and line variations.
Design parameters of the microinverter are based on microinverter product, and are given as follows:

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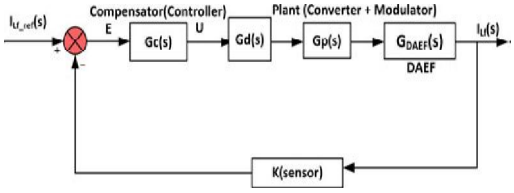

Fig. 7. Current control loop in continuous time.

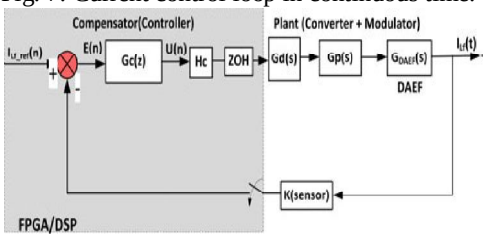

Fig. 8. Corresponding discrete model of the current control

1) topology: first-stage buck–boost dc/dc converter and second-stage full-bridge dc/ac inverter;
2) input voltage *V*in = 30–50 Vdc;
3) output Voltage *V*out = 240 Vac max and output current *I*out = 1.25 A;
4) switching frequency *Fs* = 50 kHz;
5) output filter components, *L* = 500 μH and *C* = 2.2 μF;
6) desired current-loop bandwidth *Fbw* = 10 kHz;
7) desired phase margin PM = 30–90◦.

The block diagram of the inductor current control loop in the s-domain and its corresponding digitized system are shown in Figs. 7 and 8, respectively. Four TFs are required to verify the system stability. These TFs are namely, the plant or the inverter *Gp* (*s*), the decoupling TF resulting from the *DQ* transformation *Gd* (*s*), the DAEF TF GDAEF(*s*), and the compensator *Gc* (*s*) which needs to be designed to fulfill the stability requirement.

The open-loop TF for the system without the compensator can be written as

$$\mathrm{TF}_{\mathrm{op}} = K_m K_b G_d(s)\, G_p(s)\, G_{\mathrm{DAEF}}(s) \qquad (9)$$

where ,

Km is the modulator gain; *Km* = 1/*Vs* and *Vs* is the peak value of the oscillator ramp signal. *Kb* is the plant dc gain, *Kb* = *V*in max. *Gp* (*s*) is the plant TF, which is derived using (5) and (6) as follows:

$$sI_R(s) = \frac{V_g}{L} D_g - \frac{1}{L} V_R(s) \qquad (10)$$

$$sV_R(s) = \frac{1}{C} I_R(s) - \frac{1}{Z - C} V_R(s). \qquad (11)$$

$$I_R(s) = \frac{V_g \cdot D_g - V_R(s)}{s \cdot L} \qquad (12)$$

$$V_R(s) = \frac{Z \cdot I_R(s)}{s \cdot Z \cdot C + 1}. \qquad (13)$$

Substituting (12) into (13) and including the modulator gain *Km* and plant gain *Kb* , the control to output inductor current

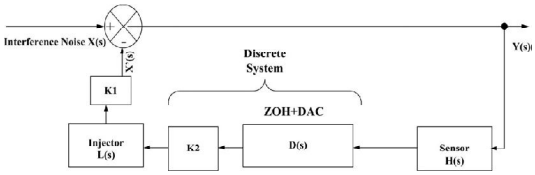

Fig. 9. Control diagram of the DAEF.

TF can be obtained as

$$G_p(s) = \frac{K_m \cdot K_b \cdot V_g}{s^2 \cdot L \cdot C + s\frac{L}{Z} + 1}. \qquad (14)$$

The decoupling TF *Gd* (*s*) is expressed as

$$G_d(s) = \frac{1}{s \cdot L + 1}. \qquad (15)$$

Finally, the TF of the DAEF is derived according to Fig. 9.
The closed-loop TF of the DAEF can be written as

$$G_{\mathrm{DAEF}}(s) = \frac{1}{1 + K_1 K_2 H(s) D(s) L(s)} \qquad (16)$$

where

*K*1 is the injector gain, which is equal to −1 to digitally invert the sensed signal.

*K*2 is the bits inversion algorithm implemented in the DSP device.

H (*s*) is the Laplace transform TF of the high-pass filter and is given by

$$H(s) = \frac{s}{s + \omega_1} \qquad (17)$$

Where ,

ω1 is the corner frequency of the high-pass filter. *L*(s) is the Laplace transform TF of the *RC* low-pass filter which is given by

$$L(s) = \frac{1}{1 + \frac{s}{\omega_2}} \qquad (18)$$

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Where

$\omega 2$ is the corner frequency of the low-pass filter. $D(s)$ is the Laplace transform TF of the zero-order-hold (ZOH) ADC

where T is the ADC clock/sampling period.

The effect of the ZOH on the feedback loop is to increase the gain by a magnitude of sin $\omega T/2$ and introduce a phase shift of $\omega T/2$, which is a negligible time delay. Substituting $H(s)$, $L(s)$, and $D(s)$ into (16) by (17)–(19), respectively, the closed-loop TF of the feedback diagram of Fig. 8 can be expressed as

$$G_{\mathrm{DAEF}}(s) = \frac{(s+\omega_1)(s+\omega_Z)}{s^Z + (\omega_1+\omega_Z)s + \left[\omega_1\omega_Z + \frac{K_1 K_Z \omega_Z}{T}(1-e^{-sT})\right]}. \quad (20)$$

Therefore, by replacing Gp (s), Gd (s), and GDAEF(s) in (9) by (14), (15), and (20), respectively, the uncompensated control to-inductor current open-loop TF of the micro inverter system can be evaluated in MATLAB. The Bode plot of the open-loop uncompensated system TF is shown in Fig. 10. The plot exhibits an unstable system, with infinite phase margin and the −20-dB slope is far from crossing the unity gain line (0-dB line). Hence, to satisfy the stability criteria, the system must be compensated.

V. COMPENSATOR DESIGN

As previously mentioned, the output current control in DQ frame converts the sinusoidal steady state into a dc steady-state operating point. This conversion allows the micro inverter compensator to be designed according to dc/dc converters design method. Using a digital redesign approach, a type III compensator is found to be adequate for this seventh-order control system (9) to achieve stability requirements and fast transient response is formulated in the s-domain using a conventional analog design method. The continuous-time TF is then converted into a discrete time using a bilinear approximation method. The digital compensator is finally implemented in an FPGA using descriptive language. In this section, only the design procedure in the s-domain is presented for the purpose to verify that the designed compensator can satisfy the stability criteria under different load and line conditions. The type III compensator is referred to as a double-pole double-zero compensation network because it introduces double zeros into the error amplifier compensation to reduce the steep gain slope above the double pole caused by the LC filter and its associated −180◦ phase shift. The circuit diagram of the type III compensator is shown in Fig. 11, and its TF is given by

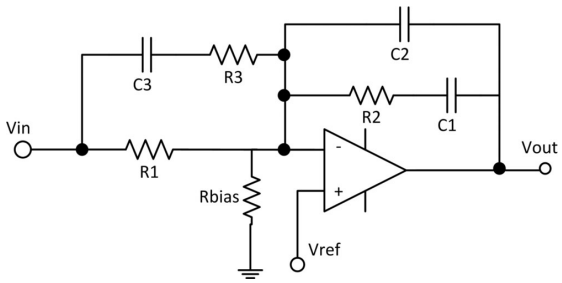

Fig 11. Schematic diagram of the type III compensator.

$$G_C(s) = \frac{(1+sR_2C_1)[1+sC_3(R_1+R_3)]}{sR_1(C_1+C_2)(1+sR_3C_3)\left(1+sR_2\frac{C_1C_2}{C_1+C_2}\right)}. \quad (21)$$

$R1$ is arbitrarily chosen to be $10K$, so that the parameter values of the circuit can be evaluated using the K-factor method as follows:

$$K = \tan\left(\frac{M-P-90^\circ}{4}+45^\circ\right) \quad (22)$$

Where

M is the desired phase margin chosen as 45◦. P is the phase shift of the converter at crossover frequency, which is equal to 92◦ according to Fig. 9

$$C_2 = \frac{1}{2\pi F_c G_{\mathrm{EA}} R_1} = 15.2\ \mathrm{pF} \quad (23)$$

$$C_1 = C_2(K-1) = 20\ \mathrm{pF} \quad (24)$$

$$R_2 = \frac{\sqrt{K}}{2\pi F_c C_1} = 1.2\ \mathrm{M\Omega} \quad (25)$$

$$R_3 = \frac{R_1}{K-1} = 7.5\ \mathrm{k\Omega} \quad (26)$$

$$C_3 = \frac{1}{2\pi F_c \sqrt{K} R_3} = 1.4\ \mathrm{nF}. \quad (27)$$

The type III compensator has a double zero located at a frequency fz below Fc , and a double pole located at a frequency fp above Fc given as

$$f_z = \frac{F_c}{\sqrt{K}} = 6.5\ \mathrm{kHz} \quad (28)$$

$$f_p = F_c\sqrt{K} = 15.2\ \mathrm{kHz}. \quad (29)$$

The control-to-inductor current TF of the micro inverter system (30), including the compensator, is evaluated in MATLAB

$$TF_{\mathrm{comp}} = K_m K_b G_d(s) G_p(s) F(s) G_c(s). \quad (30)$$

The Bode plot of the micro inverter compensated control system is shown in Fig. 12. It can be seen that the control system exhibits a gain margin of 28 dB and phase margin of 79◦. These parameters are large enough in providing the desired stability of the closed-loop control system.

The Nyquist plot, including the time delay produced by the ZOH function, is shown in Fig. 13.

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According to the Nyquist theorem, the net number of the encirclement N is equal to the number of zeros in the right half-plane (RHP) minus the number of open-loop poles P in the RHP; in other words

$$N = Z - P. \quad (31)$$

In the case of the micro inverter, the number of poles of the open-loop TF is $P = 0$, and the number of zeros in the RHP of the closed-loop TF is $Z = 0$; therefore, $N = 0$, which implies that the system is stable. This is shown in Fig. 13, where there is no encirclement of the -1 point. This also proves that the ZOH delay function is insignificantly low to have an impact on the system stability.

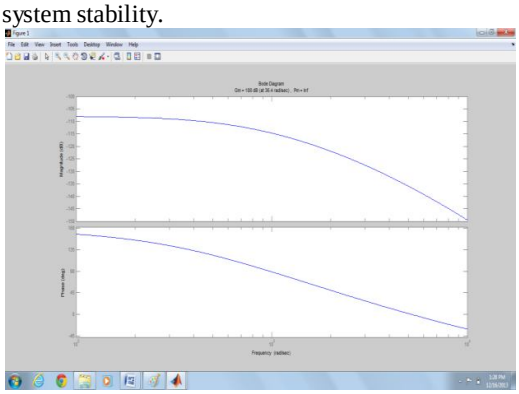

fig.10Bode plot of the open loop un-compensated control system.

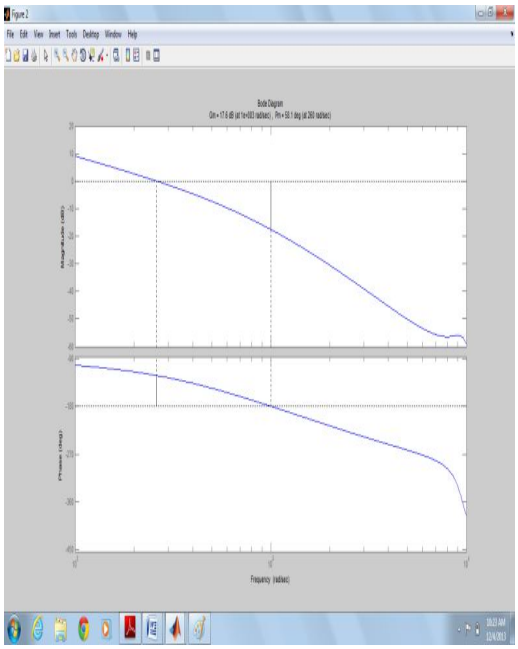

Fig. 11 Open Loop Phase & Gain Margin

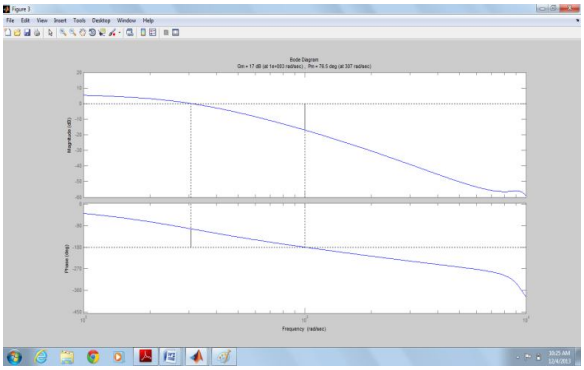

Fig.12 closed loopPhase&GainMargin

num/den =

-200 s^2

-0.05 s^4 + 40000500 s^3 + 399999999804.0001 s^2 + 40000 s

num/den = -1600000 s^2

2.75e-014 s^7 + 2.2042e-005 s^6 + 33.5979 s^5 + 420441.1332 s^4 + 906667166.2754 s^3 + 399999999890.6668 s^2 + 40000 s

num/den = 5.8e-010 s^2 + 4.8e-005 s + 1

3.8e-015 s^3 + 7.3e-012 s^2 + 3.5e-007 s

num/den = 0.0232 s^4 + 1920 s^3 + 40000000 s^2

1.045e-028 s^10 + 8.376e-020 s^9 + 1.2783e-013 s^8 + 1.8507e-009 s^7 + 1.8274e-005 s^6 + 0.15529 s^5 + 320.2651 s^4 + 140960 s^3 + 20000000.014 s^2

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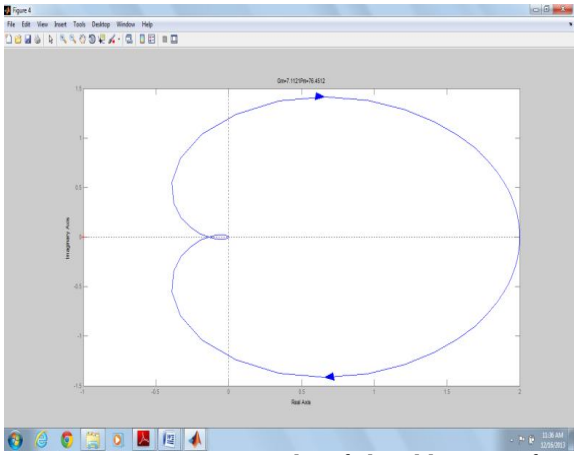

Fig .13 Nyquist plot of closed loop transfer function

VI. EXPERIMENTAL RESULTS

The proposed FPGA-based digital controller has been tested on a 200-W grid-tied microinverter whose parameters were given in Section IV.The test setup is shown in Fig. 14. The microinverter unit is fed from a PV simulator to generate the specific power curve at maximum power point. The output of the microinverter is connected to the ac grid through an isolation transformer. The conducted emission testing run according to CISPR16-1 test setup and using CISPR22 standard limits.

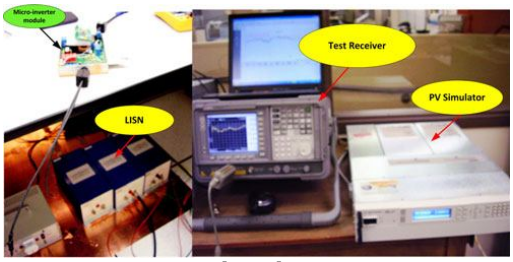

Fig. 14. Conducted emissions test setup.

Fig.

The first test was performed with the passive EMI filter designed into the dc–ac inverter. According to the results reflected in Fig. 15, an average peak of 35 dBμV across the spectrum (0.15–30 MHz) can be observed with the highest peak of 42 dBμV at 162 kHz

. The second round of testing was done without any filters in the microinverter unit, i.e., the passive EMI filter components were removed from the inverter unit. The resulting spectrum is shown in Fig. 16. An average peak of 50 dBμV can be seen across the frequency spectrum with the highest peak of 58 dBμV at around 1.8 MHz

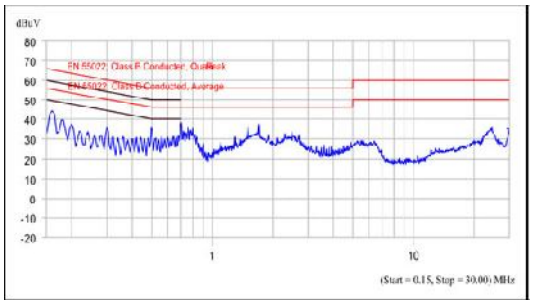

Fig. 15. Conducted emissions spectrum of the micro inverter with passive EMI filter..

This reflects the conducted EMI noise generated in the micro inverter that can be flown through the utility grid. The last measurement was conducted with the DAEF prototype connected to the ac side of the micro inverter unit with the passive EMI filter removed from the unit, in order to see the contribution of the proposed DAEF. The resulting EMC spectrum is depicted in Fig. 17. An average peak of 35 dBμV across the spectrum is obtained with the highest peak of 43 dBμV at 162 kHz is observed.

Fig. 16. Conducted emissions spectrum of the microinverter without EMI filters.

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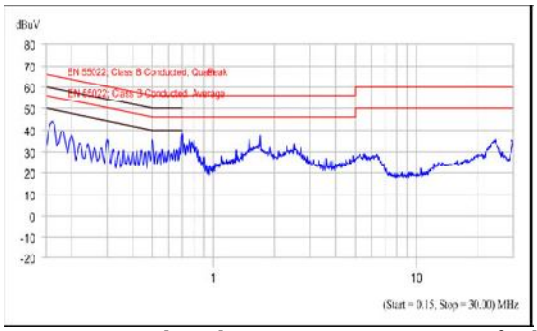

Fig. 17. Conducted emissions spectrum of the microinverter with DAEF installed.

As can be observed, in Figs. 15 and 17, the EMI attenuation performance of the DAEF prototype can match or outperform the one with the passive EMI filter. Furthermore, this confirms the viability of the proposed DAEF to replace the conventional passive EMI filter to save space and decrease the power losses in the inverter, therefore increasing the power efficiency of the microinverter.

VII. CONCLUSION

This paper proves the feasibility of replacing the conventional analog passive EMI filter by the DAEF in a solar grid-tied microinverter. In addition, the DAEF has been implemented concurrently with the inverter digital controller in an FPGA-based design. The TF of the micro inverter control system has been derived and analyzed using the *DQ* reference frame modeling technique. The stability of the micro inverter with the proposed digital controller has been verified and a compensator has been designed accordingly using the digital redesign approach. Compared with the conventional analog EMI suppression techniques, the size of the DAEF is not proportional to the power ratings of the converter; this means no bulky capacitor and oversized EMI choke need to be used. While providing matching or better EMI attenuation performance, significant reduction of the size, cost, and space of the overall power converter PCB can be achieved, hence further reducing power losses and increasing overall efficiency of the inverter.

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