

Performance Comparison for Different Configurations of SRAM Cells

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ABSTRACT: Memories are a core part of most of the electronic systems. Performance in terms of speed and power dissipation is the major areas of concern in today's memory technology. In this paper SRAM cells based on 6T, 7T, 8T, and 9T configurations are compared on the basis of performance for read and write operations. Studied results show that the power dissipation in 7T SRAM cell is least among other configurations because this structure uses a single bit for both read and write operations. This SRAM cell also provides the least power delay product among different studied SRAM configurations. Performance in terms of power dissipation and power delay product are least for 7T SRAM cell among the other SRAM configurations in 90nm CMOS technology.

KEYWORDS: SRAM, Power, Delay, Power delay product, Write, Read.

I. INTRODUCTION

The use of SRAM is expected to increase in future for both portable and high performance microprocessor. SRAM plays a critical role in modern microprocessor system, portable devices like PDA, cellular phones, and portable multimedia devices [1]. To achieve higher speed microprocessor, SRAM based cache memories are commonly used. The trend of scaling of device brings several challenges like power dissipation, sub threshold leakage, reverse diode leakage, and stability [2]. Nowadays research on very low threshold voltage and ultra-thin gate oxide are in progressive stage, due to reduction in the threshold voltage and the gate oxide thickness. The phenomena like intrinsic parameter fluctuation, random dopant fluctuation, oxides thickness fluctuation, and line edge roughness further degrade the stability of SRAM cells [3-5]. Large scale integration and fabrication process has resulted in increased density of devices by decreasing the device physical dimensions. Performance in terms of low power dissipation and high speed operation are the major challenges of integrated circuit design in deep submicron and nanoscale technologies. Designing high performance VLSI chip is becoming necessity for mobile communication and computing devices. Advances in battery technology have not taken place as fast as advances in the electronic devices and systems. So, designing electronic systems having high performance in terms of high speed and low power dissipation is a challenging task.

Low power and high speed circuit design differs from applications to applications. In case of battery operated portable systems, such as cellular phones and laptops, the overall goal of power minimization using low power circuit design is to keep the battery lifetime and weight reasonable. For high performance and non battery operated systems, such as workstations and multimedia digital signal processors, the overall goal of power minimization is to reduce the overall system cost (cooling, packaging and energy bill) while ensuring long term device reliability. These different requirements are the driving factors for low power and high speed electronic system design [6-7].

Paper is organized as follows. Different SRAM cell Configurations (6T, 7T, 8T, and 9T) are discussed in section II. Section III provides performance comparison in terms of power, delay, and power delay product for various types of SRAM configurations. Finally, conclusion is provided in section IV.

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II. RELATED WORK

Fig.1 shows a 6T SRAM cell [8]. This SRAM cell shows poor stability and has small hold and read static noise margins. In read operation, the stability decreases because of the voltage division between the access transistor and the driver transistor. The basic cell of 6T SRAM cell consists of six MOS transistors. This SRAM cell provides less read noise margin which further degrades due to process variation. To achieve higher read noise margin in 6T SRAM cell, width of pull down transistors has to be increased which eventually increases the issue of rise in leakage power dissipation [8]. This SRAM cell consumes more power and shows poor stability for small feature sizes with low voltage supply. During operation, the stability decreases due to the voltage division between the accesses and driver transistors.

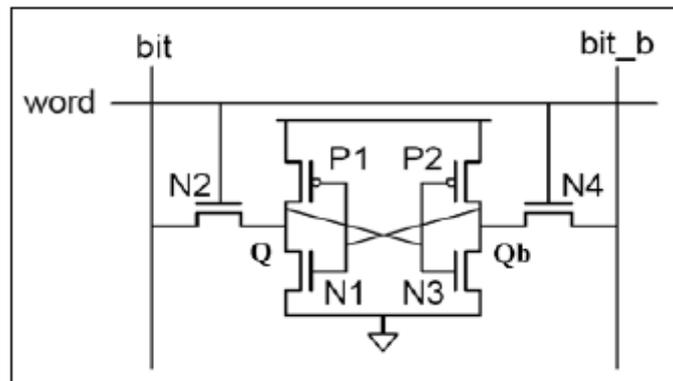


Fig. 1. A 6T SRAM cell

Figure shows a 7T SRAM cell [9]. The 7T SRAM cell has a good read stability and static noise margins. This cell has 7 transistors where only one bit line (BL), one word line (WL) and one read line (RL) is used. For writing into the memory cell, bit line (BL) and word line (WL) are used by keeping read line (RL) inactive. Similarly, for reading from memory cell, bit line (BL) and read line (RL) are used and word line is kept inactive [6]. 7T SRAM cell uses only one bit line, so power required for charging and discharging of one more bit line is reduced.

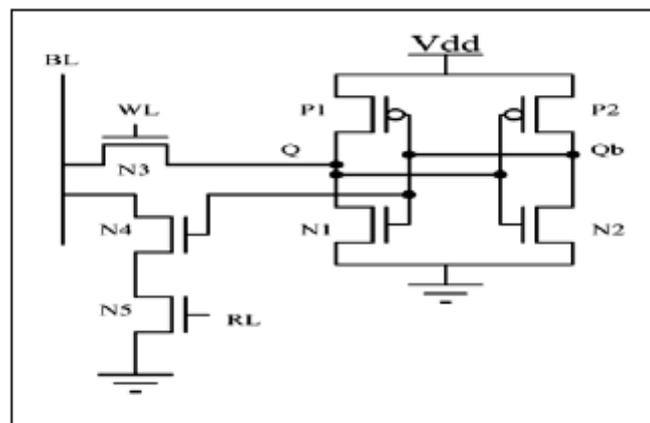


Fig. 2. A 7T SRAM cell

8T SRAM cell gives high noise margin but its write noise margin is very small. Therefore 8T SRAM is more prone to failure during write operation. Besides this its write time is higher and this cell occupies 30% more space than a conventional 6T SRAM cell [9]. 9T SRAM cell has high read noise margin, write noise margin and also has small write

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time. This SRAM cell is more prone to leakage. 8T SRAM and 9T SRAM cells provide higher read noise margin as compared to 6T SRAM cell. Literature survey reveals that higher performance in terms of power dissipation and power delay product can be achieved by using 7T SRAM cell.

III. PERFORMANCE COMPARISON OF DIFFERENT SRAM CELLS

The conventional 6T SRAM and studied 7T SRAM have been compared for the parameters: read delay, write delay, power dissipation, and power delay product in 90nm CMOS technology at $V_{DD} = 1.80V$. Table 1 shows the power dissipation for various operations in 6T and 7T SRAM cells [8]. Similarly, Table 2 shows delay for various operations in 6T and 7T SRAM cells [8].

Table 1. Power dissipation for various operations in 6T and 7T SRAM cells

| Operation | Power dissipation using 6T SRAM cell | Power dissipation using 7T SRAM cell |
|-----------|--------------------------------------|--------------------------------------|
| Read 0 | 8.26 μW | 7.11 μW |
| Read 1 | 8.52 μW | 6.70 μW |
| Write 0 | 9.35 μW | 7.29 μW |
| Write 1 | 9.35 μW | 7.73 μW |

Table 2. Delay for various operations in 6T and 7T SRAM cells

| SRAM operation | Delay using 6T SRAM cell | Delay using 7T SRAM cell |
|----------------|--------------------------|--------------------------|
| Read 0 | 25.50 ps | 35.00 ps |
| Read 1 | 22.50 ps | ≈ 0.00 ps |
| Write 0 | 72.80 ps | 85.70 ps |
| Write 1 | 104.10ps | 139.30 ps |

Table 3 shows the power delay product of different SRAM cells at $V_{DD} = 1.32V$ in 90nm CMOS technology [9]. In battery operated systems, there is a great demand to increase the life time of battery, while in high speed systems, speed is the major concern. For low power and high speed operations, designers have to concern on both speed and power dissipation [9]. For such type of system, power delay product is an important parameter. It is observed from Table 3 that 7T SRAM cell gives a lesser power delay product at 1.32V voltage supply in 90nm CMOS technology.

Table 3. Power delay product of different SRAM cells

| SRAM Cells | Power delay product at $V_{DD} = 1.32V$ |
|------------|---|
| 6T | 2.57e-12 Ws |
| 7T | 1.05 e-13 Ws |
| 8T | 1.05 e-13 Ws |
| 9T | 3.49 e-13 Ws |

IV. CONCLUSION

Different SRAM configurations: 6T, 7T, 8T, and 9T have been studied for their performance analysis. Literature survey reveals that 7T SRAM cell has the advantage of higher noise margin and smaller power dissipation in comparison with other discussed SRAM configurations. The studied results also show that this SRAM cell has the least power delay product among different SRAM configurations (6T, 7T, 8T, and 9T SRAM configurations) in 90nm CMOS technology.

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