Signal Flow Graph Realization of Higher-Order Current-Mode All Pole Low-Pass Filters Using Five Current Follower Transconductance Amplifiers (CFTAs)

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INTRODUCTION

The current Follower Transconductance Amplifier (CFTA) has been introduced in Biolek D [1]. This current input and output...
building block is particularly useful in realizing analog signal processing functions requiring explicit current outputs. The CFTA is slightly modified from the conventional Current Differencing Transconductance Amplifier (CDTA) [2] by replacing the current differencing unit with a current follower and complementing the circuit with a simple current mirror for copying the z-terminal current. CFTA is a composite of a CF usually realized from a translinear CCII, a Current Conveyor Transconductance Amplifier (CCTA) has directly a CCII followed by an OTA [3]. The CFTA element is a combination of the current follower and the multioutput operational transconductance amplifier. Consequently, there are several structures for realizing the current mode of active filters using CFTAs [4]. However, the work had been studied in the synthesis of the general nth-order all-pole lowpass transfer function. Also, the realization of an nth-order lowpass filter using current conveyors was introduced in Gunes EO [5] the circuit has too many grounded resistors, i.e. (n+1) current conveyors, n grounded resistors and n grounded capacitors. Therefore, this work largely focuses on presenting a general synthesis procedure for the realization of the Nth-Order all-pole low pass Transfer function. The approach is based on drawing a signal flow graph directly from the given transfer function and then obtaining, from the graph, the Active-C filter involving CFTAs. The resulting circuit uses a minimum number of n CFTAs and n grounded capacitors, which makes the circuit especially suitable for monolithic implementation. It is shown that the design procedure proposed here is general and simple. Simulation results from MATLAB Simulink illustrate the properties of the proposed design procedure.

In this present study, the recent work of Dike is extended to include the active building block Current Follower Transconductance Amplifier (CFTA) and its basic applications like amplifiers, grounded and floating inductors and active filters in analog signal processing. Designed examples and computer simulations by Matlab Simulink confirm the usefulness of the proposed approach. Its various instrumental applications are filter and conventional controllers (proportional, integral and derivative). These CFTA based conventional controllers are studied and their characteristics are analysed through computer simulation and verified in Matlab Simulink.

**Literature Review**

Bipolar and CMOS technologies are used for CFTA implementation. One of the CFTA realizations using bipolar technology is reported in Herencsár N [6]. The advantage of these circuits is high overall gain compared to CMOS based implementations. A high gain, these CFTA structures also produce high power dissipation due to the use of leakages in BJT. Another bipolar implementation which is an extension of CFTA known as ZC-CFTA is presented in Tangsrirat W [7]. In this structure, an extra z-terminal termed as z-copy is included to provide design flexibility. A Current-Controlled CFTA (CCCFTA) based on BJT technology is presented in Jaikla W [8]. In this structure, the input voltages of f-terminals is zero and therefore these terminals have a finite resistance that can be controlled through bias currents [9-11].

CMOS is also sometimes referred to as complementary-symmetry metal-oxide-semiconductor. The words “complementary-symmetry” refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type (PMOS) and n-type (NMOS) metal oxide semiconductor field-effect transistors (MOSFETs) for logic functions. CMOS technology-based CFTA structures has also been reported in the literature. One such structure is reported in Chauhan AS [11] which has an advantage of high impedance at the z-terminal. A low power CMOS realization of the CFTA is reported in Li YA [12]. In this structure, the input stages are constructed using VF, due to which this CFTA has very low input resistance. The modification of CFTA known as CC-CFTA is reported in Herencsár N [13] which has an advantage of better OTA gain and multiple outputs can be drawn out of CFTA. Another CMOS based CFTA is reported in Herencsár N [13]. This circuit exhibit very low impedance at the inputs and high (typically in GΩ). A comparison of available CFTA structures in terms of supply voltage, technology and number of transistors, gain, power dissipation, and terminal impedances is presented in Table 1.

**Table 1.** Bipolar realization of CFTA.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Technology</th>
<th>Supply voltage</th>
<th>Bias current</th>
<th>Transconductance gain</th>
<th>Power dissipation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tangsrirat et al.</td>
<td>Bipolar</td>
<td>± 3 V</td>
<td>100 μA</td>
<td>2 mS</td>
<td>-</td>
</tr>
<tr>
<td>Lahiri et al.</td>
<td>Bipolar</td>
<td>± 2.5 V</td>
<td>50 μA</td>
<td>0.96 mS</td>
<td>-</td>
</tr>
<tr>
<td>Jaikla et al.</td>
<td>Bipolar</td>
<td>± 1.5 V</td>
<td>100 μA</td>
<td>-</td>
<td>8.11 mW</td>
</tr>
<tr>
<td>Tangsrirat et al.</td>
<td>0.35 μCOMS</td>
<td>± 2.5 V</td>
<td>10 μA</td>
<td>-</td>
<td>0.43 mW</td>
</tr>
<tr>
<td>Herencsár et al.</td>
<td>0.5 μCOMS</td>
<td>± 1.85 V</td>
<td>400 μA</td>
<td>-</td>
<td>10.6 mW</td>
</tr>
<tr>
<td>Singh et al.</td>
<td>0.25 μCOMS</td>
<td>± 0.75 V</td>
<td>40 μA</td>
<td>-</td>
<td>0.6 mW</td>
</tr>
</tbody>
</table>

Bipolar-based CFTA circuit realization suitable for the monolithic IC fabrication is displayed in Figure 1.
Bipolar realization of the CFTA used in this work is shown in Figure 1. The circuit consists of a current conveyor circuit Q1-Q8 and operational transconductance amplifier Q9-Q20. Therefore, in this case, the transconductance gain $g_m = \frac{I_m}{2V_T}$ is directly proportional to the external bias current $I_B$, which can be written as where $V_T \approx 26$ mV at 27°C is the thermal voltage.

**CMOS Realization of CFTA**

CMOS-based CFTA circuit realization suitable for the monolithic IC fabrication is displayed in Figure 2. CMOS realization of the CFTA used in this work is shown in Figure 2. The circuit consists of a current conveyor circuit Q1-Q8 and operational transconductance amplifier Q9-Q20. Therefore, in this case, the transconductance gain of CMOS based 1th CFTA ($i=1,2,3$), can be controlled through the biasing current $I_{Bi}$ which can be written as $g_m = \sqrt{\beta_o C_{ox}}$ where $\beta_o = \mu C_{ox} \frac{W}{L}$ is the process parameter, is the free electron mobility in the channel, is the gate oxide capacitance per unit area, $W$ and $L$ are the channel width and length respectively.

**LITERATURE SURVEY**

In the past few decades, the current mode (CM) analog signal processing has received considerable interest owing to the advantages offered by CM techniques which have been elaborated. This has resulted in the emergence of various CM analog building blocks and CFTA is one among those. The CFTA block was first reported by Biolek D [2]. A Current Follower Transconductance
Amplifier (CFTA) can be considered to be a reduced version of the CDTA instead of the current-differencing unit as the front end, it has a current follower as the front end which can be easily implemented from a CCII+ by grounding its Y-terminal. The operation of the CCII current conveyor is such that if Current conveyor (CCII+) is constructed by a Voltage Follower (VF) between the Y-terminal and the X-terminal in order to accomplish \( v_x = v_y \), and a Current Mirror (CM) between the X-terminal and the Z-terminal in order to accomplish \( i_z = i_x \) \(^{14}\). The block diagram of the CFTA can be drawn as shown in Figure 3a. Thus, it is a four-terminal building block having one input terminal \( f \) and three outputs terminals \( Z, x^+ \) and \( x^- \). The output current entering into terminal \( Z \) is the same as the one entering into the low impedance terminal \( f \), whereas when terminal \( Z \) is terminated into an impedance, two complimentary output currents are available as \( i^+\) and \( i^-\) which are respectively given by \( i^+_x = g_m v_z \) and \( i^-_x = -g_m v_z \). A CC-based implementation of the CFTA is shown in Figure 3b which can also be considered to be a special case of the CDTA with input terminal \( n \) being grounded \(^{12}\).

**Figure 3.** CFTA realization (a): block diagram implementation; (b): Implementation of the CFTA using CCII and OTA.

**MATHEMATICAL MODEL**

This current input and output building block is particularly useful in realizing analog signal processing functions requiring explicit current outputs. The symbolic representation of the CFTA and its behavior model are shown in Figure 4. Assuming the standard notation, the terminal defining relations of this device can be characterized by the following set of equations \(^{14}\).

\[
V_f = 0, \quad i_z = i_f, \quad i_x = g_m v_Z = z_i Z_{Z} \]

where \( g_m \) is the transconductance gain of the CFTA and \( Z_z \) is an external impedance connected to the \( z \)-terminal. The CFTA consists essentially of the current follower at the input port and the multi-output transconductance amplifier at the output part. According to Biolek D \(^{13}\) and Figure 4, the \( f \)-terminal forms the current input terminal at ground potential \( (V_f = 0) \) and the output current at the \( z \)-terminal \( (i_z) \) follows the current \( (i_f) \) through the \( f \)-terminal. The voltage drop at the \( z \)-terminal \( (V_z) \) is then converted to a current at the \( x \)-terminal \( (i_x) \) by a \( g_m \)-parameter. In general, the \( g_m \)-value is adjustable over several decades by a supplied bias current/voltage, which lends electronic controllability to design circuit parameters. It is seen that the graph consists of two basic operations, which are current summation and current lossless integrator, as redraw in Figures 5b and 6c, respectively. In most of the applications, the \( z \)-terminal of a CFTA element connected by grounded load impedance \( Z \). Special Signal Flow Graphs (SFGs) can be used in such circuits for their analysis and synthesis; these are called “IVI” (Current-Voltage-Current) Signal Flow Graphs. Figure 3a shows the “IVI” SFG of the CFTA element. As shown in Figure 5b. SFG can be simplified by removing the intermediate voltage node. Using the current and voltage relations of the CFTA given in equation (1),

**Figure 4.** The CFTA.
We can easily find that these two sub-graphs also can be realized using CFTA by the sub-circuits shown in Figures 4b and 6a, respectively.

Using Kirchhoff’s current law (KCL), we get

\[ I_f + sCV_z = sC(V_z) \]

Where \( I_z = I_f \) and \( C \) is the capacitance of the CFTA-C circuit.

\[ I_z + sCV_z = \frac{sC}{g_m} \Rightarrow V_z = \frac{I_z}{sC} \Rightarrow I_z = I_z \left(1 - \frac{g_m}{sC}\right) = stI_z \]  \hspace{1cm} (1)

For the CFTA-based realization, it can readily obtain the CFTA-C circuit by interconnecting the corresponding sub-circuits of Figure 6a according to the overall signal flow representation of Figure 7. The CFTA-C circuit realizing any nth-order low-pass...
current transfer function is shown in Figure 7. For this realization, it has to be noted that the proposed filter configuration contains \( n \) CFTAs as active elements and \( n \) capacitors as passive elements for general \( n \)-th order filter function. Also, note that the circuit realization uses only grounded capacitors that are suitable for the integrated circuit point of view \([15]\) and also provides low-input impedance and high-output impedance terminals that are desirable for cascading in current-mode \([16,17]\). We can see that the low input impedance \( f \) terminal of each CFTA is connected to high output impedance \( \pm x \) terminals of other CFTA. Parasitic impedances are connected between true ground node \( f \) and virtually grounded node \( f \). Therefore, these are almost ineffective. As a result, The parasitic impedances of \( -x \) terminal of CFTA-1 at node 1, \( +x \) terminal of CFTA-1 at node 2, \( -x \) terminal of CFTA-2 at node 1, \( +x \) terminal of CFTA-2 at node 3 and \( -x \) terminal of CFTA-3 at node 1, \( +x \) terminal of CFTA-3 at node 4 and \( -x \) terminal of CFTA-4 at node 1, \( +x \) terminal of CFTA-4 at node 5 and \( -x \) terminal of CFTA-\( n \) at node 1, \( 1 +x \) terminal of CFTA-\( n \) at node \( n \) are almost ineffective. The only parasitic impedances for consideration are \( z_1, z_2, z_3, \ldots z_n \) across external capacitors \( C_1, C_2, C_3, C_4, \ldots C_n \) connected between high impedance \( z \) terminal and ground of CFTA-1, CFTA-2, CFTA-3, CFTA-4... and CFTA-\( n \).

**Figure 7.** CFTA-based realization of the \( n \)-order current-mode low-pass filter, corresponding to the SFG given in Figure 6.

The above expression can be represented by the signal flow graph (SFG) as shown in Figure 6.

![Figure 8](image)

**Figure 8.** Signal flow graph representing equation (2).

The corresponding set of equations are:

\[
I_1 = I_{in} - I_2 - I_3 - \ldots - I_7
\]

\[
I_2 = I_1 - \left(1 - \frac{s b_n}{b_{n-1}}\right) \Rightarrow I_2 \frac{s b_n}{b_{n-1}} = I_1
\]

\[
I_3 = I_2 - \left(1 - \frac{s b_n}{b_{n-1}}\right) \Rightarrow I_3 \frac{s b_n}{b_{n-1}} = I_2
\]

\[
I_4 = I_3 - \left(1 - \frac{s b_n}{b_{n-1}}\right) \Rightarrow I_4 \frac{s b_n}{b_{n-1}} = I_3
\]
\[
I_5 = I_4 = \left(1 - \frac{sb_n}{b_{n-1}}\right)I_6 \Rightarrow I_5 \frac{sb_n}{b_{n-1}} = I_4
\]

\[
I_6 = I_5 = \left(1 - \frac{sb_n}{b_{n-1}}\right)I_6 \Rightarrow I_6 \frac{sb_n}{b_{n-1}} = I_5
\]

\[
l_7 = l_5(1-sb_1) \Rightarrow l_7 sb_1 = l_6
\]

\[
l_{out} = l_7 \text{ and } l_{in} \text{ represent a source node, } l_{out} \text{ a sink node.}
\]

The denominator of a filter transfer function determines the poles and the fall-off rate of the frequency response. The denominator of the biquadratic function has the same form for all types of filters. The general form of an n-order lowpass current transfer function can be expressed by the following formula:

\[
\frac{I_o(s)}{I_in(s)} = \frac{1}{b_ns^n + b_{n-1}s^{n-1} + \ldots + b_2s^2 + b_1s + 1}
\]

From the realization of Figure 7, the design equations can be obtained by comparing Figure 5b with Figure 8. The results are summarized as follows:

\[
\frac{b_n}{b_{n-1}} = \frac{c_1}{g_{m1}}
\]

\[
\frac{b_{n-1}}{b_{n-2}} = \frac{c_2}{g_{m2}}
\]

\[
\ldots
\]

\[
\frac{b_2}{b_1} = \frac{c_{n-1}}{g_{m(n)}}
\]

\[
b_1 = \frac{c_n}{g_{m(n)}}
\]

It should be noted from the above expressions that the coefficients \(b_i (i=1,2,3,4,5 \ldots ,n)\) of the realized function can be tuned electronically by adjusting the \(g_m\) value of the CFTA.

**MATERIALS AND METHODS**

In the proposed circuit topologies in Figure 9, we can see that the low impedance f terminal of each CFTA is connected to high impedance ± x terminals of other CFTA. This use of current feedback minimizes or eliminates the possibilities of parasitic impedance effects of CFTAs to be considered. A practical CFTA, to any other element, includes various ports parasitic as shown in Figures 9-14.

### Third-Order Butterworth Low Pass Filter

Parasitic impedances are connected between true ground node f and virtually grounded node f. Therefore, these are almost ineffective. As a result, the parasitic impedances of -x terminal of CFTA-1 at node 1, +x terminal of CFTA-1 at node 2, -x terminal of CFTA-2 at node 1, +x terminal of CFTA-2 at node 3 and -x terminal of CFTA-3 at node 1 are almost ineffective. The only parasitic impedances for consideration are \(z_1\), \(z_2\), \(z_3\) and \(z_4\) across external capacitors \(C_1\), \(C_2\), and \(C_3\) connected between high impedance z terminal and ground of CFTA-1, CFTA-2, and CFTA-3.

### Fourth-Order Butterworth Low Pass Filter

Parasitic impedances are connected between true ground node f and virtually grounded node f. Therefore, these are almost ineffective. As a result, the parasitic impedances of -x terminal of CFTA-1 at node 1, +x terminal of CFTA-1 at node 2, -x terminal of CFTA-2 at node 1, +x terminal of CFTA-2 at node 3 and -x terminal of CFTA-3 at node 1 +x terminal of CFTA-3 at node 4 and -x terminal of CFTA-4 at node 1 are almost ineffective. The only parasitic impedances for consideration are \(z_1\), \(z_2\), \(z_3\) and \(z_4\) across external capacitors \(C_1\), \(C_2\), \(C_3\) and \(C_4\) connected between high impedance z terminal and ground of CFTA-1, CFTA-2, CFTA-3, and...
Fifth-Order Butterworth Low Pass Filter

Parasitic impedances are connected between true ground node f and virtually grounded node f. Therefore, these are almost ineffective. As a result, the parasitic impedances of -x terminal of CFTA-1 at node 1, +x terminal of CFTA-1 at node 2, -x terminal of CFTA-2 at node 1, +x terminal of CFTA-2 at node 3 and -x terminal of CFTA-3 at node 1 +x terminal of CFTA-3 at node 4 and -x terminal of CFTA-4 at node 1 +x terminal of CFTA-4 at node 5 and -x terminal of CFTA-5 at node 1 are almost ineffective. The only parasitic impedances for consideration are $z_1$, $z_2$, $z_3$, $z_4$ and $z_5$ across external capacitors $C_1$, $C_2$, $C_3$, $C_4$ and $C_5$ connected between high impedance z terminal and ground of CFTA-1, CFTA-2, CFTA-3, CFTA-4 and CFTA-5.

EXPLANATION OF LOW PASS FILTERS

Third-Order Butterworth Lowpass Filter

The third-order all-pole low-pass Butterworth current transfer function. It can easily show that this transfer function can be represented by the signal flow graph shown in Figure 9a, and the corresponding circuit realization of this graph is thus shown in Figure 9b.

Figure 9. Third-order low-pass transfer function of equation (4): (a): signal flow graph representation; (b): circuit realization.

Consider for Third-order all-pole low pass Butterworth current transfer function. The corresponding set of equations are:

\[ I_1 = I_{in} - I_2 - I_4 - I_6 \]
\[ I_2 = I_1 - (1-s^3b_3/b_2)I_2 \Rightarrow I_2s^3b_3/b_2 = I_1 \]
\[ I_3 = I_2 \]
\[ I_4 = I_3 - (1-s^2b_2/b_1)I_4 \Rightarrow I_4s^2b_2/b_1 = I_3 \]
\[ I_5 = I_4 \]
\[ I_6 = I_5(1-sb_1)I_6 \Rightarrow I_6sb_1 = I_5 \]
\[ I_{out} = I_6 \]

And $I_{in}$ represents a source node, $I_{out}$ a sink node.

The third-order low-pass transfer function is considered. Generally, the current transfer function of the normalized third-order Butterworth low-pass filter is defined as:

\[ \frac{I_o(s)}{I_{in}(s)} = \frac{1}{b_3s^3 + b_2s^2 + b_1s + 1} = \frac{1}{s^3 + 2s^2 + 2s + 1} \] (4)
Third Order Low Pass Filter of Course Simulink

CDTA-based circuit realization

In this case, the design equations of the circuit are found as:

\[
\frac{b_1}{b_2} = \frac{c_1}{g_{m1}} = \frac{1}{2}, \quad \frac{b_2}{b_1} = \frac{c_2}{g_{m2}} = 1, \quad \frac{b_3}{b_2} = \frac{c_3}{g_{m3}} = 2 \text{ and } b_0 = 1 \quad (5)
\]

Thus, the normalized component values are obtained as:

\[C_1 = C_2 = C_3 = 1F, \quad G_{m1} = \frac{2A}{V}, \quad G_{m2} = \frac{1A}{V}, \quad G_{m3} = \frac{1A}{V}.\]

Routine circuit analysis of Figure 6b yields the current transfer function as follows:

\[
\frac{I_m(s)}{I_{in}(s)} = \frac{g_{m1} g_{m2} g_{m3}}{C_1 C_2 C_3} \left( \frac{g_{m1} g_{m2}}{C_1} s^2 + \frac{g_{m1} g_{m3}}{C_2} s + \frac{g_{m2} g_{m3}}{C_3} \right)
\]

\[
(6)
\]

The active and passive sensitivities of the natural angular frequency (\(\omega\)) and quality factor (\(Q\)) are calculated using relations given in Soderstrand MA [18]. The results of active and passive sensitivity analysis of various parameters for the proposed filter are given in Table 2. It is clearly seen from Table 2 that all the sensitivities are low and within unity in magnitude. Thus, all the sensitivities are small.

### Table 2. Sensitivities for the circuit parameters in Figure 9.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>(g_{m1})</th>
<th>(g_{m2})</th>
<th>(g_{m3})</th>
<th>(c_1)</th>
<th>(c_2)</th>
<th>(c_3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(b_0)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
</tr>
<tr>
<td>(b_1)</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>-1</td>
<td>-1</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure 10. The state-space representation of the transfer function.

Figure 11. Model for third-order low-pass transfer function.
Fourth-Order Butterworth Lowpass Filter

Fourth-order all-pole low pass Butterworth current transfer function. It can easily show that this transfer function can be represented by the signal flow graph shown in Figure 12a and the corresponding circuit realization of this graph is thus shown in Figure 12b.

Consider for fourth-order all-pole low pass Butterworth current transfer function. The corresponding set of equations are:

\[ I_1 = I_{in} - I_2 - I_4 - I_6 - I_8 \]

\[ I_2 = I_1 - \left( \frac{1 - s^2 b_2}{b_2} \right) I_2 \Rightarrow I_2 \frac{s^2 b_2}{b_2} = I_1 \]

\[ I_3 = I_2 \]

\[ I_4 = I_3 - \left( \frac{1 - s^3 b_3}{b_3} \right) I_4 \Rightarrow I_4 \frac{s^3 b_3}{b_3} = I_3 \]

\[ I_5 = I_4 \]

\[ I_6 = I_5 - \left( \frac{1 - s^2 b_1}{b_1} \right) I_6 \Rightarrow I_6 \frac{s^2 b_1}{b_1} = I_5 \]

\[ I_7 = I_6 \]

\[ I_8 = I_7 \left( 1 - s \right) I_8 \Rightarrow I_8 \frac{b_2}{b_2} = I_7 \]

\[ I_{out} = I_8 \]

And \( I_{(in)} \) represents a source node, \( I_{out} \) a sink node.

![Signal Flow Graph](image1.png)

**Figure 12.** Fourth-order low-pass transfer function of equation (6), (a): signal flow graph representation; (b): circuit realization.

The fourth-order low-pass transfer function is considered. Generally, the current transfer function of the normalized fourth-order Butterworth low-pass filter is defined as

\[ \frac{I_o(s)}{I_{in}(s)} = \frac{1}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + 1} = \frac{1}{s^4 + 2s^3 + 3s^2 + 2s + 1} \]
Figure 13. The state-space representation of the transfer function.

Fourth Order Low Pass Filter of Course Simulink

In this case, the design equations of the circuit are found as:

\[
\frac{b_4}{b_3} = -\frac{c_1}{g_{m1}}, \quad \frac{b_3}{b_2} = -\frac{c_2}{g_{m2}}, \quad \frac{b_2}{b_1} = -\frac{c_3}{g_{m3}}, \quad b_o = \frac{C_4}{g_{m4}} = 2 \quad \text{and} \quad b_o = 1.
\]  

Thus, the normalized component values are obtained as \( C_1 = C_2 = C_3 = C_4 = 1F \), \( g_{m1} = 2A/V \), \( g_{m2} = \frac{3}{2}A/V \), \( g_{m3} = \frac{2}{3}A/V \) and \( g_{m4} = \sqrt{2}A/V \). Routine circuit analysis of Figure 8b yields the current transfer function as follows:

\[
\frac{I_o(s)}{I_{in}(s)} = \frac{g_{m1}g_{m2}g_{m3}g_{m4}}{C_1C_2C_3C_4} \frac{s^4}{s^4 + \left( \frac{g_{m1}}{C_1} \right)s^3 + \left( \frac{g_{m1}g_{m2}}{C_1C_2} \right)s^2 + \left( \frac{g_{m1}g_{m2}g_{m3}}{C_1C_2C_3} \right)s + \left( \frac{g_{m1}g_{m2}g_{m3}g_{m4}}{C_1C_2C_3C_4} \right)}
\]

Fifth-Order Butterworth Lowpass Filter

Fifth-order all-pole low pass Butterworth current transfer function. It can easily show that this transfer function can be represented by the signal flow graph shown in Figure 15a, and the corresponding circuit realization of this graph is thus shown in Figure 15b.
Consider for fifth-order all-pole low pass Butterworth current transfer function. The corresponding set of equations are:

\[ I_1 = I_{in} - I_2 - I_4 - I_6 - I_8 - I_{10} \]

\[ I_2 = I_1 - \left( \frac{1 - s^2 b_3}{b_4} \right) I_2 \Rightarrow I_2 \frac{s^2 b_3}{b_4} = I_1 \]

\[ I_3 = I_2 \]

\[ I_4 = I_3 - \left( \frac{1 - s^3 b_2}{b_3} \right) I_4 \Rightarrow I_4 \frac{s^3 b_2}{b_3} = I_3 \]

\[ I_5 = I_4 \]

\[ I_6 = I_5 - \left( \frac{1 - s^2 b_1}{b_2} \right) I_6 \Rightarrow I_6 \frac{s^2 b_1}{b_2} = I_5 \]

\[ I_7 = I_6 \]

\[ I_8 = I_7 - \left( \frac{1 - s^2 b_1}{b_1} \right) I_8 \Rightarrow I_8 s b_1 = I_7 \]

\[ I_9 = I_8 \]

\[ I_{10} = I_9 - (1 - s b_1) I_{10} \Rightarrow I_{10} s b_1 = I_9 \]

\[ I_{out} = I_{10} \]

And \( I_{in} \) represents a source node, \( I_{out} \) a sink node.

The fifth-order low-pass transfer function is considered. Generally, the current transfer function of the normalized fifth-order Butterworth low-pass filter is defined as

\[
\frac{I_o(s)}{I_{in}(s)} = \frac{1}{b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + 1} = \frac{1}{s^5 + 3s^4 + 5s^3 + 5s^2 + 3s + 1}
\]  

(11)
In this case, the design equations of the circuit are found as:
\[
g_{m_1} = 2A/V, \quad g_{m_2} = \frac{3}{2} A/V, \quad g_{m_3} = \frac{2}{3} A/V, \quad g_{m_4} = \frac{1}{2} A/V, \quad b_0 = 1.
\]

thus, the normalized component values are obtained as:
\[
C_1 = C_2 = C_3 = C_4 = C_5 = 1F,
\]

yields the current transfer function as follows:
\[
\frac{I_o(s)}{I_i(s)} = \frac{g_{m_1}g_{m_2}g_{m_3}g_{m_4}g_{m_5}}{C_1C_2C_3C_4C_5}
\]

From (10) and (13), the coefficient sensitivities to active and passive components are 1 or 0. Also, the active and passive sensitivities of the natural angular frequency and quality factor are calculated and found as 1 or 0 [18]. Thus, all the sensitivities are small.

The workability of the proposed circuits was tested and verified in MATLAB Simulink using 0.35 µm CMOS process parameters provided by MOSIS (AGILENT) and the Bipolar parameters for NR100N (NPN) and PR100N (PNP) as listed in Table 3.
\[ g_{\text{m}} = \frac{I_o}{2V_T} \text{ and } V_T \approx 26 \text{ mV at } 27^\circ \text{C.} \]

As an example, the illustrative current-mode third, fourth and fifth order all-pass filter of Figures 9-17 was designed with \( \omega_0=106 \text{ rad/sec.} \) For this purpose, the denormalized component values were chosen as \( C_1=C_2=C_3=C_4=C_5=1 \text{nF}. \)

### First-Order

\[ g_{m1}=2\text{mAV/V (}I_{01}\approx 104 \text{ μA)}, g_{m2}=1\text{mAV/V (}I_{02}\approx 52 \text{ μA)}, \text{and } g_{m3}=1/2 \text{mAV/V (}I_{03}\approx 26 \text{ μA).} \]

### Second-Order

\[ g_{m1}=2\text{mAV/V (}I_{01}\approx 104 \text{ μA)}, g_{m2}=3/2 \text{mAV/V (}I_{02}\approx 78 \text{ μA)}, \text{and } g_{m3}=2/3 \text{mAV/V (}I_{03}\approx 35 \text{ μA)}, \text{and } g_{m4}=1/2 \text{mAV/V (}I_{04}\approx 26 \text{ μA).} \]

### Third-Order

\[ g_{m1}=3\text{mAV/V (}I_{01}\approx 156 \text{ μA)}, g_{m2}=5/3 \text{mAV/V (}I_{02}\approx 87 \text{ μA)}, \text{and } g_{m3}=1 \text{mAV/V (}I_{03}\approx 52 \text{ μA)}, g_{m4}=3/5 \text{mAV/V (}I_{04}\approx 31.2 \text{ μA)}, \text{and } g_{m5}=1/3 \text{mAV/V (}I_{05}\approx 17.3 \text{ μA)} \]

### Table 3. Bipolar and CMOS process parameters.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Process Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>NR100N</td>
<td>IS=121E-18, BF=137.5, VAF=159.4, IKF=6.974E-3, ISE=36E-16, NE=1.713, BR=0.7258, VAR=10.73, IKR=2.198E-3, RE=1, RB=524.6, RRM=25, RC=50, CJE=0.214E12, VIE=0.5, MJ=0.28, CJC=0.983E-13, VJC=0.5, MJC=0.3, XCJ=0.034, CJS=0.913E-12, VIS=0.64, MJ=0.4, FC=0.5, TF=0.425E-8, TR=0.5E-8, EG=1.206, XTB=1.538, XTI=2.0</td>
</tr>
<tr>
<td>PR100N</td>
<td>IS=73.5E-18, BF=110, VAF=51.8, IKF=2.359E-3, ISE=25.1E-16, NE=1.650, BR=0.4745, VAR=9.96, IKR=6.478E-3, RE=3, RB=327, RRM=24.55, RC=50, CJE=0.18E12, VIE=0.5, MJ=0.28, CJC=0.16E12, VJC=0.8, MJC=0.4, XCJ=0.037, CJS=1.03E-12, VIS=0.55, MJ=0.35, FC=0.5, TF=0.610E-9, TR=0.610E-8, EG=1.206, XTB=1.866, XTI=1.7</td>
</tr>
</tbody>
</table>

**Figure 18.** Bipolar implementation of the CFTA used for simulations.

The power supply rail voltages and bias currents were respectively selected as: \( \pm V=1.85 \text{ V and } I_B=400 \text{ μA).} \) In this case, the transconductance gain \( (g_{m}) \) of the CFTA is CMOS based 1th CFTA \( (i=1,2,3) \), and can be controlled through the biasing current \( I_B \) which can also be written by

\[ g_{m}=\sqrt{\beta I_B}, \text{ where } \beta = \mu C_{ox} \frac{W}{L} \]

is the process parameter, \( \mu \) is the free electron mobility in the channel, \( C_{ox} \) is the gate oxide capacitance per unit area, \( W \) and \( L \) are the channel width and length respectively. For the parameters \( \beta = \mu C_{ox} \frac{W}{L} \) and \( \beta = \mu C_{ox} \frac{W}{L} \), and \( \beta = \mu C_{ox} \frac{W}{L} \), \( \beta = \mu C_{ox} \frac{W}{L} \)

For 0.5 μm CMOS process used in this case, \( KP=(\mu C_{ox})_{P MOS} \) and \( KP=(\mu C_{ox})_{N MOS} \) were given. Therefore, the aspect ratios of MOS Transistors for CFTA and the dimensions of MOS transistors were used as specified in Table 4.
Table 4. Transistor dimensions of CMOS implemented CFTA.

<table>
<thead>
<tr>
<th>NMOS transistor</th>
<th>Dimensions W (μm)/L(μm)</th>
<th>PMOS transistor</th>
<th>Dimensions W (μm)/L(μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M3, M4, M7, M8</td>
<td>1.0/1.0</td>
<td>M1, M2, M5, M6</td>
<td>3.1/1.0</td>
</tr>
<tr>
<td>M10, M12, M13, M14, M15, M20</td>
<td>1.0/1.0</td>
<td>M9, M11, M16, M17, M18, M19</td>
<td>3.1/1.0</td>
</tr>
</tbody>
</table>

As an example, the illustrative current-mode third, fourth and fifth-order all-pass filter of Figures 9-17 were designed with $\omega_0 = 106$ rad/sec. For this purpose, the denormalized component values were chosen as

**Fourth-Order**

$g_{m1} = 147.3 \mu A/V (I_{01} \cong 104 \mu A)$, $g_{m2} = 104.6 \mu A/V (I_{02} \cong 52 \mu A)$, and $g_{m3} = 73.65 \mu A/V (I_{03} \cong 26 \mu A)$. $C_1 = 73.65\text{pF}$, $C_2 = 104.6\text{pF}$, and $C_3 = 147.3\text{pF}$.

**Fifth-Order**

$g_{m1} = 147.3 \mu A/V (I_{01} \cong 104 \mu A)$, $g_{m2} = 127.6 \mu A/V (I_{02} \cong 78 \mu A)$, and $g_{m3} = 85.45 \mu A/V (I_{03} \cong 35\mu A)$, and $g_{m4} = 73.65 \mu A/V (I_{04} \cong 26\mu A)$. $C_1 = 73.65\text{pF}$, $C_2 = 85.07\text{pF}$, $C_3 = 128.72\text{pF}$, and $C_4 = 147.3\text{pF}$.

**Sixth-Order**

$g_{m1} = 180.41 \mu A/V (I_{01} \cong 156 \mu A)$, $g_{m2} = 134.7 \mu A/V (I_{02} \cong 87 \mu A)$, and $g_{m3} = 104.16 \mu A/V (I_{03} \cong 52 \mu A)$, $g_{m4} = 80.7 \mu A/V (I_{04} \cong 31.2\mu A)$, $g_{m5} = 60.18 \mu A/V (I_{05} \cong 17.3\mu A)$, $C_1 = 36.14\text{pF}$, $C_2 = 80.8\text{pF}$, $C_3 = 104.16\text{pF}$, $C_4 = 134.5\text{pF}$ and $C_5 = 180.23\text{pF}$.

![Figure 19](image1.png)

**Figure 19.** CMOS implementation of the CFTA used for simulations.

The simulated third, fourth and fifth-order all-pole low pass circuits with the theoretical values are shown in **Figure 20**, which is obtained by applying a sinusoidal input of bias currents at 159 kHz.

![Figure 20](image2.png)

**Figure 20.** Simulated third, fourth and fifth-order all-pole low pass circuits.
Ideal gain and phase responses of the third, fourth and fifth-order all-pole low pass filter responses compared with the theoretical values are shown in Figure 21.

![Figure 21](image)

**Figure 21.** Gain and phase responses of the third, fourth and fifth-order all-pole low pass filter.

The time-domain analysis of third-order all-pole low pass filter is also shown in Figure 22, which is obtained by applying a sinusoidal input of 150 μA peak to peak at 0.159 Hz.

![Figure 22](image)

**Figure 22.** Time-domain response of proposed third-order all-pole low pass filter with respect to sinusoidal current output/input signal.

The time-domain analysis of the fourth-order all-pole low pass filter is also shown in Figure 23, which is obtained by applying a sinusoidal input of 40 μA peak at 0.159 Hz.

![Figure 23](image)

**Figure 23.** Time domain response of proposed fourth-order all-pole low pass filter with respect to sinusoidal current output/input signal.

The time-domain analysis of the fifth order all-pole low pass filter is also shown in Figure 24 which is obtained by applying a sinusoidal input of 10 μA peak at 0.159 Hz.

![Figure 24](image)

**Figure 24.** Time-domain response of proposed fifth-order all-pole low pass filter with respect to sinusoidal current output/input signal.

The THDs of the proposed fifth-order all-pole low pass filter can also be verified by applying multi-tones to the filters at the bias current equal to 100 μA at a constant frequency of 159 kHz. From Figure 25, it appears that the cut of band tones has been removed and only the in-band tones can be obtained at the output.

![Figure 25](image)
Figure 25. The THDs of the proposed fifth-order all-pole low pass filter.

The comparison between the proposed third-order Butterworth low pass filter, fourth-order Butterworth low pass filter and fifth-order Butterworth low pass filter is expressed in Table 5.

Table 5. Fourth-order Butterworth low pass filter and fifth-order Butterworth low pass filter.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Active Element</td>
<td>3</td>
<td>4 CFTA</td>
<td>5 CFTA</td>
<td></td>
</tr>
<tr>
<td>Number of Passive Element</td>
<td>C₁=C₂=C₃=1nF</td>
<td>C₁=C₂=C₃=1nF</td>
<td>C₁=C₂=C₃=1nF</td>
<td></td>
</tr>
<tr>
<td>Tunability of Q and W₀</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>Low active-passive sensitivity</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>Power Supply Rails(CMOS)</td>
<td>± V=0.75 V</td>
<td>± V=0.75 V</td>
<td>± V=0.75 V</td>
<td></td>
</tr>
<tr>
<td>Supply voltage (Bipolar)</td>
<td>± V=3 V</td>
<td>± V=3 V</td>
<td>± V=3 V</td>
<td></td>
</tr>
<tr>
<td>Designed pole frequency</td>
<td>159 KHz</td>
<td>159 KHz</td>
<td>159 KHz</td>
<td></td>
</tr>
<tr>
<td>Type of dependence on the bias current</td>
<td>non-linear</td>
<td>non-linear</td>
<td>non-linear</td>
<td></td>
</tr>
<tr>
<td>Matching condition required</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
<td></td>
</tr>
<tr>
<td>Power consumed</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td></td>
</tr>
</tbody>
</table>

CONCLUSION

In this paper, a Signal flow graph to synthesize the general, all-pole low pass current transfer function by an active-C circuit using the SFG representation of any nth-order all-pole low pass circuit requires only n CFTAs and n grounded capacitors. Third-order Butterworth low pass circuit require only three CFTAs and three grounded capacitors, fourth-order Butterworth low pass circuit require only four CFTAs and four grounded capacitors and fifth-order Butterworth low pass circuit require only five CFTAs and five grounded capacitors. The approach is based on drawing a signal flow graph directly from the graph of Active-C filter involving CFTA. It has been shown that the resulting structures are canonical in the number of active components n CFTAs for realizations, making them especially suitable for integration. The circuits also have low sensitivity characteristics and exhibit electronic controllability coefficients via transconductance gains gm of CFTAs. The simulation results from MATLAB Simulink are in excellent agreement with theoretical assumptions. However, a slight deviation may arise due to the parasitic involved. The circuit is operated at a supply voltage of ± 3 V, power supply rails of ± 1.85 V, and power dissipation of 10.6 mW, which are attractive for battery-operated portable electronic gadgets and mobile communication systems. The use of CFTAs as active elements in the filter design, in which there is the availability of high impedance explicit output terminals for proper impedance matching and no external buffers will be needed to draw the current-mode responses. High impedance explicit outputs are also suitable for direct cascading to implement higher-order current mode all-pole low pass filters using CFTAs.

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REFERENCES