ISSN (Online) : 2319 – 8753
ISSN (Print) : 2347 - 6710

International Journal of Innovative Research in Science, Engineering and Technology

An ISO 3297: 2007 Certified Organization, Volume 3, Special Issue 1, February 2014

International Conference on Engineering Technology and Science-(ICETS'14)
On 10th & 11th February Organized by

Department of CIVIL, CSE, ECE, EEE, MECHNICAL Engg. and S&H of Muthayammal College of Engineering, Rasipuram, Tamilnadu, India

Transistor Clamped Cascaded H-Bridge Multilevel Inverter Fed Induction Motor Drive

M. Manoj Kumar[1], N.Karthini[2], M.Revathy[3]

P.G Scholar, Sri Subramanya College of Engg & Tech, Palani, Tamilnadu, India[1, 2]

Assistant professor, Sri Subramanya College of Engg & Tech, Palani, Tamilnadu, India. [3]

Abstract — This paper presents a three phase twenty five level transistor clamped H-bridge (TCHB) based cascaded multilevel inverter for induction motor drive system. A Multicarrier phase disposition (PD) method is used to achieve minimum total harmonics distortion (THD) in the output voltage of multilevel inverters. The analysis of the output voltage harmonics are carried out and compared with the 25 level conventional cascaded H-bridge inverters. The proposed system is verified through simulation and the simulation results are compared with the conventional inverter. From the result the proposed inverter offers much less total harmonic distortion.

Index Terms— Cascaded H-bridge, cascaded neutral-point clamped inverter, five-level inverter, multicarrier phase-shifted pulse-width modulation (CPS-PWM), multilevel inverter, transistor-clamped converter.

I. INTRODUCTION

The concept of multilevel converters is finding increased attention in industry and academia as one of the preferred choices of electronic power conversion for high-power applications. They can provide an efficient alternative to high power applications, providing a high quality output voltage, increasing the efficiency and robustness, and reducing the electromagnetic interference The multilevel inverter has been implemented in various applications ranging from medium to high-power levels, such as motor drives [1], power conditioning devices [2] also conventional or renewable energy generation and distribution [3]. There are three major multilevel voltage source inverters topologies, namely neutral-point-clamped (NPC) or the diode-clamped inverter [4], cascaded multilevel [5], and flying capacitor (capacitor clamped) [6]. There are also topologies that have been introduced and have successfully found various industrial applications. Modulation strategies applied to multilevel inverters are selective harmonics elimination carrier-based pulse-width modulation (PWM), space vector modulation (SVM), and staircase or fundamental frequency modulation.

Now a days, many publications have addressed multilevel inverter technology and stressed the growing importance of multilevel inverters for high-power applications [7].

This paper focuses on the transistor clamped H-bridge based multilevel inverter topology. Generally, among these topologies, the cascaded multilevel inverter has the possible to be the most reliable and achieve the best fault tolerance owing to its modularity; a feature that enables the inverter to continue operating at lower power levels after cell failure [8]. Modularity also permits the cascaded multilevel inverter to be stacked easily for high-power and high-voltage applications.

The cascaded multilevel inverter typically comprises several identical single phase H-bridge cells cascaded in series at its output side. This configuration is commonly referred to as a cascaded H-bridge (CHB), which can be classified as symmetrical if the dc bus voltages are equal in all the series power cells, or as asymmetrical if otherwise. In an asymmetrical CHB, dc voltages are varied to produce more output levels [9]. Consequently, inverter design becomes more complicated as each power cell has to be sized accordingly to the different power levels, comprising isolated dc sources. This makes symmetrical CHB modularity beneficial over asymmetrical with regard to maintenance and cost.

For the symmetrical cascaded inverter, voltage level increase is possible without varying dc voltage with the same number of power cells, as proposed by this paper. Recently, the transistor clamped converter topology has received increased attention as it provides a simpler approach to increase output levels by taking different voltage levels from the series stacked capacitors [10]. In this paper, the proposed new configuration uses a five-level transistor-clamped H-bridge (TCHB) as a power cell that can produce a five-level output instead of three-level as

ISSN (Online) : 2319 – 8753
ISSN (Print) : 2347 - 6710

International Journal of Innovative Research in Science, Engineering and Technology

An ISO 3297: 2007 Certified Organization, Volume 3, Special Issue 1, February 2014

International Conference on Engineering Technology and Science-(ICETS'14)

On 10th & 11th February Organized by

Department of CIVIL, CSE, ECE, EEE, MECHNICAL Engg. and S&H of Muthayammal College of Engineering, Rasipuram, Tamilnadu, India

with the conventional H-bridge [11]. A similar arrangement using a NPC in each power cell has been presented [12]. However, an excessive number of power switches and diodes are required. In [13], though the number of switches for each cell is lower, and to achieve the same output quality, more cells are required, which increases the number of isolated dc sources, and bulky transformers.

II. TRANSISTOR CLAMPED TOPOLOGY

Recently, the transistor clamped converter topology has received increased attention as it provides a simpler approach to increase output levels by taking different voltage levels from the series stacked capacitors.

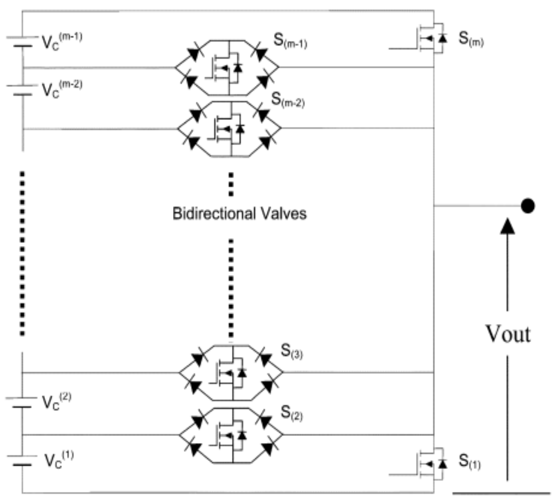

Fig. 1. The m-level transistor-clamped inverter.

A. Transistor-Clamped Inverter

The transistor-clamped inverter has the advantage of requiring the same number of power transistors as the levels generated, and therefore, the semiconductors are reduced by half with respect to the previous topologies. A 51-level converter requires 51 transistors (instead of 100 transistors). Fig. 1 shows the circuit topology of a m-level transistor clamped inverter, which fulfills

$$T = m \quad (1)$$

In this topology, the control of the gates is very simple because only one power transistor is switched-on at a time. Then, there is a direct relation between the output voltage, V_{out}, and the transistor that has to be turned-on. However, and despite the excellent characteristics of this topology, the number of transistors is still too large to allow the implementation of a practical converter with more than 50 levels.

B. TCC

The TCC concept is very similar to that of the DCC and was first introduced in 1977 [14]. Instead of clamping the connection points between switches and the capacitors through diodes, it is done by bidirectional switches. This gives a controllable path for the currents through the clamping devices, like with the ANPC. In [15], a bidirectional switch using four diodes and one transistor is presented, and the topology is explored Fig. 2. Three-phase three-level TCC. from three to several levels. In [16], a three-level version with a bidirectional switch based on two antiseries-connected IGBTs is proposed. Since the three-level case has a neutral point, just like the NPC, and it is fully controllable, this topology is also known as neutral point piloted (NPP) converter, and can be seen in Fig. 2. Note that two switches in series are necessary in the upper and lower parts of the converter leg to reach medium voltage. The two central IGBTs form the bidirectional switch, which, when switched on, generates the zero voltage level.

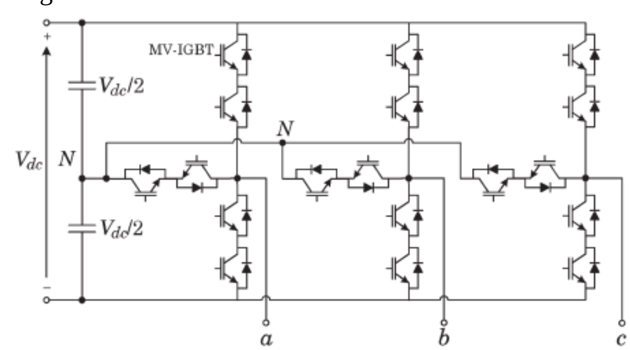

Fig. 2. Three- phase three-level TCC.

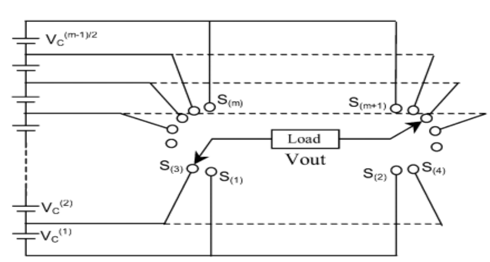

Fig. 3. The m-level inverter using an "H" bridge.

ISSN (Online) : 2319 – 8753
ISSN (Print) : 2347 - 6710

International Journal of Innovative Research in Science, Engineering and Technology

An ISO 3297: 2007 Certified Organization, Volume 3, Special Issue 1, February 2014

International Conference on Engineering Technology and Science-(ICETS'14)
On 10th & 11th February Organized by

Department of CIVIL, CSE, ECE, EEE, MECHNICAL Engg. and S&H of Muthayammal College of Engineering, Rasipuram, Tamilnadu, India

This topology has found industrial application [17] and is aimed for medium voltage (3.3, 6.6, and 9.9 kV) and high power up to 48 MW. The losses shared by the devices enable to switch at higher switching frequencies, which can efficiently increase the determined output frequency. Hence, this inverter can be meeting for variable high-speed areas, such as traction applications.

C. TCC Using H-Bridge

One solution for increasing the number of steps could be the use of "H" converters, like the one shown in Fig. 3, which consists of connecting two of the previously discussed topologies in series (two legs). If transistor-clamped inverters are used to build an "H" inverter, the number of transistors essential for an m-level inverter is m+1, which means only one more transistor than what is required for a simple leg configuration. However, the number of dc sources is reduced to 50%, which is the most important advantage of "H" converters.

Another characteristic is that the "H" topology has many redundant combinations of switches' positions to produce the same voltage levels. As an example, the level "zero" can be generated with switches in position S(1) and S(2), or S(3) and
S(4), or S(5) and S(6), and so on. Another characteristic of "H" converters is that they only produce an odd number of levels, which ensures the presence of the "0-V" level at the load. For example, a 51-level inverter using an "H" configuration with transistor-clamped topology involves 52 transistors, but only 25 power supplies as a replacement for the 50 required when using a single leg. Therefore, the problem related to increasing the number of levels and reducing the size and complexity has been moderately solved, since power supplies have been compact to 50%.

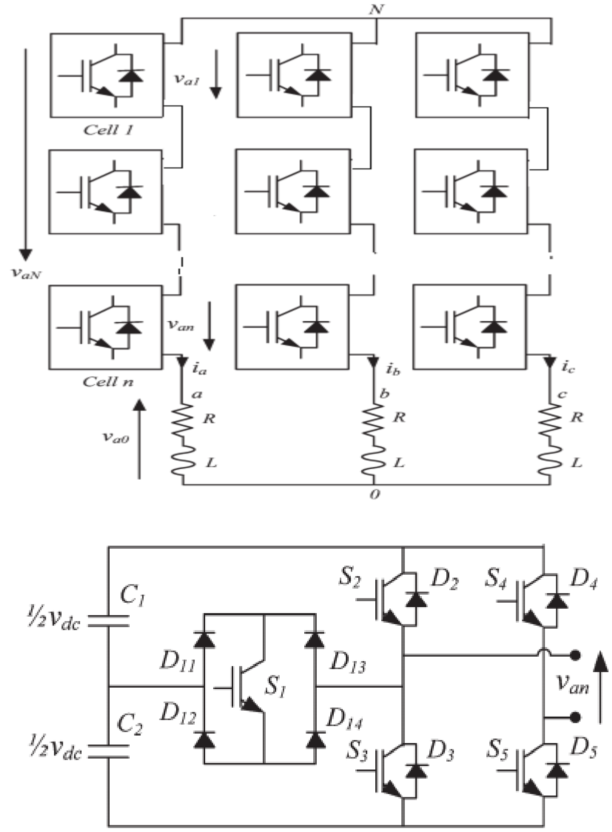

Fig. 4. TCHB: (a) general configuration of the proposed three-phase cascaded multilevel inverter and (b) topology of five-level transistor-clamped H-bridge for each cell.

III. PROPOSED INVERTER

Fig. 4(a) is the general configuration of the proposed inverter, comprising N_C series-connected five-level TCHB cells. Fig. 4(b) shows the cell with the additional one bidirectional switch connected between the first leg of the H-bridge and the capacitor midpoint, enabling five output voltage levels ($\pm v_{dc}, \pm(1/2)v_{dc}, 0$) to be produced based on the switch combinations given in Table I. The number of power cells required depends mainly on the operating voltage and production cost. In this case, a two-cell configuration is sufficient to produce a high-quality output with up to 17-voltage levels.

In general, the maximum levels in the phase and line voltages of the proposed inverter, based on NC cells, are given by the following equations:

$$n_p = 4N_C + 1 \quad (2)$$

ISSN (Online) : 2319 – 8753
ISSN (Print) : 2347 - 6710

International Journal of Innovative Research in Science, Engineering and Technology

An ISO 3297: 2007 Certified Organization, Volume 3, Special Issue 1, February 2014

International Conference on Engineering Technology and Science-(ICETS'14)
On 10th & 11th February Organized by

Department of CIVIL, CSE, ECE, EEE, MECHNICAL Engg. and S&H of Muthayammal College of Engineering, Rasipuram, Tamilnadu, India

$$n_l = 8N_C + 1 \quad (3)$$

Based on valid switch combinations, $S_1 - S_5$ in Table I, the cell output voltage Van can be represented by

$$V_{an} = V_{dc}(S_{5n} - S_{4n})\{(1/2)S_{1n} + |S_{2n} - S_{4n}|.|S_{3n} - S_{5n}|\} \quad (4)$$

Summation of all the power cell voltages gives the phase-to neutral voltage, V_{aN} and line voltage V_{ab}, respectively, as

$$V_{aN} = \sum_{n=1}^{Nc} V_{an} \quad (5)$$

$$V_{ab} = V_{aN} - V_{bN} \quad (6)$$

TABLE I
FIVE-LEVEL TRANSISTOR-CLAMPED H-BRIDGE OUTPUT VOLTAGE

S1	S2	S3	S4	S5	Van
0	1	0	0	1	Vdc
1	0	0	0	1	0.5 Vdc
0	0 or 1	1 or 0	0 or 1	1 or 0	0
1	0	0	1	0	-0.5 Vdc
0	0	1	1	0	-Vdc

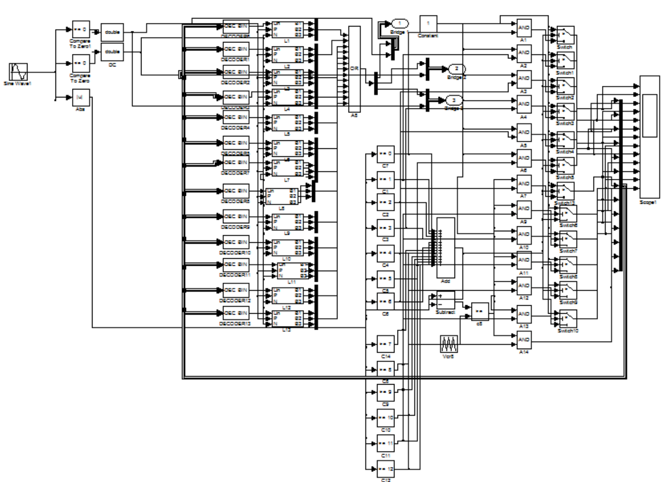

Fig. 5. PWM signal generation with multicarrier phase-disposition modulation.

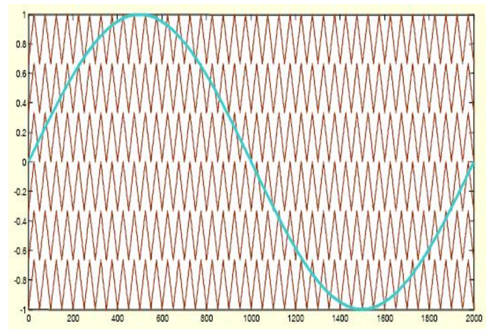

Fig .6. phase disposition PWM.

IV. MODULATION TECHNIQUE

A Phase disposition (PDPWM) modulation technique was introduced to generate the PWM switching signals in the proposed system. This technique involves, for m-level inverter the number of carriers (m-l) which are all in phase accordingly.

In 7 -level inverter all the six carrier waves are in phase with each other and compared with reference signal [18]. According to that, the gate pulses are generated and are associated to each switching devices. The phase disposition modulation technique is demonstrated in Fig.6

The simulation diagram of a PWM generation circuit is shown in fig.5.

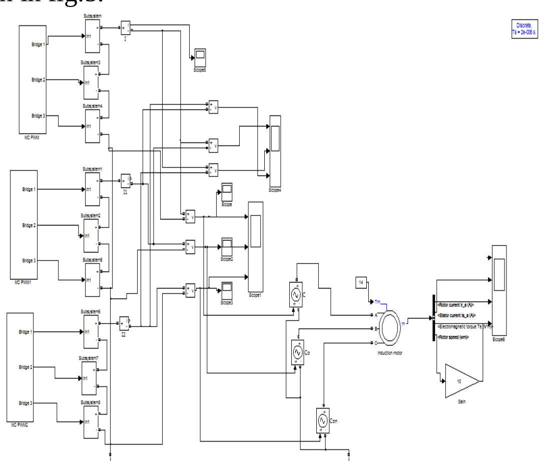

Fig .7.Simulation diagram of 25-level transistor clamped H-bridge (TCHB) cascaded multilevel inverter.

ISSN (Online) : 2319 – 8753
ISSN (Print) : 2347 - 6710

International Journal of Innovative Research in Science, Engineering and Technology

An ISO 3297: 2007 Certified Organization, Volume 3, Special Issue 1, February 2014

International Conference on Engineering Technology and Science-(ICETS'14)
On 10th & 11th February Organized by

Department of CIVIL, CSE, ECE, EEE, MECHNICAL Engg. and S&H of Muthayammal College of Engineering, Rasipuram, Tamilnadu, India

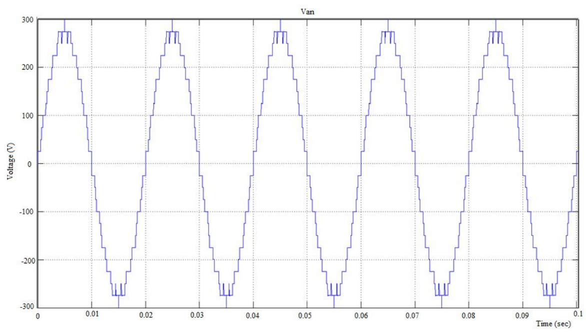

Fig. 8.Phase voltage (V_{an}) diagram

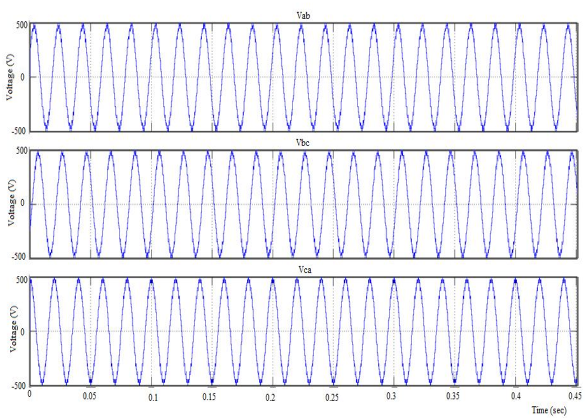

Fig .9.Line to line voltage output.

V. SIMULATION RESULTS

In order to verify that the proposed inverter, simulations were performed by using MATLAB/SIMULINK. Fig. 7 shows the Mat lab/ Simulink model of Simulation diagram of 25-level transistor clamped H-bridge (TCHB) cascaded multilevel inverter.

Proposed inverter involves three major divisions, they are PWM generation unit, DC-AC conversion and drives arrangement. Fig .8 shows the single leg phase voltage (Van) diagram, which shows the output level of phase voltage value.

Fig .9 indicates the line to line voltage of a proposed inverter.

Fig .10 shows the motor parameter output value which includes stator current, rotor current, torque, and speed.

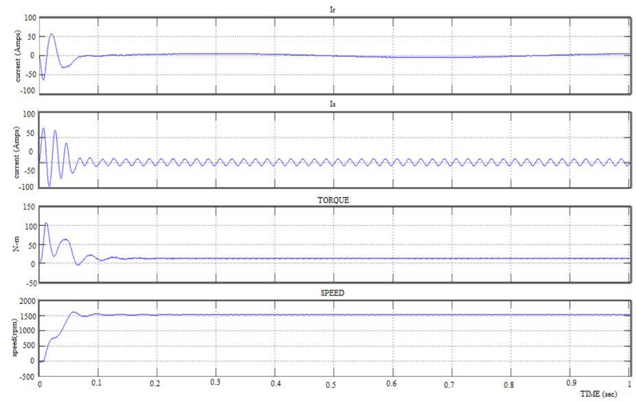

Fig.10. Motor parameter output

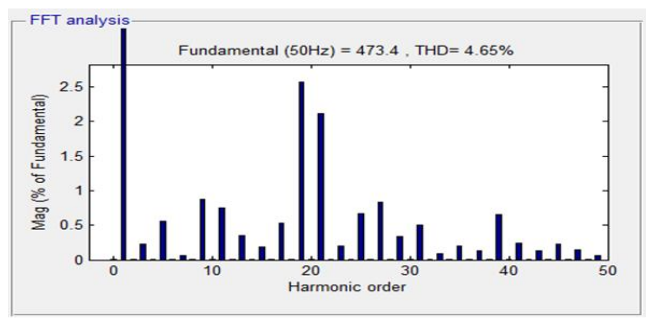

Fig .10.Line voltage harmonics with its THD value of a proposed inverter.

TABLE II
A COMPARISION OF THE CONVENTIONAL INVERTER AND THE PROPOSED INVERTER

Parameters	Conventional inverter	Proposed inverter
No of switches per leg	48	15
No of dc sources per leg	12	03
Line to line THD value	5.60%	4.65%

VI. CONCLUSION

In this paper, a 25-level transistor clamped H-bridge (TCHB) cascaded multilevel inverter with multicarrier

ISSN (Online) : 2319 – 8753
ISSN (Print) : 2347 - 6710

International Journal of Innovative Research in Science, Engineering and Technology

An ISO 3297: 2007 Certified Organization, Volume 3, Special Issue 1, February 2014

International Conference on Engineering Technology and Science-(ICETS'14)
On 10th & 11th February Organized by

Department of CIVIL, CSE, ECE, EEE, MECHNICAL Engg. and S&H of Muthayammal College of Engineering, Rasipuram, Tamilnadu, India

phase disposition (PD) is presented. The harmonics present in the inverter output voltage is determined through FFT analysis. The comparisons between the proposed inverter to 25-level conventional cascaded multilevel inverter in terms of harmonics were presented. Simulation results indicate that the THD of proposed inverter is much lesser than that of conventional cascaded multilevel inverter. The THD value of line to line voltage (V_{an}) of a proposed inverter is 4.65%. The proposed inverter is simulated by using MATLAB/ Simulink performance waveforms are verified.

REFERENCES

[1] P. W. Hammond, "A new approach to enhance power quality for medium voltage AC drives," IEEE Trans. Ind. Appl., vol. 33, no. 1, pp. 202–208, Jan./Feb. 1997.

[2] A. Varschavsky, J. Dixon, M. Rotella, and L. Moran, "Cascaded nine level inverter for hybrid-series active power filter, using industrial controller," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2761–2767, Aug. 2010.

[3] P. Lezana and R. Aceiton, "Hybrid multicell converter: Topology and modulation," IEEE Trans. Ind. Electron., vol. 58, no. 9, pp. 3938–3945, Sep. 2011.

[4] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

[5] F. Z. Peng, J. W. McKeever, and D. J. Adams, "Cascade multilevel inverters for utility applications," in Proc. Int. Conf. Ind. Electron Control Instrum., 1997, vol. 2, pp. 437–442.

[6] M. F. Escalante, J. C. Vannier, and A. Arzande, "Flying capacitor multilevel inverters and DTC motor drive applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 809–815, Aug. 2002.

[7] B. Wu, High-Power Converters and AC Drives. New York: Wiley-IEEE Press, Mar. 2006.

[8] P. Lezana and G. Ortiz, "Extended operation of cascade multicell converters under fault condition," IEEE Trans. Ind. Electron., vol. 56, no. 7, pp. 2697–2703, Jul. 2009.

[9] M. A. Perez, P. Cortes, and J. Rodriguez, "Predictive control algorithm technique for multilevel asymmetric cascaded H-bridge inverters," IEEE Trans. Ind. Electron., vol. 55, no. 12, pp. 4354–4361, Dec. 2008.

[10] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B.Wu,J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," IEEE Trans. Ind. Electron., vol. 57,no. 8, pp. 2553–2580, Aug. 2010.

[11] P. Sung-Jun, K. Feel-Soon, L. M. Hyung, and U. K. Cheul, "A new single phase five-level PWM inverter employing a deadbeat control scheme," IEEE Trans. Power Electron., vol. 18, no. 3, pp. 831–843, May 2003.

[12] B. Ge, F. Z. Peng, A. T. de Almeida, and H. Abu-Rub, "An effective control technique for medium-voltage high-power induction motor fed by cascaded neutral-point-clamped inverter," IEEE Trans. Ind Electron., vol. 57, no. 8, pp. 2659–2668, Aug. 2010.

[13] G. Waltrich and I. Barbi, "Three-phase cascaded multilevel inverter using power cells with two inverter legs in series," IEEE Trans. Ind Electron., vol. 57, no. 8, pp. 2605–2612, Aug. 2010.

[14] J. Holtz, "Selbstgefuhrte wechselrichter mit treppenformiger ausgangss-pannung fur grose leistung und hohe frequenz," Siemens Forschungsund Entwicklungsberichte, vol. 6, no. 3, pp. 164–171, 1977.

[15] J. Dixon and L.Morán, "High-level multistep inverter optimization using a minimum number of power transistors," IEEE Trans. Power Electron., vol. 21, no. 2, pp. 330–337, Mar. 2006.

[16] V. Guennegues, B. Gollentz, F. Meibody-Tabar, S. Rael, and L. Leclere, "A converter topology for high speed motor drive applications," in Proc. 13th EPE, Oct. 2009, p. 8.

[17] B. Gollentz and V. Guennegues, "Three-level inverter," U.S. Patent 20 100 084 922, Apr. 8, 2009.

[18] P.T.Josh, Jovitha Jerome and Arul Wilson," The Comparative Analysis of Multicarrier Control Techniques For SPWM Controlled Cascaded H- Bridge Multilevel Inverter," Proceedings of ICETECT 2011.