

# Two Dimensional Dual-Mode Lifting Based Discrete Wavelet Transform

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**Abstract - The Discrete Wavelet Transform (DWT) is one of the powerful signal processing tools. It has been effectively used in wide range of applications including image processing, speech analysis, pattern recognition and biometrics. Large amount of memory is required for storing the intermediate values for the implementation of Two Dimensional Discrete Wavelet Transform. Transposition Memory (TM) requirement is the major concern for the Two Dimensional 5/3 mode and 9/7 mode Lifting Based Discrete Wavelet Transform (LDWT). Interlaced Read Scan algorithm is proposed to achieve a Memory Efficient hardware Architecture for 2-D Dual Mode Lifting Based Discrete Wavelet transform, that reduces the TM. For Hardware Simplicity, Multiplier-less architecture is proposed which is applicable for both lossy and lossless coding.**

**Keywords: 2-D Dual Mode Lifting Based Discrete Wavelet Transform, Transposition Memory (TM).**

## 1. INTRODUCTION

Image compression is the application of data compression on digital images. Hence, image compression is necessary to reduce the amount of data required to represent a digital image. The main objective of image compression is to reduce redundancy of the image data in order to store or transmit data, at a given bit-rate (or compression rate). There are two forms of compression techniques. They are Lossless Compression and Lossy Compression.

A lossless algorithm reproduces the image exactly, where a small difference from neighbouring

data can result in statements with different meanings. A lossy algorithm loses some data where the loss may be unacceptable in many applications. The exact reconstructed value of each sample of the image is not necessary, where the varying loss of information can be accepted.

An image is represented as a two dimensional array of coefficients, each point representing the brightness level in that point. Most natural images have smooth colour variations, with sharp edges in between the smooth variations. The smooth variations and the sharp edges add upon them to the image, thereby giving a detailed image.

### A. DISCRETE WAVELET TRANSFORM

The wavelet transform is one of the major processing tools for image compression. Since the implementation of wavelet transform is remarkable, it is extensively used for signal analysis, compressing etc. In discrete wavelet transform, an image compression can be performed by passing the image signal through an analysis filter bank which consists of low pass and high pass filter at each level. The low pass filter extracts the coarse information of the signal and the high pass filter extracts the detail information of the signal. The output of both the filtering operations is then decimated by two. This way of down-sampling the filtered content of the image signal gives the first level decomposition output.

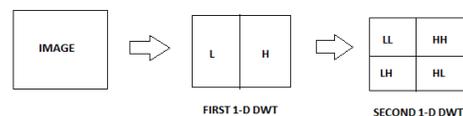


Fig 1. Block diagram of 2-D DWT for image

From the Fig 1, it is shown that the two dimensional Discrete transform can be accomplished by performing two separate one-dimensional transforms. For the image application, first the image is filtered along the horizontal direction using low pass and high pass analysis filter banks and then decimated by two. Decimating the transformed image gives the total sizes same as the original image.

Then it is followed by filtering the sub image along the vertical direction and then decimated by two. Finally the image is divided into four bands denoted by LL, HL, LH, LL sub-band images after the second one level decomposition. The LL Sub-band contains the compressed form of a original image. The reconstruction of the image can be carried out by up-sampling the data by the same factor of two on all four sub-bands at the coarsest scale and filtering those sub-bands in each dimension. The process is repeated until the image is fully reconstructed.

*B. Lifting Structures*

Implementation of DWT can be done as convolution based and lifting based. Since the convolution based operation has high computational complexity and large memory requirements, lifting based operations has been presented to overcome those drawbacks. The Lifting Structures (LS) method is a second generation wavelet transform for constructing wavelets.

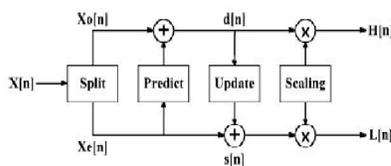


Fig 2.Lifting Structure

From the Fig 2, The Lifting method divides the input signal samples into both even and odd samples. Then Predict function (P) predicts odd samples from the even samples. The difference between this predict value and the odd sample values, gives the high frequency part of the signal which is known as the "detail" coefficients (d). Then applying the update function (U) on detail signal and combining the result with even samples gives the "approximation" coefficients (S).

The details and approximation coefficients (d , s) in lifting scheme, respectively, are the high pass and low pass outputs. Therefore, for prediction block,

$$d = X_{\text{odd}} - P (X_{\text{even}}), \tag{1}$$

for update block,

$$s = X_{\text{even}} + U (d) \tag{2}$$

Thus the Lifting Method consists of three main steps: Split, Predict and Update. Scaling is done at final stage to obtain the normalized value of high pass and low pass frequency outputs from the predict and update steps. The LS method has many advantages. It is efficient, minimizes the arithmetic operations, uses reduced memory registers and it is used to implement 5/3 and 9/7 wavelets, for lossless and lossy compression in the JPEG 2000 standard.

**II. RELATED WORKS**

Chih-Hsien Hsia et al (2013) proposed a low TM DWT architecture [1], which is the priority concern in spatial frequency domain implementation. In general, the memory requirement in DWT ranges from 2N to N<sup>2</sup> for the 2-D 5/3 and 9/7 modes LDWT. To reduce the TM, the memory access must be redirected. This paper presents a new approach, namely, interlaced read scan algorithm (IRSA) that changes the signal reading order from row-wise only to mixed row and column wise, and thus reduces the TM. The proposed 2-D LDWT is based on parallel and pipelined schemes to increase the operation speed. For hardware implementation, it can replace the multipliers with shifters and adders to yield high hardware utilization. Consequently, this 2-D LDWT has the characteristics of high hardware utilization, low memory requirement, and regular signal flow.

Chao-Tsung Huang et al (2004) proposed the flipping structure for the lifting-based discrete wavelet transform [3], which minimizes the critical path as well as the memory requirement of the lifting based discrete wavelet transform. The problem of serious timing accumulation for the conventional lifting-based architectures is addressed by flipping conventional lifting structures. The flipping structure also has better performance in the issues of round off noise and internal word length. In addition to reducing the critical path, the flipping structure can also provide

well-featured architectures for lifting-based DWT filters.

Basant. K. Mohanty et al (2011) presented a modular and pipeline architecture for lifting-based multilevel 2-D DWT [2]. Overall area-delay product is reduced in the proposed design by appropriate partitioning and scheduling of the computation of individual decomposition levels. The cascaded pipeline structure is proposed to maximize the Hardware Utilization Efficiency (HUE). Moreover, the proposed structure is scalable for high-throughput and area-constrained implementation. The redundancies resulting from the decimated wavelet filtering maximizes the HUE. From the result it is found that, the proposed scalable structure offers better Slice Delay Product (SDP) than the best of the corresponding existing structures for different input-block sizes and image sizes.

Wei Zhang et al (2012) proposed high speed and reduced area 2-D Discrete Wavelet Transform (2-D DWT) architecture is proposed [5]. In order to achieve a critical path with only one multiplier, four pipelining stages are required for one lifting step, or a large temporal buffer is needed. The number of arithmetic operations is reduced by using modified lifting scheme for flipping structure, where the predictor and updater stages are merged into a single lifting scheme and the co-efficients are inverted. To improve the speed, a technique called parallel processing is adopted, where with a single clock cycle four inputs are processed to obtain four outputs. In addition, the two-input/two-output parallel scanning architecture is adopted in our design. The proposed architecture only requires three registers between the row and column filters as the transposing buffer, so that higher efficiency can be achieved.

### III. PROBLEM DEFINITION

Several VLSI architectures have been proposed for efficient implementation of the 2-D LDWT. The implementation requires hardware architecture that needs large TM components or arithmetic components. Therefore a low TM requirement is the priority concern in the implementation of 2-D DWT. Although the lifting-based scheme has low complexity, its long and irregular signal paths induce a major limitation for efficient hardware implementations.

### IV. PROPOSED METHOD

The 2-D LDWT uses horizontal 1-D LDWT decomposition and a vertical 1-D LDWT decomposition to yield the 2-D LDWT. Each level of decomposition requires a large amount of memory which is termed here as Transposition memory. Therefore memory requirement dominates the hardware cost and architectural complexity of 2-D LDWT.

JPEG2000 gives the better image standard at high compression ratio. The filters used in JPEG2000 are (5, 3), (9, 7), (13, 7), (2, 6), (2, 10) and (6, 10). The LDWT Algorithm for 5/3 and 9/7 filters are presented in this paper.

#### A. INTERLACED READ SCAN ALGORITHM

In conventional lifting structures, the inter-mediate filter coefficients are stored in the Transposition memory which is of the order of  $N^2$  for an  $N \times N$ . Since it is a huge quantity using the memory of size  $N^2$ , the new technique named INTERLACED READ SCAN (IRSA), which is employed in the paper [1] is used to reduce the required TM to  $2N$  for 5/3 mode LDWT or  $4N$  for 9/7 mode LDWT. The Fig 3 shows the interlaced read scan technique of reading the image pixels.

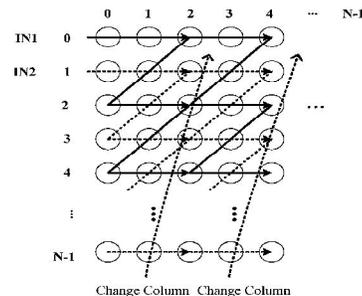


Fig 3. IRSA OF 2-D DWT

To increase the speed of operation, two pixels i.e.  $IN_1$  and  $IN_2$  are read in a single clock cycle from separate rows in the horizontal manner. When three pixels are read in three different clock cycles, the high pass filter output can be computed based on the equation (3)-(4) for 5/3 and (5)-(8) for 9/7 LDWT. One of the pixels, which is termed as the overlapped pixel is stored in the internal memory that can be used for

the computation of low pass filter output. Since two pixels are read in the particular one clock cycle, two high pass filters outputs can be obtained, thereby reading three pixels from subsequent two rows. The low pass filter outputs are computed from those two high pass filter output and the overlapped pixel in the same row, which is stored in the internal memory. This process of reading the image pixels and the computation of high pass and low pass filter outputs is repeated to the end of the row from where the next set of reading the pixels is transferred to the first row of the unread pixels. Thus the first level DWT stage is computed reading all the pixels in the horizontal manner.

The second-stage 1-D DWT works in a similar manner as the first-stage 1-D DWT, but reading the pixels is done in the vertical direction. The obtained high pass and low pass filter outputs from the first level is arranged separately in the vertical manner. When three high pass outputs are read, HH filter output can be computed. For the HL output, two HH and an overlapped high pass filter output is required. Similarly for LH outputs, three consecutive low pass filter outputs are required and for LL, two LH and an overlapped low filter output is required. The computation of HH, LH, HL, and LL are based on the equations (3)-(8). Thus the output from the second level 1-D DWT HH, LH, LH, LL sub-bands are obtained.

The difference between 5/3 and 9/7 mode LDWT is that the 9/7 LDWT requires extra two lifting steps compared to 5/3 mode LDWT.

**B. 2-D DWT:**

Consider a 7x7 image in Fig 4, where the input image pixels are fed to first stage 1-D DWT. The first levels of DWT decomposition yields the low pass and high pass filter outputs.

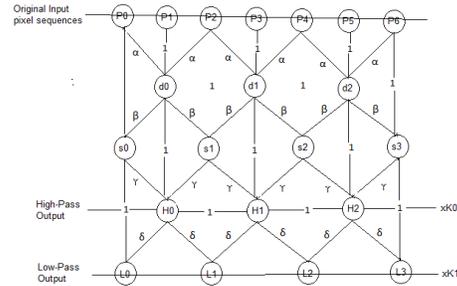
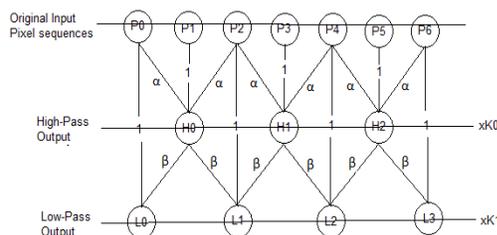


Fig 4. 5/3 and 9/7 LDWT Algorithms

Lifting steps associated with 5/3 mode LDWT yields

$$H_0 = [(P_0 + P_2) \times \alpha + P_1] \times K_0 \quad (3)$$

$$L_1 = [(P_0 + P_1) \times \beta + P_2] \times K_1 \quad (4)$$

Where the filter co-efficients are  $\alpha = -1/2$  and  $\beta = 1/4$  and  $K_0$  and  $K_1 = 1$ , where  $K_0$  and  $K_1$  denotes the scaling co-efficients. Similarly for 9/7 mode LDWT,

$$d_0 = (P_0 + P_2) \times \alpha + P_1 \quad (5)$$

$$s_1 = (d_0 + d_1) \times \beta + P_2 \quad (6)$$

$$H_0 = [(s_0 + s_1) \times \gamma + d_0] \times K_0 \quad (7)$$

$$L_1 = [(H_0 + H_1) \times \delta + s_1] \times K_1 \quad (8)$$

Where the filter co-efficients  $\alpha = -1.586134142, \beta = -0.052980118, \gamma = 0.882911075, \delta = +0.443506852, K_0 = 1.230174104$ , and  $K_1 = 1/K_0$ . The same method can be extended to any default filters in JPEG2000, except the lifting steps associated with it.

Each first-stage 1-D DWT receives one input data at one internal clock cycle. The computation involves after reading three input data, the two even pixels are added and the added pixel value is multiplied to the filter co-efficient values. The filter coefficient values are different for every filter.

To reduce the hardware complexity, Carry Save Adder is used for its fast computation and for multiplication purpose, Shift and add approach based on Horner's rule is employed. The following are steps for the multiplication based on Horner's rule.

- a) The binary equivalent of the filter coefficient is obtained.

METHOD	ADDER S	MULTIPLIER	TM	CRITICAL PATH
FLIPPING (2004)	16	10	5.5N	$T_M+5T_A$
MODIFIED FLIPPING (2012)	16	10	3 N	$T_M$
5/3 FILTER (proposed)	8	0	2 N	$2T_M+4T_A$
9/7 FILTER (proposed)	16	0	4 N	$2T_M+4T_A$

b) The Horner's algorithm is based on the positions of the 1's in the filter coefficient i.e. right most 1 and their distance to the immediate 1 to their left is considered as the weight, which is to be multiplied with multiplicand pixel value and adding it to the same multiplicand value, the immediate value is obtained

c) The second step is repeated moving left, obtaining the intermediate values until the last 1 before the binary point.

d) In the last step, first 1 distant right from the decimal point is considered as the weight and it is then multiplied with the previously obtained intermediate value.

For example for 9/7 filter,  $\gamma = 0.882911075$  and its binary equivalent is 0.110011001100 when the pixel X to be multiplied by  $\gamma$ , so the multiplication can be carried out using horner's rule is shown in the Fig 5 as,

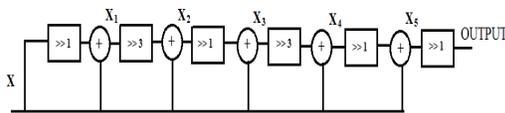


Fig 5. Horner's rule for multiplication

The result obtained is then added with the odd pixel, thus the high frequency output is obtained. Horner's method of shift-add algorithm results in minimized shifters and adders compared to multiplication based on shift-add approach. The obtained high frequency filter outputs are stored in the register memory that can be further used in the computation of low frequency filter output.

The second level of decomposition can be carried out with the obtained high pass and low pass

filter outputs from the first stage in the similar manner, the only difference is that the images signals are processed in the vertical manner. The output from the second level decomposition is that the four sub-band coefficients LL, LH, HL, HH co-efficients.

**Table**-Performance comparison of different Lifting Based Architectures

Therefore the overall system diagram of 2-D Dual mode LDWT is given as shown in the fig 6, which contains the two sets of 1-D DWT at the first stage and two sets of 1-D DWT at the second stage. The two sets of 1-D DWT in the first stage shows the two sets of inputs  $IN_1$  and  $IN_2$  are processed in parallel that yields two sets of high frequency and low frequency outputs. The High frequency output from the first stage is fed to the upper second 1-D DWT and the low frequency output from the first stage is fed to the lower second 1-D DWT.

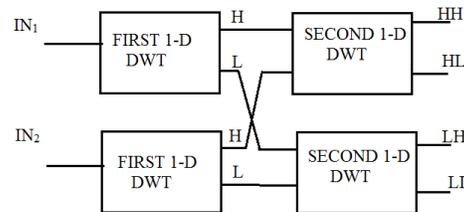


Fig 6. System diagram of 2-D LDWT

The obtained coefficients in which the LL sub-band contains the compressed form of the input image. The levels of decomposition can be carried out to the desired number of stages until the required output is obtained.

## V. COMPARISONS AND RESULTS

The wavelet coefficients of the dual-mode LDWT are different. The coefficients for 5/3 mode LDWT are  $\alpha = -0.5$  and  $\beta = 0.25$  and for 9/7 mode  $\alpha = -1.586134142$ ,  $\beta = -0.052980118$ ,  $\gamma = +0.0882911075$ ,  $\delta = +0.443506852$ . For calculation simplicity, multiplication is implemented using shift-add approach based on Horner's rule, where the floating point representation of the filter coefficients is considered. Therefore, operation complexity is reduced compared to integer type multiplication based on shift and add

approach. Also the number of shifters is reduced compared to other methods.

The performance comparison of different Lifting Based architectures with the proposed method is given in the Table below in terms of the number of multipliers, adders, TM size and critical path (CP).

A trade-off exists between low TM and low complexity in the design of the 2-D dual-mode LDWT architecture. Comparison results indicate that the proposed VLSI architecture outperforms the previous works in terms of TM size, in particular around 50% less memory requirement than that of existing lifting based DWT architectures and to reduce the TM requirement IRSA is proposed.

As the result, the TM of an image of size  $N \times N$  simply needs  $2N$  or  $4N$  for  $5/3$  or  $9/7$  schemes, respectively. A 2-D LDWT was designed and simulated with VHDL to verify the performance of the proposed hardware architecture.

## VI. CONCLUSION

A new 2-D Dual Mode Lifting Based DWT architecture to meet the requirements of image compression is proposed. It can provide low memory requirement and less hardware complexity. Moreover, a new approach, namely, IRSA, was proposed to reduce the TM requirement for the 2-D dual-mode LDWT. The proposed 2-D architectures were more efficient than former architectures in trading off low TM requirement, regular memory access sequence. The  $5/3$  and  $9/7$  filter with different lifting steps were realized by cascading the four modules (split, predict, update, and scaling phases). This method is applicable to both lossy and lossless image applications. Moreover, the architecture is fully based on multiplier-less hardware that reduces the hardware complexity.

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