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# 3D Simulation Study Of Soft Error On Junctionless 6T-SRAM

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**Abstract**— As CMOS device is scaling down significantly, the sensitivity of Integrated Circuits (ICs) to Single Event Upset (SEU) radiation increases. As soft errors emerge as reliability threat there is significant interest in the development of various techniques, both at device and circuit level, for SEU hardness in SRAM memories. Junctionless Transistor (JLT) based on 6T-SRAM cell is studied in this paper for their SEU or soft error performance using 3D TCAD simulations. The critical dose observed in JLT based 6T-SRAM to flip the cell is given by Linear Energy Transfer (LET) = 0.1 pC/μm. The simulation result analyzes electrical and SEU radiation parameters to study its impact on JLT based 6T-SRAM memory circuits.

***Keywords***— Soft error, Junctionless 6T-SRAM, SEU Radiation, LET, HeavyIon, TCAD Simulation

## I.INTRODUCTION

Scaling of CMOS devices are mainly suffering from Short Channel Effect (SCEs) and Drain Induced Barrier Lowering (DIBL). Also as the CMOS device is scaling down, the impact of radiation, coming from the natural space or present in the terrestrial environment, on integrated circuits (ICs) is going up [1] i.e. the amount of minimum charge (known as critical charge) required to flip the memory cell (SRAM) decreases with scaling [2]. This event is known as soft error. Increasing design and fabrication complexities, smaller feature sizes, lower voltage and higher current levels, intrinsic parameter fluctuations, higher operating frequencies are also projected to cause an increase in the soft error failure rate in sub-90 nm ICs [3]. Soft error studies of deep sub-micron MOSFET-based 6T-SRAMs are dealt in detail in [4, 5]. ITRS roadmap indicates that semiconductor memories will occupy major portion of chip area in the near future technologies [6]. SEUs have also been analyzed as an important reliability factor in the development of semiconductor memories [7]. Semiconductor memories such as SRAM is by far the dominant form of embedded memory found in today's ICs occupying as much as 60-70% of the total chip area and about 75%-85% of the transistor count in some IC products [8]. The most commonly used 6T-SRAM memory cell design uses six transistors to store a bit.

Since, the CMOS scaling technology brings in many unconventional devices especially FinFET, it is necessary to study the radiation effect on these devices and circuits. The transient response of FinFET is studied in [9] through by 3-D numerical simulation of sensitivity to SEU. FinFET-based 6T-SRAM circuits are studied using TCAD simulations [10]. Junctionless FinFET introduced by Colinge et. al. [11] has attracted device community. The simple radiation analysis of a junctionless device is studied by Munteanu et. al. [12]. Soft error study of Junctionless FinFET based SRAM is yet to be studied. In this paper, we have studied the SEU/soft error performance of tri-gate Jnless 6T-SRAM circuit. Minimum radiation dose required to flip the cell is found out by doing the transient simulations using TCAD device simulator.

This paper is organized as follows: Section II discusses about Junctionless device construction and calibration Section III talks about Junctionless 6T-SRAM structure simulation and SRAM operation. Section IV explains SEU radiation phenomena on Junctionless 6T-SRAM and provides the simulation results and discussions. Section V provides the conclusion.

## II.DEVICE CONSTRUCTION AND CALIBRATION

The various device parameters are shown in the schematic diagram of Fig. 1. Sentaurus TCAD simulator from Synopsys is used in this work. The simulator has many features and modules used in our simulation are: Sentaurus Structure Editor (SDE) is used to create device structure, an individual device, common Tri-Gate-NMOS and PMOS JLT is created as shown in Fig.2 and Fig.3 prior to SRAM simulation.

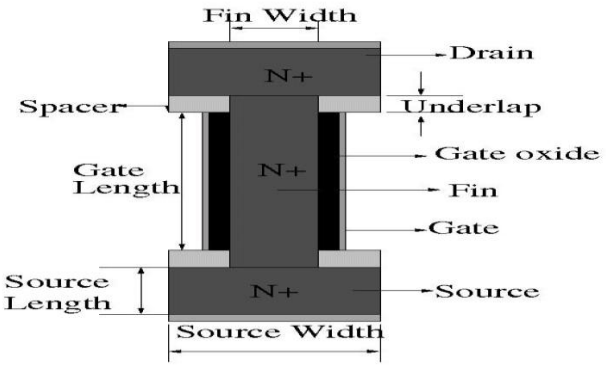


Fig.1 Schematic view of 2-D Junctionless FET

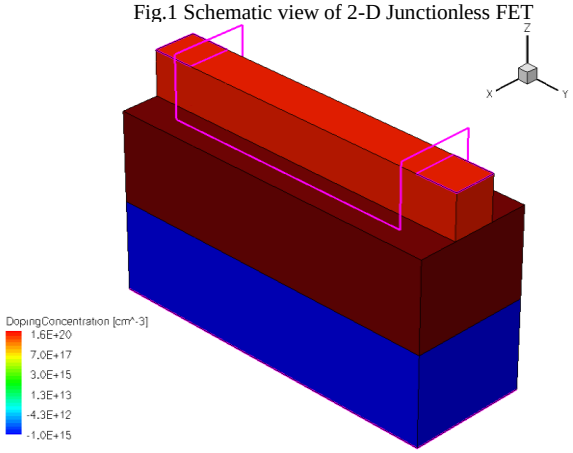


Fig. 2 Common Tri-gate JLT NMOS Device Structure (Gate Oxide is removed)

While doing the device simulation, the mobility model includes doping dependency, high-field saturation and transverse field (i.e. gate field) dependency etc.

Sentaurus Device (SDEVICE) Simulator is used to simulate transient curves, Inspect is used to view the results [13]. An $I_D$-$V_G$ characteristic of NMOS device is shown in Fig. 4. Supply Voltage ($V_{dd}$) used in this study is 1 V. Table I gives the various device dimensions and doping values.

### III. Junctionless 6T SRAM Structure

JLT is a multigate FET with no PN nor N+N or P+P junctions. Unlike a MOSFET, for a JLFET channel, the doping concentration and type are equal to those in the source and drain. Since this device has no concentration gradient in the lateral direction of the conduction layer, it does not have any p–n junction. The doping concentration used in JLT typically in the range of $10^{19}$ $cm^{-3}$, uniform, and homogenous across the source (S), channel, and drain (D) region.

A JLT based 6T-SRAM cell is designed by replacing the conventional MOSFETs or SOI (silicon-On-Insulator) based multi-gate transistors with Jnless transistors.

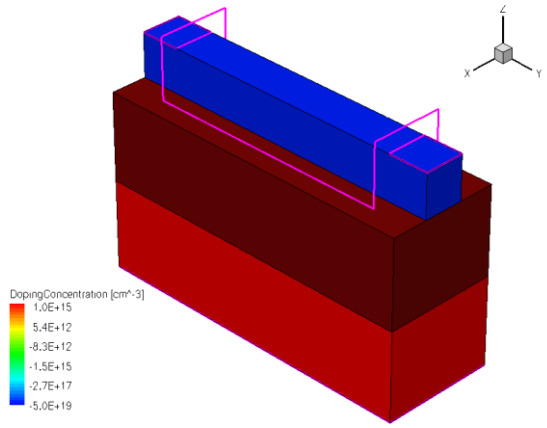


Fig. 3 Common Tri-gate JLT PMOS Device Structure (Gate Oxide is removed)

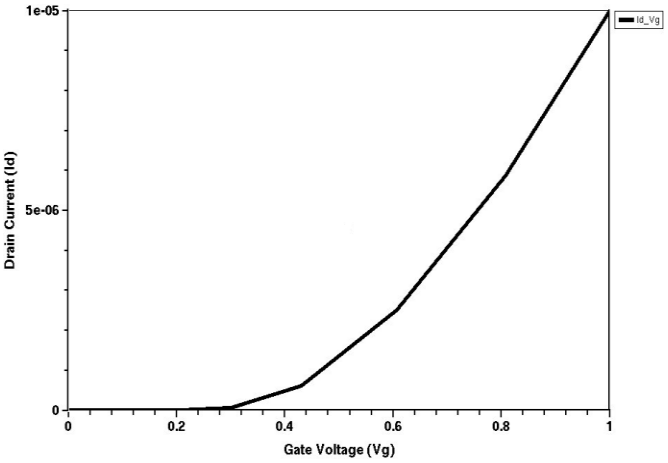


Fig 4 Common Tri-gate JLT NMOS Device $I_D$-$V_G$ Simulation

TABLE I.
Device Dimensions

| Parameter | Value |
|---|---|
| Gate length ($L_g$) | 30 nm |
| Gate-oxide thickness ($T_{ox}$) | 2 nm |
| Fin width (W ) | 5 nm |
| Fin height (H ) | 5 nm |
| Channel doping | $8\times 10^{19}/cm^3$ (N transistor)<br>$2.5\times 10^{19}/cm^3$(P transistor) |
| Source-drain doping | $8 \times 10^{19}/cm^3$ ( N transistor)<br>$2.5 \times 10^{19}/cm^3$ ( P transistor) |

The generated 6T-SRAM structure from SDE is shown in Fig. 5. Meshing is shown on one-side of the device namely (N2, ACC2, P2 transistors) in Fig. 5. In this new design approach, trigate Jnless device provides gate controllability on three sides. Using a trigate device architecture it is possible to turn the device on and off to obtain MOSFET-like electrical characteristics.

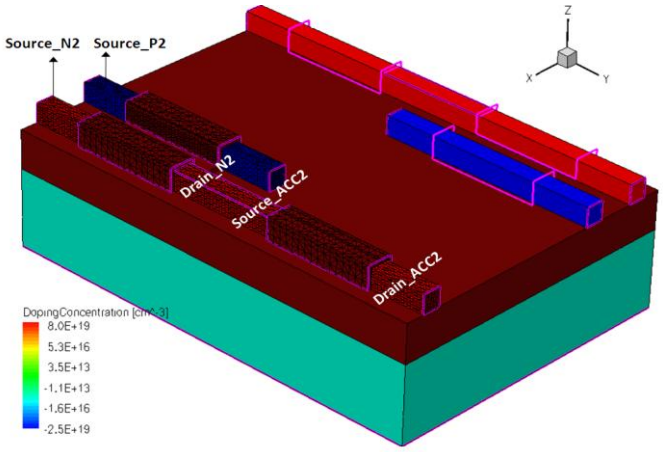


Fig.5 Common Tri-gate JLT 6T-SRAM Structure

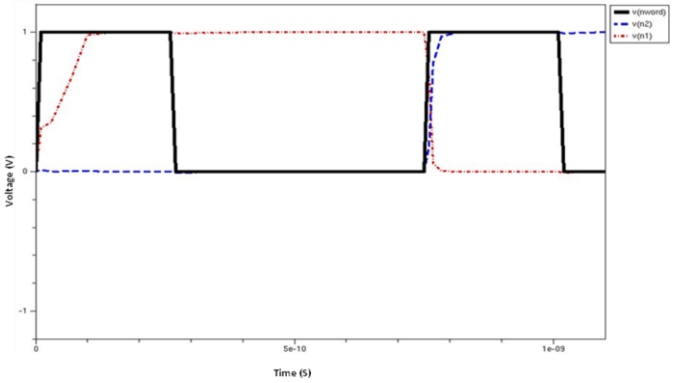


Fig.6 6T-SRAM simulation

In this work, JLT based 6T-SRAM is subjected to heavy ion based SEU radiation. Minimum radiation dose required to flip the cell is found out by doing the transient simulations with radiation models turned-on in TCAD device simulator.

Figure 6 shows 6T-SRAM operation simulation curve before SEU radiation. Mixed mode simulation approach is used in SRAM simulation. In mixed mode simulation some portion of the circuit can be simulated at the device level and some part of the circuit can use compact models. In this study, interconnects are assumed to be perfect interconnects. The details of rise and fall time, pulse width of data and access pulses used in SRAM simulation are given in Table II.

TABLE II.
DATA AND ACCESS PULSE TIMINGS

| nbit(data) | | | n(word) | | |
|---|---|---|---|---|---|
| Rise Time (pS) | Fall Time (pS) | Pulse width (pS) | Rise Time (pS) | Fall Time (pS) | Pulsewidth (pS) |
| 10 | 10 | 500 | 10 | 10 | 250 |

## IV. SEU RADIATION EFFECTS AND RESULTS

The simulation of SEU caused by a heavy ion impact is activated by using the proper keyword ('HeavyIon') in the physics section of SDEVICE. The characteristics of the heavy ion like direction, characteristic radius, dose value or Linear Energy Transfer (LET in pC/µm), strike location etc. can be specified. The heavy ion strikes at location with direction of motion of ions from top to bottom along vertical axis. Length of the ion track is 0.035 µm, characteristic radius $w_t$ = 0.01 µm. Heavy ion bombardment is initiated in the simulation during the non-access period, at the drain region which has value '1'. Fig. 7 shows node voltages after heavy ion strike at t= 275ps for LET = 0.09 pC/ µm. By properly choosing LET value, the state of the cell can be flipped as shown in Fig. 8. The minimum required LET value to flip the cell is of our interest.

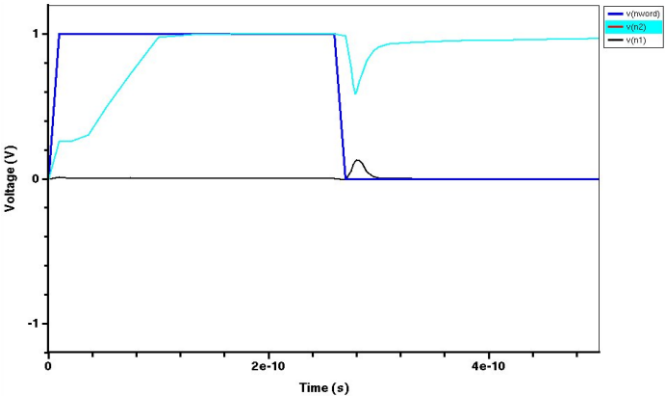


**Fig. 7** Node Voltages after Heavy Ion Strike at 275 ps (LET= 0.09 pC/µm)

Figure 9 and 10 shows the heavy ion generation, heavy ion charge density and electro-static potential distribution across the tri-gate Jnless 6T-SRAM structure during radiation at t=275 pS for a dose value of 0.09 and 0.1 pC/ µm. Dose or LET value of 0.09 pC/ µm does not flip the SRAM cell. As already stated the minimum required LET value to flip the cell is of our interest. Tri-gate Jnless 6T-SRAM based structure switches its state at LET value of 0.1 pC/µm.

There are various parameters like electron and hole densities, electron and hole current densities, electro-static potential, SRH recombination rate etc. can be analyzed to

study the SEU radiation effects. Figure 11 shows SRH recombination rate across the structure at three different time instants, i.e. @250 pS, @275 pS, and @330 pS. These time instants correspond to pre, peak and post radiations. It can be observed from Fig. 11 that the SRH recombination rate is very low for pre and post radiations.

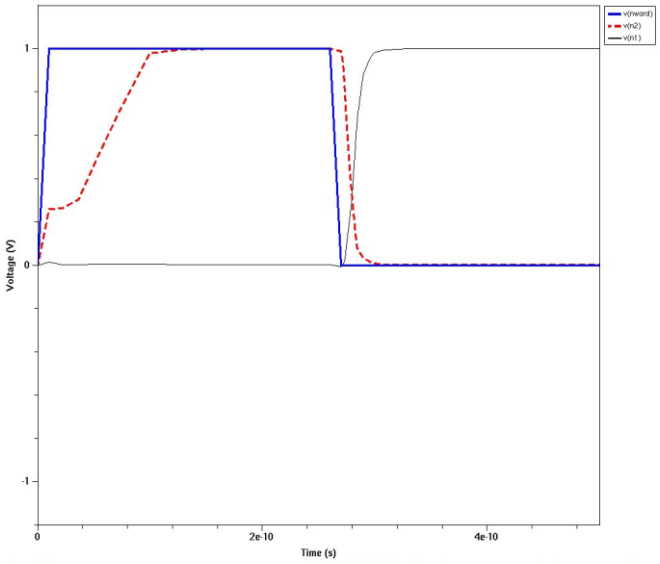


Fig. 8 Node Voltages after Heavy Ion Strike at 275 ps (LET=0.1 pC/µm)

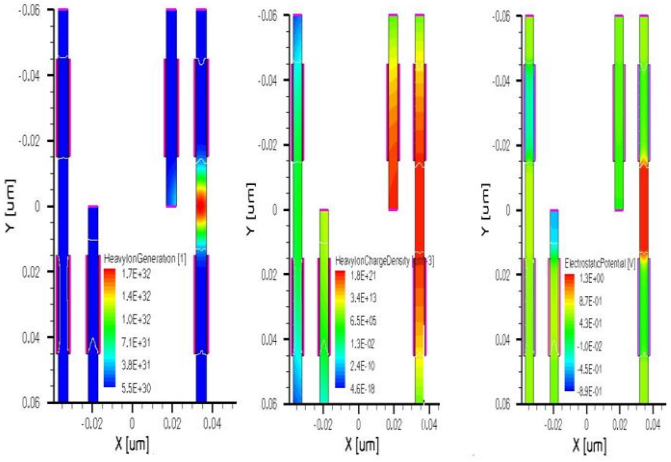


Fig. 9 2D profile of HeavyIonGeneration, HeavyIonChargeDensity, Electrostatic Potential of Tri-gate JLT 6T-SRAM structure at 275 pS (LET=0.09 pC/µm)

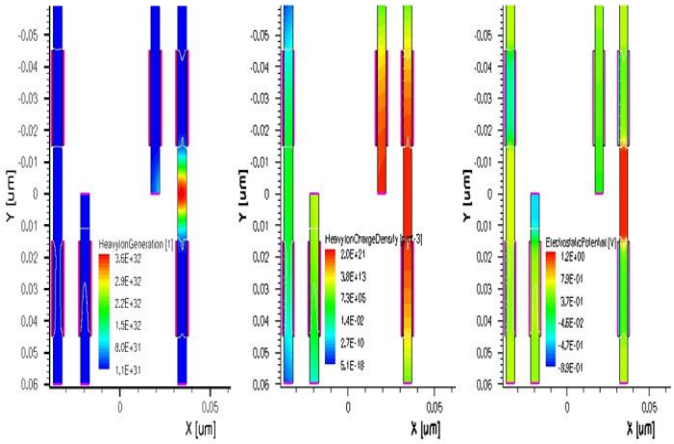


Fig. 10 2D profile of HeavyIonGeneration, HeavyIonChargeDensity, Electrostatic Potential of Tri-gate JLT 6T-SRAM structure at 275 pS (LET=0.1 pC/µm)

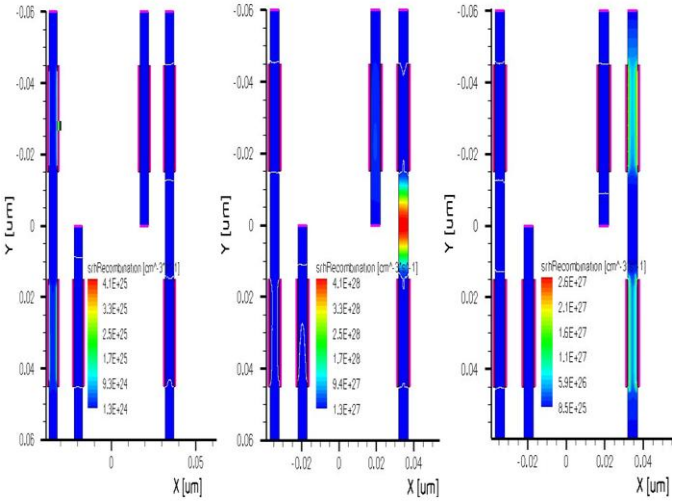


Fig. 11 Tri-gate JLT 6T-SRAM SRH Recombination pre-peak-post radiation simulation (LET=0.1 pC/µm)

## V. CONCLUSION

Tri-gate Jnless 6T-SRAM is simulated and studied for their SEU/soft error performance (the minimum LET value required to flip the cell) in TCAD. The LET required to flip the Jnless 6T-SRAM is observed and the value is found to be LET = 0.1 pC/µm. The simulation result analyzes electrical and SEU radiation parameters to study its impact on JLT based 6T-SRAM memory circuits. The future direction is to compare various topologies of Jnless 6T-SRAM with inversion mode 6T-SRAM to observe the SEU/soft error performance

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