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Power Quality Improvement in BLDC Motor Drive using Fuzzy Controlled Zeta Converter

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ABSTRACT: This paper presents a power factor corrected (PFC) fuzzy controlled zeta converter-fed brushless direct current (BLDC) motor drive as a cost-effective solution for low-power applications. In this work, by adjusting the dc link voltage of the voltage source inverter (VSI) feeding a BLDC motor, the speed of the BLDC motor is controlled . This paper deals with the implementation of pulse width modulated Zeta converter with power factor correction, lower total harmonic distortion factor and better efficiency. The proposed zeta converter based BLDC Motor drive is implemented to improve the power quality and to obtain unity power factor at ac mains for a wide range of speed control. A MATLAB/ Simulink environment is used to simulate the model to achieve a wide range of speed control with improved PQ (Power Quality) at the supply.

KEYWORDS: VSI, BLDC, PFC

I. INTRODUCTION

The day by day increasing demand for energy can create problems for the power distributors, like grid instability. In recent years brushless dc (BLDC) motors are widely used applications including appliances, automotive, aerospace, consumer, medical, automated industrial equipment and instrumentation because of their high starting torque, high efficiency, reliability, lower maintenance compared to its brushed dc motor. In a BLDC motor, the rotor magnets generate the magnetic flux, so BLDC motors achieve higher efficiency. [1] [2] Therefore, BLDC motors may be used in high end white goods (refrigerators, washing machines, dishwashers, etc.), high-end fans, and pumps and in other appliances which require high reliability and efficiency. BLDC motors have many advantages over brushed DC motors and induction motors, like higher efficiency and reliability, lower acoustic noise, smaller and lighter, greater dynamic response, better speed versus torque characteristics, higher speed range, longer life. Since the specific torque is higher it can be very useful in the applications were space and weight are critical factors. And also the BLDC motor is electrically commutated by power switches instead of brushes it has so many advantages such as no brushes/commutator maintenance, no brush friction to reduce useful torque, no mechanical limitation imposed by brushes or commutator, no arcs from brushes to generate noise, causing EMI problems.[3]

The BLDC motor drive is fed from single-phase ac supply through a diode bridge rectifier (DBR) followed by a high value of smoothening capacitor at dc link which draws a pulsed current, with a peak higher than the amplitude of the fundamental input current at ac mains due to an uncontrolled charging and discharging of the dc link capacitor.[4] This causes in poor power quality (PQ) at ac mains in terms of poor power factor (PF), high total harmonic distortion (THD) of ac mains current, and high crest factor (CF). Therefore, a Power Factor correction (PFC) converter is inevitable for Brushless DC Motor Drive inorder to improve the power quality. [5] There are many existing topologies regarding power factor correction in BLDC motor drive. Some of the existing topologies consist of a Single Ended Primary Inductance Converter (SEPIC) and buck-boost converter based BLDC motor drive which has higher losses in the voltage source inverter due to conventional PWM switching and large number of voltage and current sensors are used that additionally adds to the cost of the converter. And in another topology a cuk converter fed BLDC motor drive with a variable DC link voltage is used that reduces the switching losses since it uses only the fundamental switching frequency, but it has a major disadvantage that it requires three sensors. So it is not used for low power rating and low-cost applications.[6]-[8] The above used topologies consist of bridge converters and it also contributes switching losses so bridgeless topologies are preferred. The usage of diode rectifiers that cause more switching stresses are eliminated by bridgeless converters.[9] And also some topologies with bridgeless converters like bridgeless boost, cuk, buck-boost, SEPIC converters are there. But all these power factor correction techniques have some limitations. They

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cannot be used for low power applications.[10] So the proposed PFC technique below is designed in such a way that is suited for low power applications.[11]-[14] The objective of the paper is to use zeta converter fed BLDC motor drive inorder to improve the power quality at the supply by reducing the total harmonic distortion factor and increasing power factor to unity. And also by adjusting the dc link voltage of the voltage source inverter (VSI) feeding a BLDC motor, the speed of the BLDC motor is controlled .

II. OPERATION OF ZETA COVERTER

This converter is the latest type of single-stage input current shapers. It also uses single switching device and inherently provides an overload, short circuit, and inrush current protections. Since zeta converters behave as a resistive load to input AC mains, this converters are also called resistance emulators. Zeta converter is fourth order converters that can step down or step up the input voltage. The ZETA converter also have a series capacitor sometimes called a flying capacitor and two inductors. The ZETA converter topology gives a positive output voltage from an input voltage.

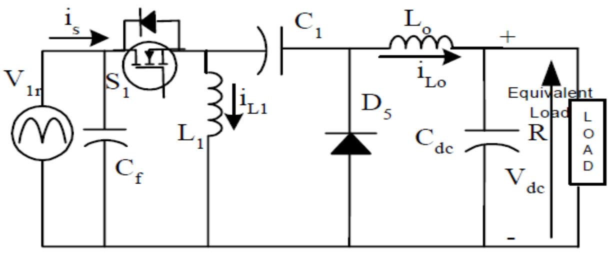

Fig. 1: Circuit of Zeta Converter

The Zeta converter has many advantages, such as buck-boost capability, and continuous output current, input to output DC insulation, so it can be used in high reliability system. This topology offer high efficiency, especially by using the synchronous rectification. The synchronous rectification can be easily implemented in this converter, because this topology, unlike the SEPIC converter, uses a low-side rectifier. The equivalent circuit of the Zeta converter is shown in Fig.1

Three modes and their associated waveforms are shown in Fig. 2(a)-(d). These modes are described as follows.

MODE I : In this stage, switch S1 is turned on and the input source supply energy to the input inductor (L_1). This energy is then subsequently transferred to output inductor (L_o) through the intermediate capacitor C_1. The current in the output inductor (i_{Lo}) and input inductor (i_{L1}) increase linearly. The intermediate capacitor voltage (V_{c1}) and the output DC-link capacitor voltage (V_{dc}) are considered constant in this stage. They are equal to the DC voltage(V_{dc}). This stage is shown in Fig.2(a)(i).

MODE II : In the second stage, switch S_1 is turned off and diode D_5 starts conducting. The stored energy from output inductance (L_o) and the input inductance (L_1) are transferred to the intermediate capacitor C_1 and the DC link capacitor filter (C_{dc}), respectively. This stage continues until i_{L1} becomes equal to the negative of i_{Lo} as shown in Fig.2(a)(ii). In this stage of Zeta converter operation, the MOSFET switch S1 is in off stage and diode D_5 is in on stage.

MODE III : This freewheeling stage lasts until the start of a new switching period and is shown in Fig.2(a)(iii). In this stage of operation neither output diode 'D_5' nor switch 'S_1' conducts. The voltage applied across inductances L_o and L_1 is zero and their currents are constant until the new switching cycle starts. The currents i_{Lo} and i_{L1} become equal and opposite at t_{off} time. Therefore, in this stage the current through the output diode is zero.

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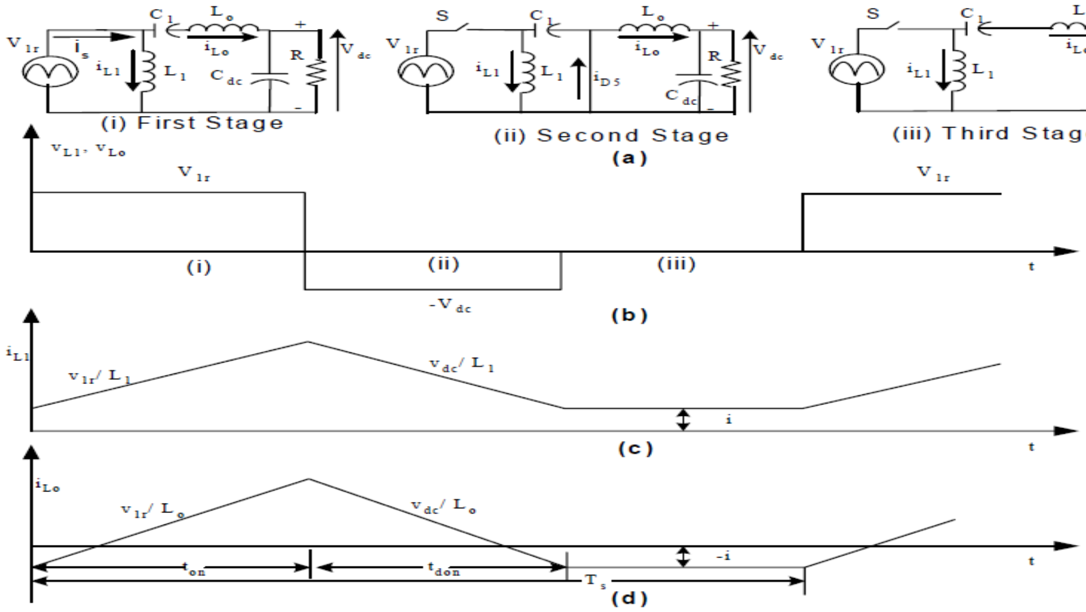

Fig. 2 (a) Three Different Operating Stages (i), (ii) and (iii) of Zeta Converter in DCM of Operation and its (b) Voltage Waveforms (c) and (d) Inductors Current Waveform

III. DESIGN OF ZETA COVERTER

The design of zeta converter for power factor correction and speed controlled in BLDC motor drive has the main objective of the PQ improvement at AC mains. The design equations of zeta converter are given below.
The expression for output DC Link Voltage of zeta converter

$$V_{dc} = \left(\frac{N_2}{N_1}\right) V_{in} \frac{D}{(1-D)} \quad (1)$$

$$V_{in} = \frac{2\sqrt{2}}{\pi} V_s \quad (2)$$

where V_{in} is the input voltage applied to zeta converter, V_s is the source voltage and D is the duty cycle of converter
The Critical value of Magnetizing Inductor is expressed as

$$L_{mc} = \left(\frac{V_{dc}^2}{P_i}\right) \frac{\{1-D\}}{2D\ f_s \left(\frac{N_2}{N_1}\right)^2} \quad (3)$$

$$L_o = \frac{V_{dc}\{1-D\}}{f_s(k\ I_o)} \quad (4)$$

where D represents the duty ratio and $N2/N1$ is the turns ratio of the HFT. the value of L_1 is selected around 1/10th of L_{mc} and f_s is the switching frequency (which is taken as 20 kHz) and L_o is the expression for output inductor and k represents the percentage ripple of the output inductor current which is taken as 40% of output inductor current.
An expression for intermediate capacitor (C_1) is as

$$C_1 = \frac{V_{dc}\ D}{\eta\{\sqrt{2}V_s + V_{dc}\}f_s} \left(\frac{P_i}{V_{dc}^2}\right) \quad (5)$$

where P_i is the instantaneous power and η is the permitted ripple voltage across intermediate capacitor
The value of DC link Capacitor is

$$C_d = \left(\frac{P}{V_{dc}}\right) \frac{1}{2\ \omega(\eta V_{dc})} \quad (6)$$

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IV. PROPOSED PFC-BASED BLDC MOTOR DRIVE WITH ZETA CONVERTER

Fig.3 shows the proposed zeta converter-fed BLDC motor drive. A single-phase ac supply is converted to DC by using DBR followed by a large value capacitive filter and zeta converter. The filter is is used to reduce DC voltage ripples, which produces an increased THD of input AC mains current and excessive peak input currents that leads to poor power factor. The zeta converter is designed to operate in DCM to act as an inherent power factor correction converter. This combination of DBR and PFC zeta converter is used to feed a BLDC motor drive through a three-phase VSI as shown in Fig.3. The speed of BLDC motor is directly proportional to the DC link voltage of the VSI. The reference voltage generator produces a voltage by multiplying the speed with the voltage constant (K_b) of the BLDC motor drive. An error voltage obtained by comparing the measured dc link voltage and reference voltage is fed to PI controller. The Proportional Integral controller is used to minimize the error signal and also it produce a controlled output to the PWM generator to produce a PWM signal of fixed frequency and varying duty ratio.

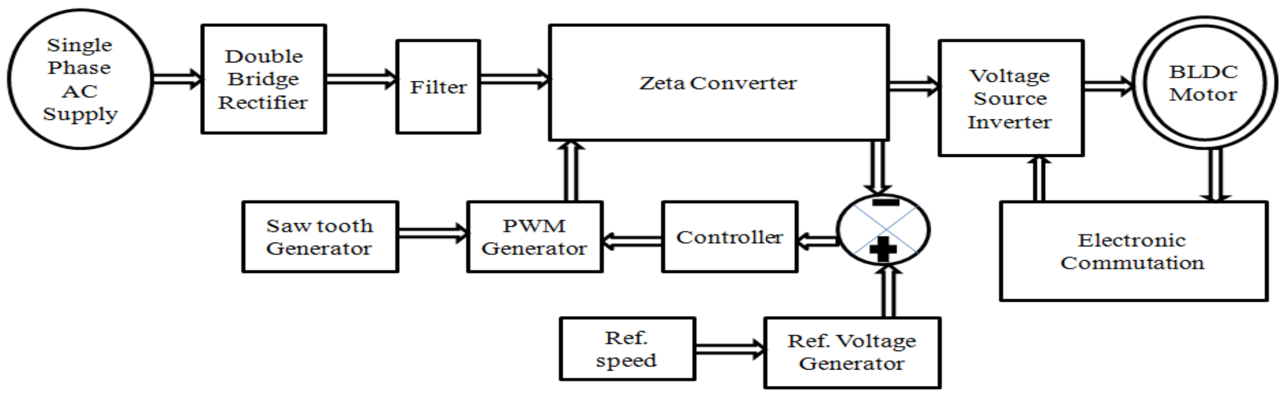

Fig.3 Proposed PFC-based zeta converter fed BLDC motor drive

4.1 FUZZY CONTROLLER

Error (E) and change in error (CE) are the inputs for the fuzzy controller whereas the output of the controller is change in duty cycle. The error is defined as the difference between the reference voltage and actual voltage , the change in error is defined as the difference between the present error and previous error and the output, Change in duty cycle is which could be either positive or negative is added with the existing duty-cycle to determine the new duty-cycle (DC_{new}) The error and change of error of the output voltage will be the two inputs of fuzzy logic controller. These two inputs are divided into five groups; NB: Negative Big, NS: Negative Small, Z: Zero Area, PS: Positive small and PB: Positive Big.

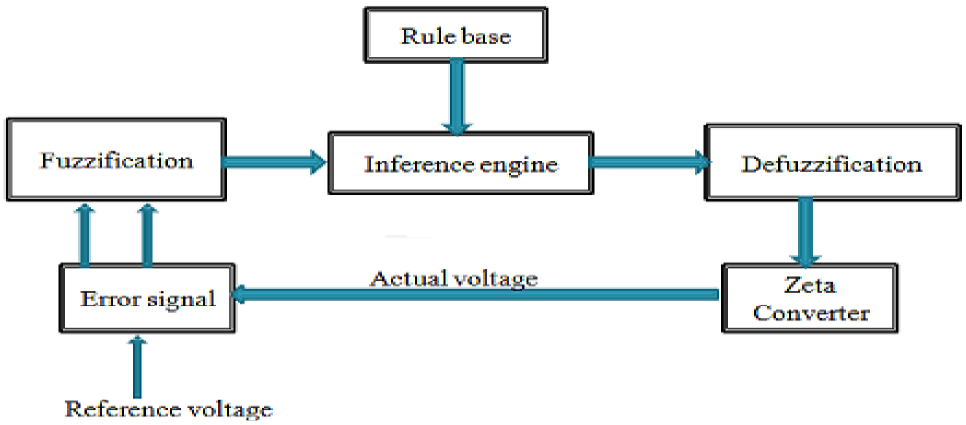

Fig.4 Fuzzy logic controller

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V. SIMULATION RESULTS AND DISCUSSION

Table 1: Specifications of BLDCMD

No. of poles	4
Rated DC bus voltage	130V
Rated Speed	1500rpm
Rated Torque	1.2Nm
Rated Power	188.49W
Voltage Constant	57.59V
Torque Constant	0.55 Nm/A
Stator windings per phase resistance	4.32

Table 1 shows the specifications of BLDC Motor Drive and a block diagram with above specifications of the drive system implementation is shown in Fig. 5.

5.1 WITHOUT ZETA CONVERTER

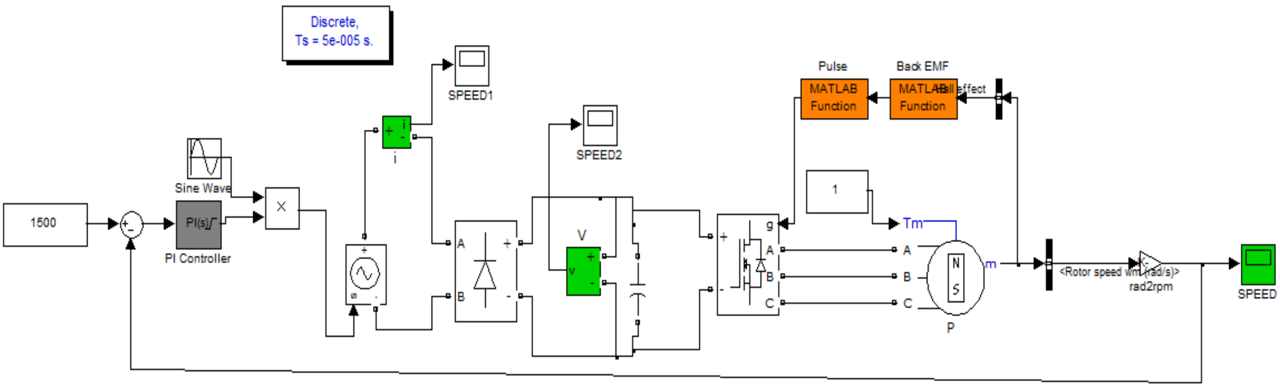

Fig.5 BLDC motor drive without PFC Converter

Fig. 5 shows the simulation model of the BLDC Motor Drive without Power Factor Correction Converter. The operation of the proposed topology has been verified by simulations. The simulations are done in Matlab/Simulink platform.

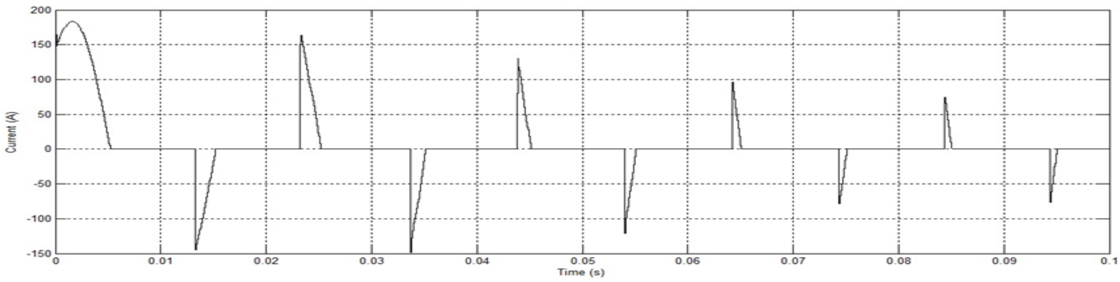

Fig.6 Current waveform at ac mains of BLDCMD without PFC converter

The BLDCMD is fed from a single-phase ac supply through a diode bridge rectifier (DBR) followed by a capacitor at dc link. It draws a pulsed current as shown in Fig. 6, with a peak higher than the amplitude of the fundamental input current at ac mains due to an uncontrolled charging of the dc link capacitor.

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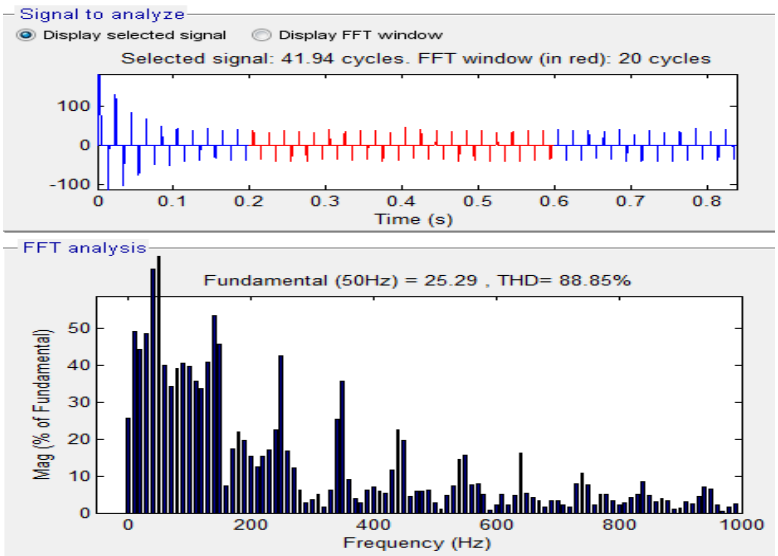

Fig.7 Harmonic Spectra of BLDC Motor Drive without PFC converters

This results in poor power quality (PQ) at ac mains, high total harmonic distortion (THD) of ac mains current (shown in fig. 7) at the value of 88.85 %.

5.2 WITH ZETA CONVERTER

Table 1: Specifications of Zeta Converter

Magnetizing inductance of HFT (*Lm*)	250 µH
Output inductor (L_o)	4.2 mH
Intermediate capacitor (*C*1)	0.44 µF
dc link capacitor (*Cd*)	2200 µF
filter capacitor (*Cf*)	330 nF
filter inductor (L_f)	3.77mH

Fig.8 shows the simulink model of BLDC Motor Drive with zeta converter. Here zeta converter is implemented to increase power quality of BLDC Motor Drive.

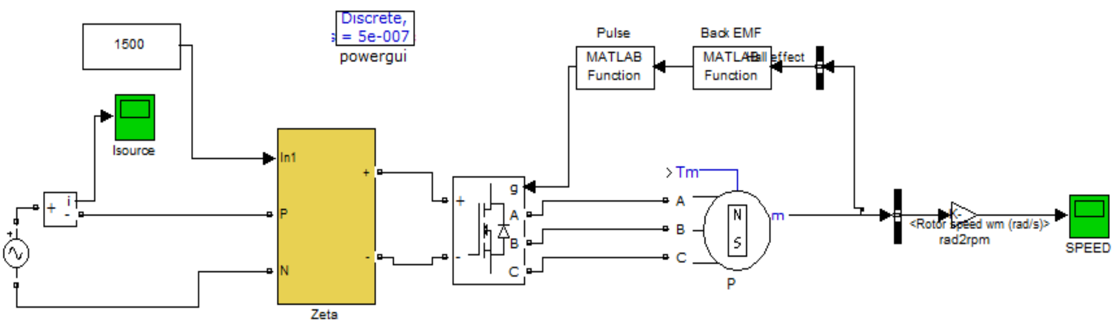

Fig.8 BLDC Motor Drive with Zeta converter for harmonic reduction

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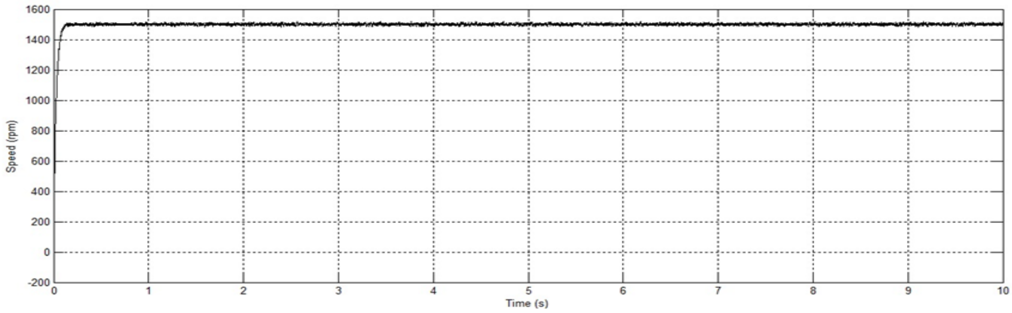

Fig.9 Speed Control of BLDC Motor Drive with Zeta converter

Fig.9 shows the speed wave form of the VSI fed BLDC motor. Here the speed is controlled at 1500 rpm. The motor speed is derived from the position inputs and is compared with the speed reference to generate the current references.

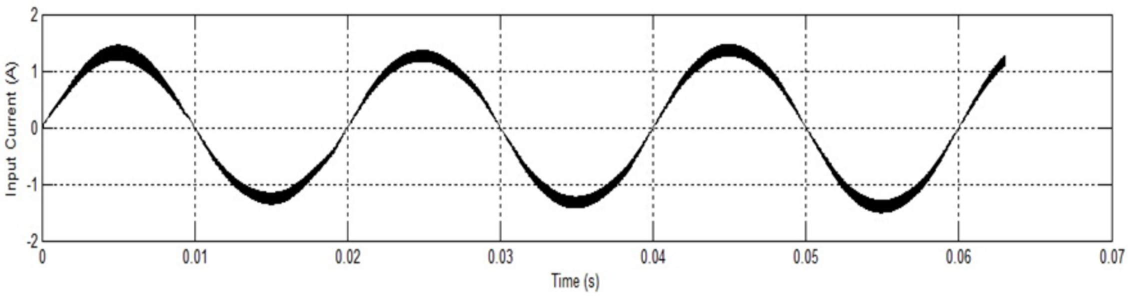

Fig.10 Current waveform at ac mains of Zeta Converter fed BLDC Motor Drive

The input current waveform plotted in Fig. 10 shows the performance improvement achieved by using the proposed Topology. The experimentally measured harmonics of the input current is shown in Fig.11.

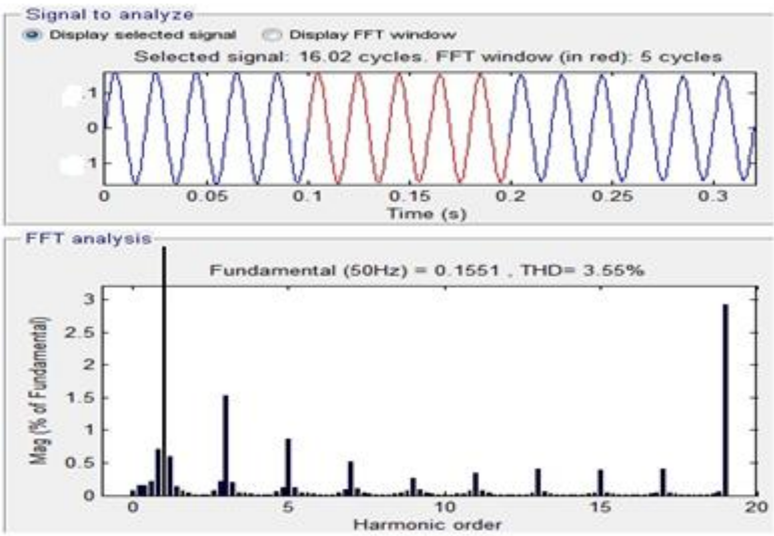

Fig.11 Harmonic Spectra of BLDC Motor Drive with PFC converters

Due to the presence of fuzzy controlled power factor correction converter in BLDC motor drive the total harmonic distortion has been reduced to 5.83% which is shown in the Fig. 11.

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5.3 INFERENCE

System Specification	THD
BLDC Motor Drive without Zeta Converter	88.85%
BLDC Motor Drive with Fuzzy Controlled Zeta Converter	5.83%

VI.CONCLUSION

A fuzzy controlled zeta converter-fed BLDC motor drive has been proposed for targeting low-power household appliances. A variable dc link voltage of VSI feeding BLDC motor has been used for controlling the speed. With this PFC converter, three-phase VSI has been operated in low frequency switching mode with reduced switching losses. An isolated zeta converter operating in DCM has been used for dc link voltage control and with PFC at ac mains. Performance of proposed drive has been found quite satisfactory for speed control over a wide range. The simulated results shows improved performance of the proposed Zeta converter fed BLDC Motor drive in terms of low THD of supply current and improved power quality at the AC mains.

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