ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 12, December 2015

Design of Wishbone Point to Point Architecture and Comparison with Shared Bus

Archana Bharti[1], Ayoush Johari[2], Soni Changlani[3]

M.Tech Scholar, Dept. of ECE, LNCTS, Bhopal, M.P, India[1]

Assistant Professor, Dept. of ECE, LNCTS, Bhopal, M.P, India[2]

Professor, Dept. of ECE, LNCTS, Bhopal, M.P, India[3]

ABSTRACT: System on chip is integration of multimillion transistors in single chip for reducing the cost of design. With the new level of integration the System on Chip design is methodology where intellectual property blocks combined on single chip and allow huge chips to be design at acceptable cost and quality. Hence a standard interface bus protocol is required to increase the productivity with design time reduction. Wishbone is flexible System on Chip bus architecture, connecting IP cores together and alleviating System on Chip integration problems. Wishbone can communicate over variety of devices.

Motivated by this, this paper presents different feature of wishbone bus interface. TheSoC design with DMA master cores and memory slave cores using wishbone point to point interconnection and shared bus interconnection scheme has been designed in Xilinx 12.3. This paper investigates and compare wishbone interconnection point to point and shared scheme.

KEYWORDS: Point to point, Shared bus,SoC,Wishbone, Xilinx.

I. INTRODUCTION

The system on chip design by wishbone interface brought a revolution in modern electronics industry by alleviating various integrations issues. This flexible design is methodology for use with semiconductor IP cores and to reduce SoC design time. With the use of standard wishbone interconnection schemes, the cores are integrated more quickly and easily and with an improvement in design efficiency. Hence it leads to reduction in SoC design time.

The wishbone is system on chip bus used to create a flexible interface that is cornerstone for both FPGA and ASIC. This supports both VHDL and VERILOG hardware description language.

Motivated by this, two types of system have been designed using wishbone point to point and shared bus interconnection scheme in Xilinx Spartan6. Finally the comparison of wishbone interconnection: point to point and shared bus interconnection is done.

The rest of this paper is compiled as follows: Proposed system architecture by using wishbone point to point and shared bus interconnection is presented in section II. The system design result of point to point and shared bus interconnection is presented in section III. Comparison of two proposed system architecture is presented in section IV. And conclusion is drawn in section.

II. PROPOSED SYSTEM ARCHITECTURE

A. POINT TO POINT INTERCONNECTION

The system design using point to point interconnection includes SYSCON, DMA and Memory cores. These cores are available in the Wishbone public domain library for VHDL [15]. The fig.1 shows the system design architecture using point to point wishbone interconnection.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 12, December 2015

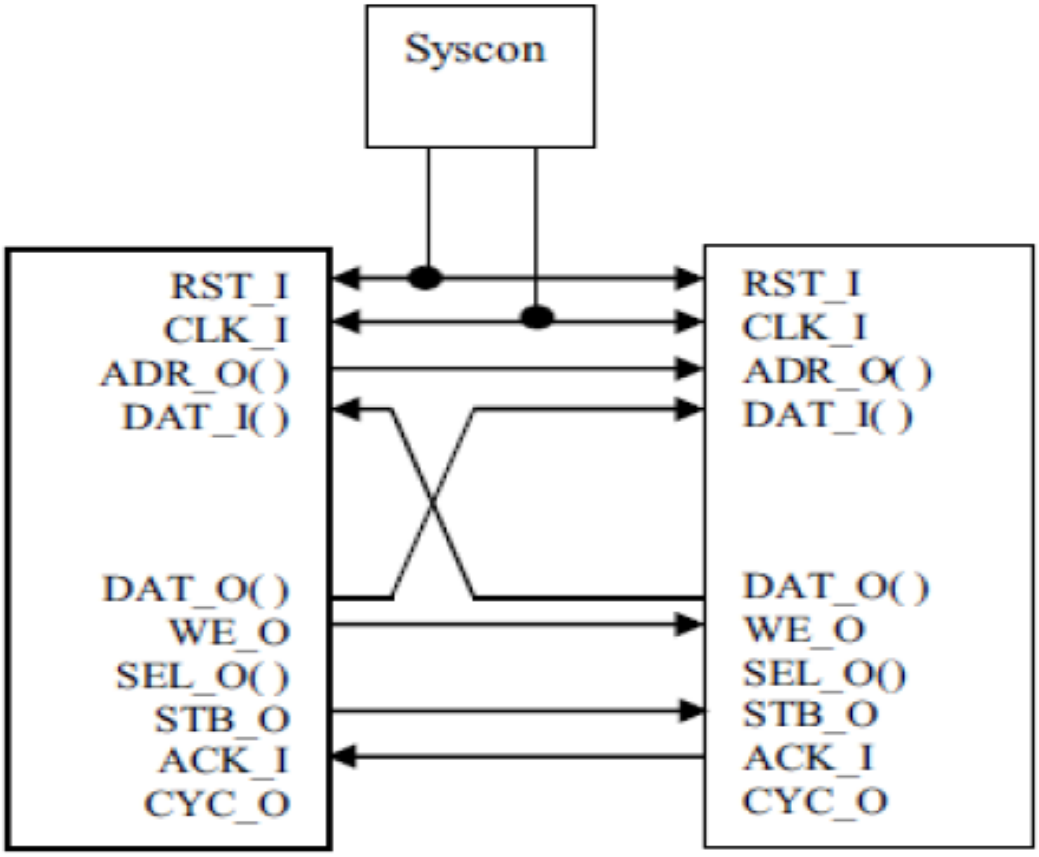

Fig.1Proposed point to point interconnection system architecture

The DMA is 32 bit unit as master interface of WISHBONE. It support two data transfer methods that is single read/write cycles and block read/write cycles. The cycle type is selected by DMODE signal. For single read/write cycle DMODE input is negated and for block read/write cycle DMODE input is asserted.

The memory is 8x32 bit size memory module as slave interface of wishbone. It supports single read/write, block read/write and RMW cycles [15]. To create ram element Xilinx core generator tool is used.

The SYSCON generate clock and reset signals compatible for wishbone point to point system.

B. SHARED BUS INTERCONNECTION

The system design using shared bus interconnection includes SYSCON, four DMA, four Memory cores and these are connected to each other by wishbone interface. The fig. 2 shows the system design architecture using shared bus wishbone interconnection.

The DMA, SYSCON and memory are describes earlier. To grant the access to master the arbiter core is used. It is four level round robin arbiter.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 12, December 2015

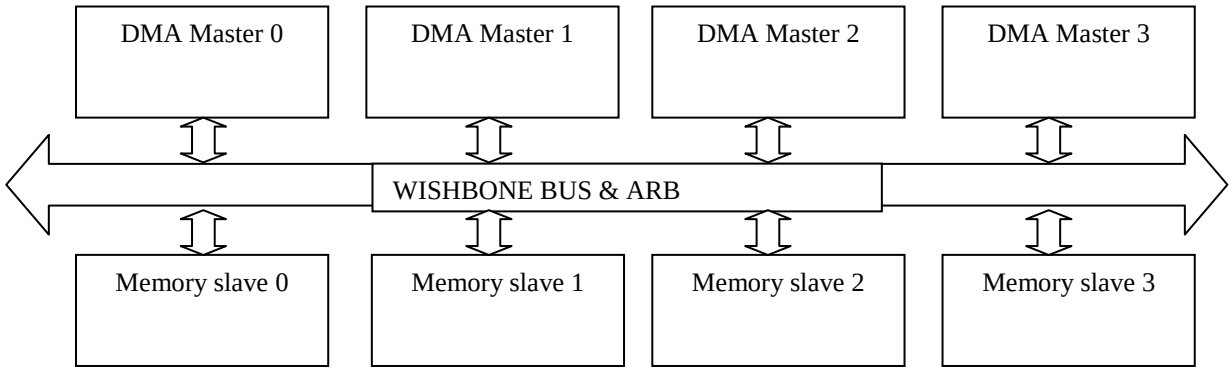

Fig.2 Proposed shared bus interconnection system architecture.

III. SYSTEM DESIGN IN XILINX-RESULT

The two type of system design by two architectures that is point to point and shared bus done in XILINX Spartan6. The fig. 3 shows the point to point system design in Xilinx Spartan6. The table 1 shows point to point system design result. The fig. 4 shows the shared bus system design in Xilinx Spartan6. The table 2 shows shared bus design result.

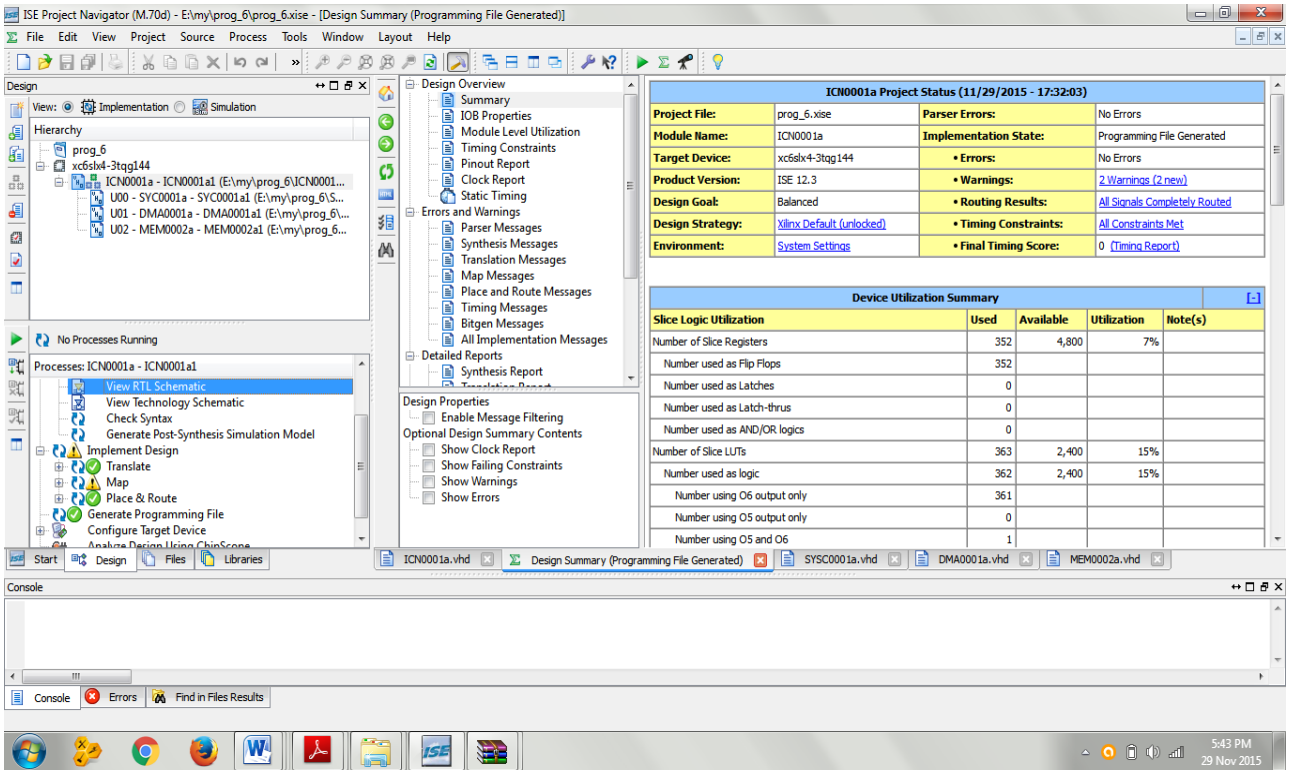

Fig. 3 Point to point system design

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 12, December 2015

Table 1
Point to point system design result

DEVICE TYPE	xc6slx4-3tqg144 (spartan6)
No. of slices registers used	352
No. used as flip flop	352
No. of slice LUTs	363
No used as logic	362

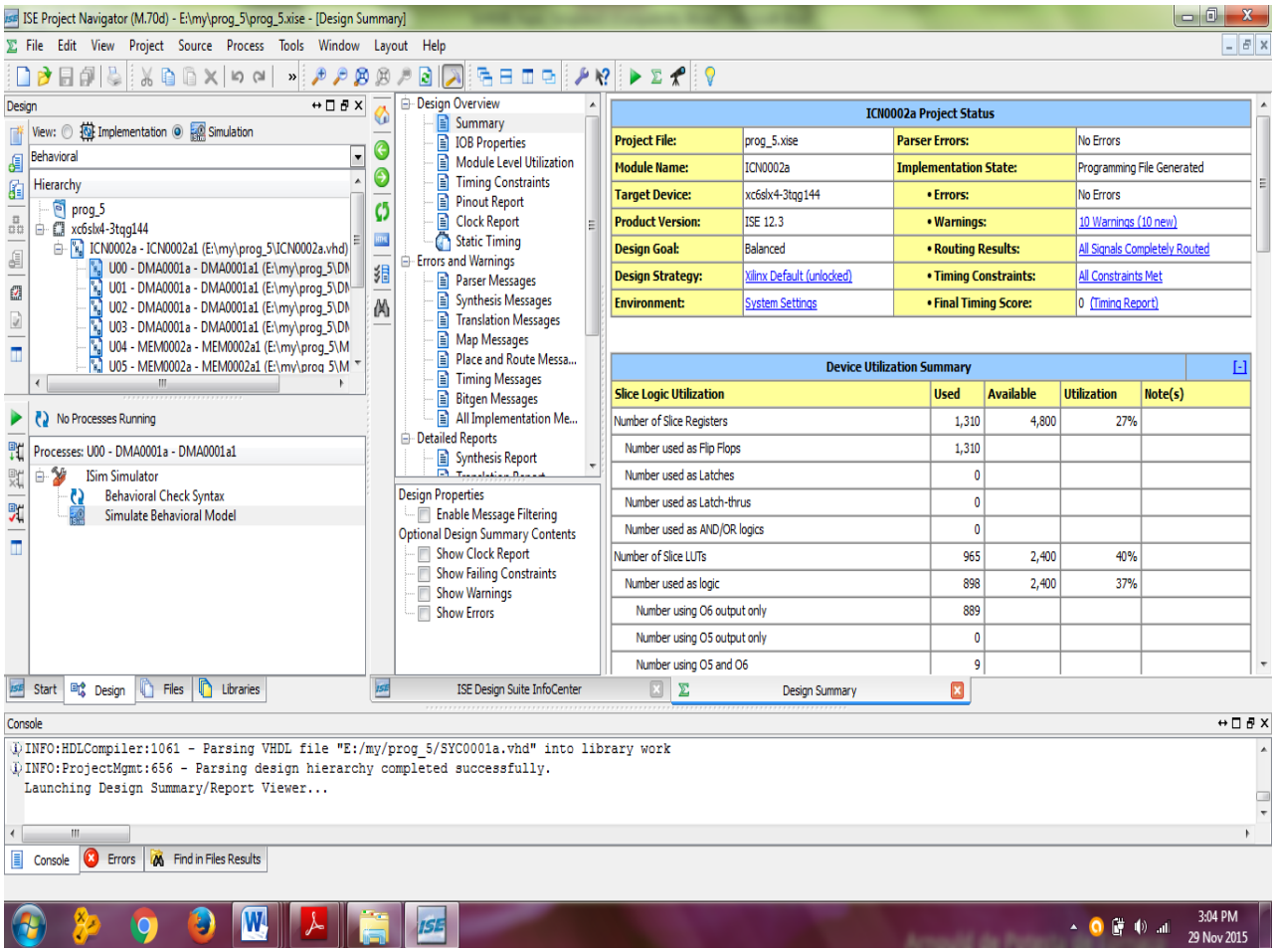

Fig.4 System design using shared bus interconnection

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 12, December 2015

The table 2
Shared bus system design result

DEVICE TYPE	xc6slx4-3tqg144 (spartan6)
No. of slices registers used	1310
No. used as flip flop	1310
No. of slice LUTs	965
No used as logic	898

IV.COMPARISON OF WISHBONE INTERCONNECTION

The table.3showthe wishbone interconnection comparison of point to point and shared bus on the design basis.

Table. 3
Comparison of wishbone interconnection

S.NO	POINT TO POINT INTERCONNECTION	SHARED BUS INTERCONNECTION
1.	In point to point interconnection involves direct connection of two participants that transfer data with each other.	In shared bus interconnection many masters and slaves shared the bus with each other.
2.	In this a single master has direct connection to single slave.	In this many masters has connection to many slaves however only one master at a time can use the bus and other masters has to weight foe their turn.
3.	It consist of SYSCON core, one DMA as master and one Memory as slave	It consists of SYSCON cores, more than one DMA as master and more than one Memory as slave.
4.	The interconnection design is direct connection of master core and slave core and simple to design.	The system design is much more complex and imposes design complexities to system integrator during SoC integration.
5.	No arbiter is needed	An arbiter is needed

V. CONCLUSION

A 32 bit system is designed by point to point and shared bus interconnection. The minimum size required for implementing point to point interconnection system is116 and shared bus interconnection system is 465 slices. The total logic elements required for implementing point to point interconnection system is 362 and for shared bus interconnection system the total logic elements required 898. The two wishbone interface systems are design by two interconnection architectures point to point and shared bus. Hence a portable, low cost SoC can be design successfully.

REFERENCES

1. D. Shanthi, R.Amutha, "Design Approach to Implementation of Arbitration Algorithm In Shared Bus Architectures (MPSoC)," IISTE vol 2, No. 4, 2011
2. Mohandeep Sharma and Dilip Kumar, "Wishbone Bus Architecture-A Survey and Comparison," International Journal of VLSI Design and Communication System (VLSICS) vol. 3, No. 2, April 2012
3. MilicaMitic and Mile Stojev, "A Survey of three System On Chip Buses: AMBA, Core Connect and WISHBONE," ICEST 2006

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 12, December 2015

4. Bharath S.V., Ashwini S. Shivannavar, and M.Z. Kurian,"Design of Efficient SoC Bus Based on Wishbone," International Journal of Innovative Technology and Exploring Engineering (IJITEE), ISSN: 2278-3075, vol. 3, Issue 1, June 2013
5. ChandralaBrijesh A., Mahesh T. Kolte, "Design and Verification Point to Point Architecture of Wishbone Bus for System On Chip," International Journal of Emerging Engineering Research and Technology, volume. 2, Issue 2, May 2014, pp 155-159
6. N. Vivekanandan, AbhilashGunaki, ChinmayaAcharya, Savio Gilbert and RushikeshBodake, "Design, Analysis and Simulation of Double Wishbone Suspension System," IPASI International Journal of Mechnical Engineering (IIJME), volume 2, Issue 6, June 2014
7. G. Prasad and N. Vasantha, "Integrating a PCI IP Core to FPGA Design and Implementation," International Journal of Engineering and Advance Technology (IJEAT), ISSN: 2249-8958, Volume 3, Issue 1, October 2013.
8. Richard Herveille, WISHBONE System-on- Chip (SoC) Interconnection Architecture for Portable IP Cores, rev. version: B4, 2010. By Open Cores Organization, p.7, 2010
9. SimranRana and Rajesh Mehra, "Design and Simulation of RISC Processor using Hyper Pipeling Technique," IOSR Journal of Mechnical and Civile Engineering (IOSR-JMCE), e-issn: 2278-1684, P-ISSN:2320-334X, volume 9, Issue 3 (sep-oct 2013), pp 49-57
10. Ahmed H. M. Soliman, E.M. Saad, M. EI Bably, and Hesham M. A. Keshk, "Designing a Wishbone Protocol Network Adapter for an Asynchronous Network On Chip," IJCST International Journal of Computer Science Issue, vol. 8, Issue 4, No. 2, July 2011, ISSN (online) : 1694-0814
11. Ho W.H. and Pinkston T.M., "A Design Methodology for Efficient Application-specific on-chip interconnects," IEEE Trans. Parallel Distributed System, 17(2), pp. 174-179, February 2006
12. ResveSaleh and Steve Witton, "System On Chip Reuse and Integration," Proceedings of the IEEE, vol. 94, NO. 6, pp 1050-1069 June 2006
13. Gajski, D.D; Wu, A.C-H; Chaiyakul, V.; Mori, S.; Nukiyama, T. and Bricoud, P., " Essential Issues for IP Reuse," Design Automation Conference 2000 Proceedings of the ASP-DAC, Asia and South Pacific pp. 111-114, 2000
14. PrasunGhosal, MalabikaBiswas, and Manish Biswas, Proceedings of the2010 International Conference on Industrial Engineering and Operation Management Dhaka, Bangladesh, January 9-10, 2010
15. AyasKanta Swain, Kamala Kant Mahapatra, "Design and Verification of Wishbone Bus Interface for System On Chip Integration," 2010 Annual IEEE India Conference(INDICON)
16. KyeongKeolRyu, Shin, and Vicent J. Mooney, "A Comparison of Five Difference Multi Processor SoC Bus Architectures, "Digital Systems Design," Proceedings Euro Micro Symposium, Warsaw, Poland, p.209, sept. 2001.
17. Wishbone System On Chip (SoC) Interconnection Architecture for Portable IP Cores, rev. version: B4, p. 92, 2010
18. Richard Herveille, "Combining Wishbone Interfaces Signals Application note," Rev. 0.2 Preliminary, p.2, April 18, 2001, Available Online at
19. http://cdn.Opencores.org/downloads/appnote-01. Pdf
20. Richard Herveille, "WISHBONE System-on-Chip (SoC) Interconnection Architecture for Portable IP Cores," Specification Rev. B3, September 7, 2002.
21. Wishfaq.htm Silicore Corporation p.4, page updated: March 18, 2002.