A High Step up Converter for Grid Connected Photovoltaic Generation System

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ABSTRACT:A high step up converter is proposed for grid connected photovoltaic generation system.An asymmetrical interleaved technique is proposed for high step up gain with high efficiency.A high step-up converter adopts boost converter with interleaved mode and a coupled inductor to increase its step-up voltage ratio. The interleaving technique connects the converter in parallel to share the power flow, this reduce the size , weight, and volume of the inductors and capacitors.Without using of high duty ratio this converter achieves a high step-up voltage-conversion ratio through a coupled inductor and the converter. The boost converter is placed in the first phase to achieve a higher voltage conversion ratio. This two phase formation is used to reduce the current stress, current ripple and also the conduction losses of metal oxide semiconductor field effect transistors (MOSFET). The Conversion efficiency is high because the leakage inductances are recycled to the output terminal. The main requirements of this Pv application is small ripples in the generator and load as well as high voltage conversion ratio.

KEYWORDS: Boost converter, MOSFET, coupled inductor, Photovoltaic system.

I.INTRODUCTION

Renewable energy attracts interest for power generation because the non renewable energy like petrol, diesels etc are diminishing and energy crisis is an important concern in most of the nations.In renewable energy, solar energy attracts more because it has more advantage compare to other renewable energy s like the selection of area is not complicated, the systems can either be operated as isolated systems or connected to the grid as a part of an integrated system, it has no moving parts; it has a long lifetime and low maintenance requirements and most importantly it is one solution that offers eco friendly power [11]. Photovoltaic system requires a power electronics interface to be connected to the grid. The most commonly used dc/dc converter is a boost converter which provides an acceptable voltage conversion ratio and also requests a continuous current from the power source [1]. The characteristics required in photovoltaic applications are low current ripple injected to the power source and high conversion efficiency. In the photovoltaic case, the current ripple impacts the power generation since it produces an oscillation around the Maximum Power Point (MPP) reducing the energy extracted from the photovoltaic generator [9]. Those characteristics make the boost converter a good candidate to interface the photovoltaic systems. Additionally it requires filter between the power generator and the power converter, increasing also the power losses, size, weight, cost and order of the system. Another possibility to reduce the converter's input current ripple is given by the interleaving structures.

The interleaving technique connects dc/dc converters in parallel to share the power flow between two or more conversion chains.However, the conventional interleaved converter has some disadvantages like the duty ratio is extremely large in order to get a high gain, this increases the current ripple, conduction losses and the turnoff losses. Then, the switches voltage stress is the high and the output diode reverse-recovery problem is very severe, which induces additional voltage and current stresses and losses and also the electromagnetic interference (EMI) noise is very serious.To improve voltage gain interleaved structures can be used with transformers or the inductors [12]. Interleaved converters is able to reduce output current ripple without any modification on the PWM technique (need phase shift only) and circuit theory of boost converter [12]-[15]. When the duty cycle is high the voltage gain is theoretically infinite. So the switch turn on period becomes long as the duty cycle (D) increases causing conduction losses to increase. The single switch boost converter power rating is limited to switch rating [12]. Interleaved parallel topology is the solution to increase the power and reduce input current ripple allowing lower power rated switches to be used.

II.PROPOSED SYSTEM MODEL AND ASSUMPTIONS

The Fig 1 shows the circuit configuration of the proposed an asymmetrical interleaved converter with voltage multiplier cell. The voltage multiplier module of the proposed converter is composed of coupled inductor, the conventional boost converter and a voltage-lift capacitor[20]. This capacitor offers an extra voltage conversion ratio. The leakage energy of the coupled inductor is recycled to the output capacitors the turns ratio of coupled inductors can be designed to enlarge voltage gain. The number of multiplier can be adjusted to get a desired duty ratio; a higher boost rate is easily obtained from the voltage multiplier [13]. The coupling coefficient of the coupled inductor is denoted by "." And "*".The equivalent circuit of coupled inductor include the magnetizing inductor Lm, Lk. This proposed converter consist of the dc input voltage Vin, two power switch S1 and S2, four diodes D1, D2, D3, D4 and four capacitors C1, C2, C3, Cb. Primary winding of the couple inductor turn is Np1 and the secondary winding of the turn is Ns2.

The Proposed system advantages are:
1) The converter is characterized by a low input current ripple and low conduction losses, making it suitable for high-power applications;
2) The converter achieves the high step-up voltage gain that renewable energy system.
3) Leakage energy is reuse and sent to the output terminal, and ease large voltage spikes on the main switch
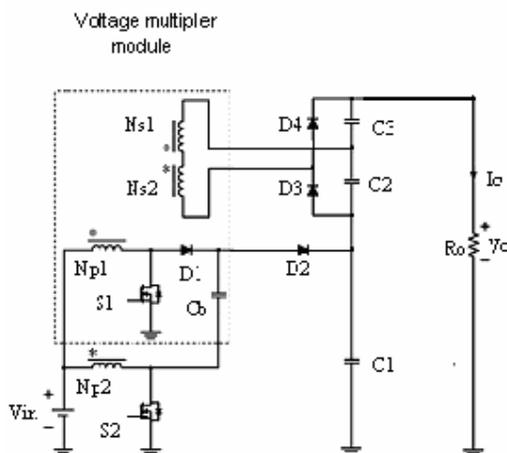4) The main switch voltage stress of the converter is considerably lower than that of the output.

Fig. 1 Proposed system circuit diagram

III .PRINCIPLE OF OPERATION

A voltage multiplier is an electrical circuit that converts electrical power from a lower voltage to a higher voltage. Module, which is stacked on a boost converter to form an asymmetrical interleaved structure [14]. Primary windings of the coupled inductors with np turnsare employed to decrease input current ripple, and secondarywindings of the coupled inductors with ns turns are connected in series to extend voltage gain. The turns ratios of the coupled inductors are the same.

The proposed converter operates in continuous conduction mode (CCM), and the duty cycles of the power switches during steady operation are interleaved with a 180◦ phase shift; the duty cycles are greater than 0.5 conventional interleaved boost converter [15]. Interleaved structure is employed in the input side to reduce the input current ripple and improve the power level.

The voltage multiplier cell is placed in the output side to achieve a high step up voltage gain and simplify the circuit structure. Moreover, the switch voltage stress is reduced as the turns ratio of the coupled inductors increases. The

output voltage is changed as load shift and the detected feedback signal is processed via proportional-integral controller, and the internal comparator generates interleaved PWM with a 180◦ phase shift**.**The key steady waveforms in one switching period of the proposed converter contain six modes

IV.MODES OF OPERATIONS

Mode1 [t0, t1]:
At t=t0 , the S1 and S2 both switches areturned on ,all the diodes are get reversed-biased . The magnetizing inductors Lm1 , Lm2 and the leakage inductorsLk1, Lk2 are linearly charged by the input voltage sourceVin ,the circuit is shown in fig 2.(a)
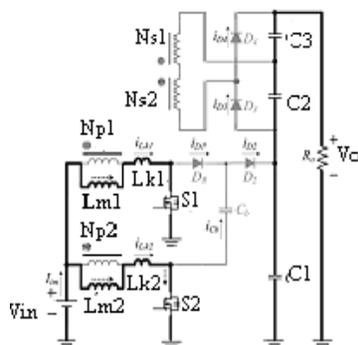

Fig 2.(a) Mode 1 [t 0 , t 1].

Mode 2 [t 1 , t 2]:
At t= t1, the power switch s2 is switchedoff, thereby diodes D2 and d4 is turned on. The energy stored in themagnetizing inductor Lm2 is transferred to the secondary side, this charging the output filter capacitor C3. The inputvoltage source, magnetizing inductor Lm2 , leakage inductorLk2 , and voltage-lift capacitor Cb release energy to the outputfilter capacitor c1 through diode D2 , thereby extending the voltageon C1.The circuit is shown in fig 2.(b).
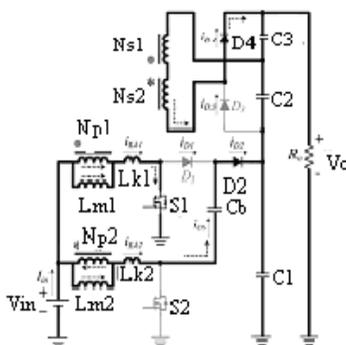

Fig. 2. (b). Mode 2 [t 1 , t 2].

Mode 3 [t 2 , t 3]:
At t=t2, the total energy of leakage inductor Lk2 has beencompletely released to the output filter capacitor C1 , the diode D2 automatically switchesoff so there is no reverse recovery problem in the diode. Magnetizing inductor Lm2 transfers energy to the secondary side chargingthe output filter capacitor C3 through the diode D4 until t3. The circuit is shown in fig.2(c).
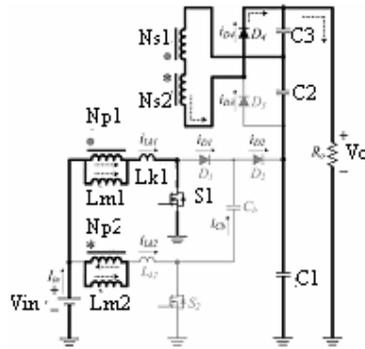
Fig 2.(c) Mode 3 [t 2 ,t 3].

Mode 4 [t 3 , t 4]:
At t= t3, the power switch S2 is switchedon and all the diodes are reversed biased. The magnetic inductance and leakage inductance gets linearly charged by the input voltage Vin. The circuit is shown in fig 2.(d). This mode 4 is similar to mode 1.
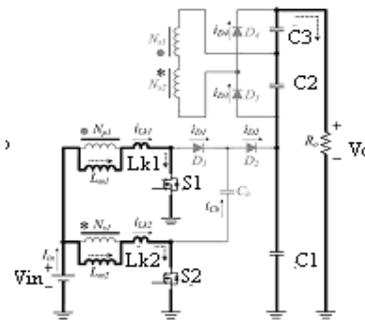

Fig 2.(d) Mode 4 [t 3 ,t 4].

Mode 5 [t 4, t 5]:
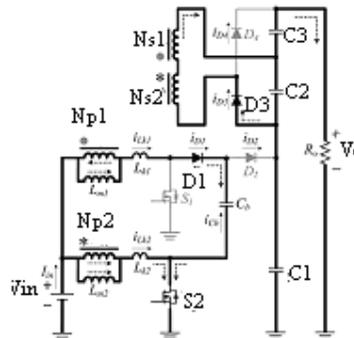At t=t4, the power switch S1 is switchedoff, which turns on diodes D1 and D3.The energy stored in magnetizing

Fig.2.(e) Mode 5 [t 4 , t 5].

magnetizing inductor Lm1 is transferredto the secondary sidecharging the output filter capacitor C2. The input voltage source and magnetizing inductor Lm1 release energy to voltage-lift capacitor Cb via diode D1, which stores extra energy in Cb. This mode of operation is shown in fig 2. (e)

Mode 6 [t 5, t 0]:

At t = t5, the total energy of leakage inductor Lk1 has been completely released to voltage-lift capacitor Cb, so the diode D1 is automatically turned off . Magnetizing inductor Lm1 transfers energy to the secondary side charging the output filter capacitor C2 via diode D3 until t0.
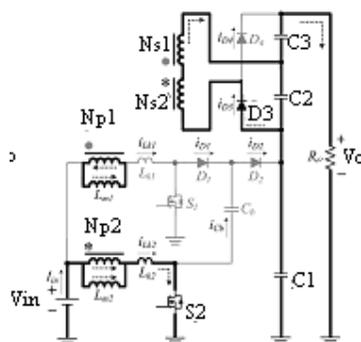

Figure 2.(f). Mode 6 [*t* 5 , *t* 0].

V. SIMULATION RESULT AND DISCUSSION

The circuits are simulated in MATLAB software. The circuit simulation of high step up converter and the output waveforms are shown in fig 3and fig 4 respectively .In the proposed high step up converter 380-V output s obtained for 40-V input. The simulation result of the proposed converter is shown in fig 4.

The proposed high step up converter function is based on the components selection and coupled inductor design .The values of the primary leakage inductors of the coupled inductors are set as close as possible for current sharing performance.When the duty cycle ratio is 0.6 , the voltage gain is 10 at a turns ratio n = 1, but the gain reaches 10 at a turns ratio n = 5. The efficiency of the proposed converter is 96.8% at Po=400W at maximum output power the conversion efficiency of the converter about 96.1%. The performance of the proposed converter is compared with the other interleaved converters introduced in [13] and [14] as shown Table 2.

Components	Symbols	Parameter
Magnetizing inductances	Lm1,Lm2	1.33
Leakage inductance	Lk1,Lk2	1.6
Turns ratio	N(Ns / Np)	1
Power switches	S1,S2	IRFR 4227
CAPACITORS	Cb, C2, C3	220
	C1	470

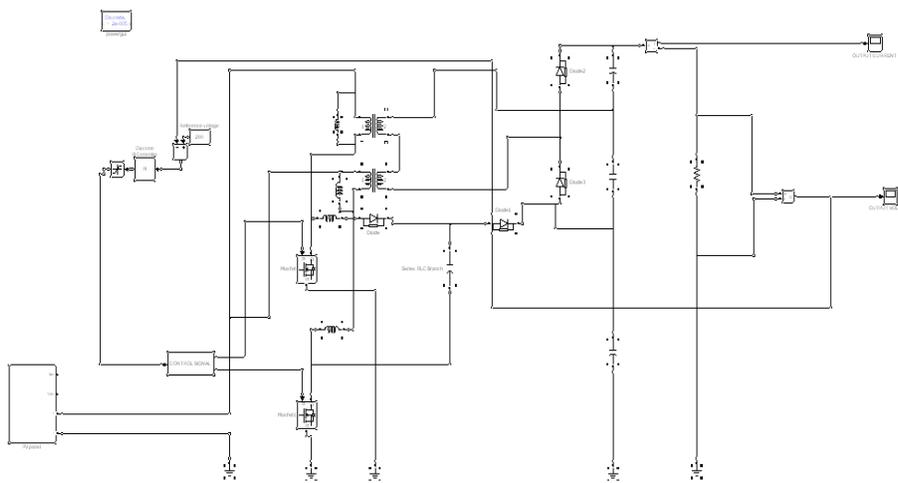Table 1.Converter components and Parameter

Fig 3.Simulation Diagram of Proposed System
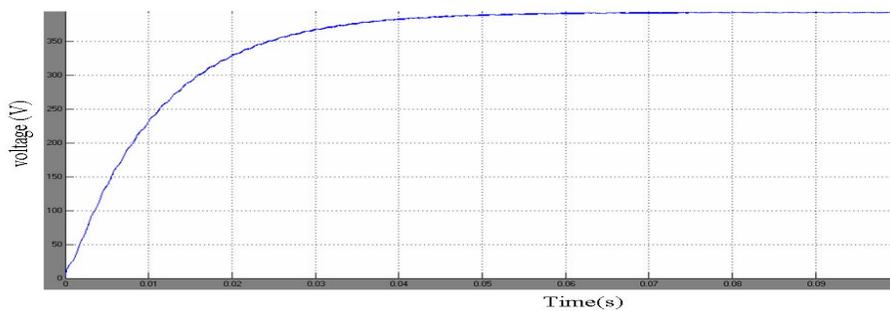
Fig 4.Simulation Output of high step up converter

INTERLEAVED CONVERTER	CONVERTER IN [14]	CONVERTER IN [13]	PROPOSED CONVERTER
Voltage gain	2/(1-D) + nD	2(n+1)/(1-D)	2(n+1)/(1-D)
Quantities of diodes	4	6	4
Quantities of cores	3	2	2
Quantities of secondary side winding	1	2	1

Table 2.Performance comparison of interleaved high step up converter

VI.CONCLUSION

This work done has presented the topological principles, and simulation results for a proposed converter. The proposed converter has been successfully implemented in an efficiently high step-up conversion without an extreme duty ratio and a number of turns ratios through the voltage multiplier module and voltage clamp feature. The interleaved PWM scheme reduces the current that pass through each power switch and constrained the input current ripple by approximately 6%. The experimental results indicate that leakage energy is recycled through capacitor *Cb* to the output terminal.The voltage stresses over the power switches are restricted much lower than the output voltage (380V). These switches, conducted to low voltage rated and low on-state resistance MOSFET, can be selected. From the aforementioned workdone, the major challenges are as follows:

1) how to extend the voltage gain and how to avoid the extreme duty cycle to reduce the current ripple;
2) how to reduce the switch voltage to make low-voltage MOSFETs available to re duce the power device cost and conduction losses;
3) how to realize the soft switching performance to reduce the switching losses;
4) how to alleviate the output diode reverse recovery problem to reduce the reverse recovery losses.

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