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A Hybrid Cascaded Multilevel Inverter for Interfacing with Renewable Energy Resources

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Abstract: A cascaded multilevel inverter and hybrid cascaded multilevel inverter characteristics is to be observed in this paper. The main objective of this paper is to propose an alternative topology of hybrid cascaded multilevel inverter applications. In this paper the different parameters (like voltage, THD) are going to observed by using hybrid cascaded multilevel inverter. The modified PWM technique is developed to reduce switching losses and also, the proposed topology can reduce the number of power switches compared to a traditional cascaded multilevel inverter. Simulink/MATLAB is used to simulate the circuit operation and for control signal.

Index Terms: H-Bridge Inveter, Thd, PWM Technique.

I. INTRODUCTION

A renewable energy application such as photovoltaic (PV) system has been widely used for a few decades since PV energy is free, abundant and distributed throughout the earth. The focus of the Engineers is to make use of abundantly available PV energy and so to design and control an inverter suitable for photo voltaic applications. Power electronic circuits with pulse width modulation (PWM) are mostly used in energy conversion systems to achieve closed loop control. But even updated pulse width modulation (PWM) techniques do not produce perfect response which strongly depend on the semiconductors switching frequency. Also, it is well known that distorted voltages and currents waveforms produce harmonic contamination, additional power losses, and high frequency noise that can affect not only the load power but also the associated controller.

This paper focuses to analyze the performance of single phase CHB multi level inverter with photovoltaic cell as its input source from 5 to 15 levels. The performance parameters are harmonics contents, number of switches and voltage stress across the switch. The effect of symmetrical/asymmetrical topology and change in PV input parameters-irradiation/temperature on the performance parameters is also analyzed.

II. MULTI-LEVEL INVERTERS

Modern electric devices are usually fed by diode or thyristors front-ends. Such equipment generates higher harmonics into a grid. Now days those problems are going more and more serious. Grids disturbances may result in malfunction or damage of electrical devices [1]-[3]. Therefore, currently many methods for elimination of harmonic pollution in the power system are developed and investigated. Restrictions on current and voltage harmonics maintained in many countries are associated with the popular idea of "clean power [4]- [5].The PWM rectifier advantages are Bi-directional power flow, Nearly sinusoidal input current, Regulation of input power factor to unity, Low harmonic distortion of line current (THD below 5%), Adjustment and stabilization of DC-link voltage (or Current), Reduced capacitor (or inductor) size due to the continuous current [6]-[7].

Recent advances in the power-handling capabilities of static switch devices such as IGBTs with voltage rating up to 4.5 kV commercially available, has made the use of the voltage source inverters (VSI) feasible for high-power applications. High power and high-voltage conversion systems have become very important issues for the power electronic industry handling the large ac drive and electrical power applications at both the transmission and distribution levels.

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A new family of multilevel inverters has emerged as the solution for working with higher voltage levels. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms.

A. H – Bridge Inverter

"H" topology has many redundant combinations of switches' positions to produce the same voltage levels. As an example, the level "zero" can be generated with switches in position S(1) and S(2), or S(3) and S(4), or S(5) and S(6), and so on.Another characteristic of "H" converters is that they only produce an odd number of levels, which ensures the existence of the "0V" level at the load .For example, a 51-level inverter using an "H" configuration with transistor-clamped topology requires 52 transistors, but only 25 power supplies instead of the 50 required when using a single leg. Therefore, the problem related to increasing the number of levels and reducing the size and complexity has been partially solved, since power supplies have been reduced to 50%.

The full-bridge topology is used to synthesize a three-level square-wave output waveform. The half-bridge and full-bridge configurations of the single-phase voltage source inverter are shown in Fig. (a) and Fig. (b), respectively.

(a) (b)

Fig.1 Converter topologies (a) Half Bridge Inverter (b) Full Bridge Inverter

B. Bridge Inverter

To generate zero level in a full-bridge inverter, the combination can be S1 and S2 on while S3 and S4 off or vice versa. The three possible levels referring to above discussion are shown in Table 1.

Table 1: Switching pattern of 3 level full bridge inverter

Conducing Switches	Load Voltage V_{AB}
S_1,S_4	+Vs
S_2,S_3	-Vs
S_1,S_2 or S_3,S_4	0

III. MULTILEVEL INVERTER STRUCTURES

A voltage level of three is considered to be the smallest number in multilevel converter topologies. Due to the bi-directional switches, the multilevel VSC can work in both rectifier and inverter modes. This is why most of the time it is referred to as a converter instead of an inverter in this dissertation. A multilevel converter can switch either its input or output nodes (or both) between multiple (more than two) levels of voltage or current.

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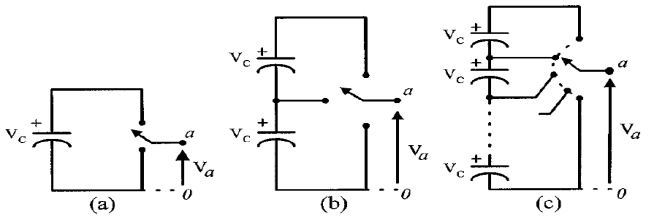

Fig. 2 One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels.

IV. CLASSIFICATION OF MULTILEVEL INVERTERS

In General, the multilevel inverters are classified as Single DC source and Multiple DC sources or Several Separate DC Sources (SDCS). Both the Diode Clamped Multilevel Inverter and the Flying Capacitor inverter comes under the category of Single DC source where the input supply is taken from a single DC source. Classification of multilevel inverters shown in fig.3

V. MODULATION TOPOLIGIES FOR MULTI LEVEL INVERTERS

Mainly the power electronic converters are operated in the "switched mode". Which means the switches within the converter are always in either one of the two states - turned off (no current flows), or turned on (saturated with only a small voltage drop across the switch). Any operation in the linear region, other than for the unavoidable transition from conducting to non-conducting, incurs an undesirable loss of efficiency and an unbearable rise in switch power dissipation. To control the flow of power in the converter, the switches alternate between these two states (i.e. on and off).

Any technique can probably be placed into one of the following three categories:

1) Off-line or pre-calculated PWM technique
2) Hysteresis control PWM
3) Carrier based PWM.

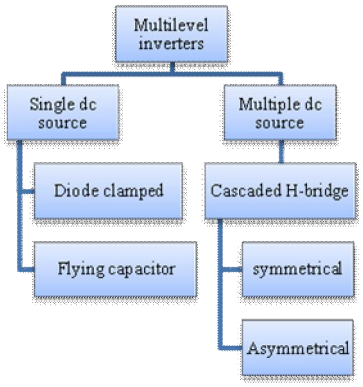

Fig. 3 Classification of multilevel inverters

A. Cascaded H Bridge Inverter

Cascaded Multilevel h-bridge inverters offer several advantages compared to their conventional counterparts. By synthesizing the AC output terminal voltage from several levels of DC voltages, staircase waveforms can be produced, which approach the sinusoidal waveform with low harmonic distortion, thus reducing filter requirements. The need of several sources on the DC side of the converter makes multilevel technology attractive for photovoltaic applications. This paper provides an overview on different multilevel topologies and investigates their suitability for single-phase with constant, variable frequencies & three phase grid connected photovoltaic systems The "multilevel converter" has drawn tremendous interest in the power industry. The general structure of the multilevel converter is to synthesize a sinusoidal

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voltage from several levels of voltages, This paper presents single-phase symmetrical, asymmetrical configuration up to 15 levels & three-phase, five-level and seven level cascaded multilevel voltage source inverter.

Photo Voltaic (PV) power supplied to the utility grid is gaining more and more visibility, while the world's power demand is increasing [1]. Not many PV systems have so far been placed into the grid due to the relatively high cost, compared with more traditional energy sources such as oil, gas, coal, nuclear, hydro, and wind. Solid-state inverters have been shown to be the enabling technology for putting PV systems into the grid.

With the advancement of power electronics and emergence of new multilevel converter topologies, it is possible to work at voltage levels beyond the classic semiconductor limits. The multilevel converters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the ratings of the individual power devices. Among the multilevel Converters [1-4], the cascaded H-bridge topology (CHB) is particularly attractive in high-voltage applications, because it requires the least number of components to synthesize the same number of voltage levels.

VI. SIMULATION OF PV FED CHB INVERTER

A Five-level to fifteen-level CHB MLIs are simulated in MATLAB-Simulink and a detailed performance analysis is done in terms of harmonic contents, voltage stress across the switches and number of switches needed. Different symmetrical and asymmetrical MLI topologies with RL load are tried out to achieve target output voltage. It shows many combinations of asymmetrical input to get the specified output voltage. Also, number of switches required for the operation and voltage stress across the switches is compared up to 15 levels.

A.PERFORMANCE COMPARISON SYMMETRICAL VS ASYMMETRICAL

To produce the same output voltage two levels, symmetrical and asymmetrical CHB MLI are constructed. Three PV arrays are considered each with output voltage of 32.9V. Two level inverters needs only 4 switches but develops high voltage stress across the switch. Also, THD content is very high (48.02%) as expected. On the other hand, seven level symmetrical CHB inverters requires more number of switches (12) with a minimum voltage stress of 32.9V and minimum THD. In terms of efficiency, Asymmetrical topology is best but with respect to voltage stress and THD its performance is better than 2 levels.

VII. SIMULATION RESULTS

Output Voltage of Five Level Cascaded Symmetrical Single Phase Multilevel Inverter

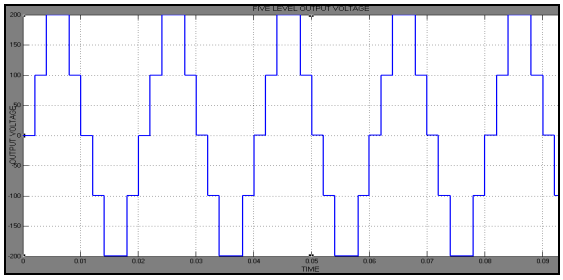

Fig.4 Five level output voltage graph with respect to time.

The magnitude of the output voltage graph is 200V. It is a simple bridge level inverter. in this we are cascading 2- single phase inverter but where as in 5- level inverter.

Advantages:

- To obtain outlet output voltage/current waveforms.
- To get minimum amount of ripple content.
- To get high switching frequency.

THD ANAYLSIS:

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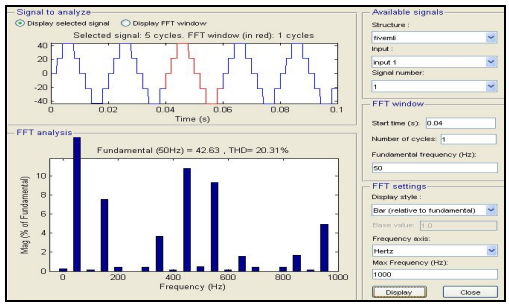

Fig. 5 THD of five level multilevel inverter

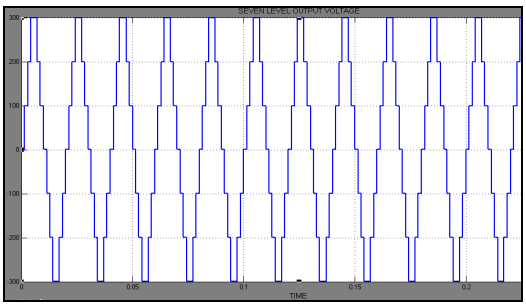

Fig.6 Output Voltage of Seven Level Cascaded Symmetrical Single phase Multilevel Inverter

The above graph represents the THD of the 5 level multilevel inverter. The THD of the 5 MLI is 20.31% at the simulation time of 0.04 to 0.06 at 50Hz frequency for single cycle. Cascaded H Bridge multilevel symmetrical single phase seven level inverter:

3-single phase inverter connected in cascaded H bridge form. We will get 7-level output voltage. The magnitude of output voltage for 7-level H bridge inverter is 300 and +300 to -300 Vpeak to peak.

When compared to 5-level inverter for 7- level inverter we will get less harmonics or ripple distortion due to which we will get partial or pure sinusoidal waveform.

Advantage:

- To obtain ouslity output voltage/current waveforms.
- To get minimum amount of ripple content.
- To get high switching frequency.

THDANALYSIS:

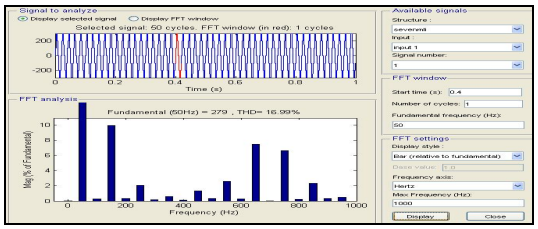

Fig.7 THD of seven level multilevel inverter

The above graph represents the THD of the 7 level multilevel inverter. The THD of the 7 MLI is 16.99% at 50Hz frequency for single cycle. The bar graph shows the related THD of 7 MLI.

Cascaded H Bridge MULTILEVEL ASYMMETRICAL Single phase Nine LEVEL INVERTER:

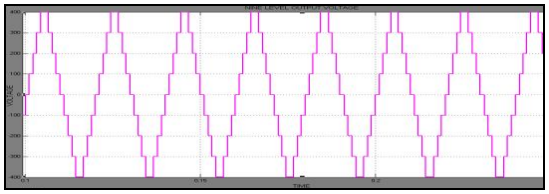

Fig. 8 Output Voltage of Nine Level Cascaded Asymmetrical Single phase Multilevel Inverter.

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This the output voltage graph of 9-level cascaded H bridge single phase multilevel inverter and obtain output 400V and peak to peak voltage is +400V to -400V. Connected four single phase inverter in cascaded manner to get 9-level inverter output

When compared to 7-level inverter for 9 level inverter we will get less harmonics or riple distortion due to which we will get partial or pure sinusoidal waveform.

Advantage:

- To obtain ouslity output voltage/current waveforms.
- To get minimum amount of ripple content.
- To get high switching frequency.

THD ANALYSIS:

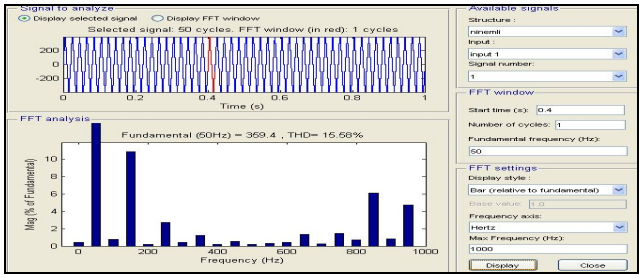

Fig.9 THD of nine level multilevel inverter

The above graph represents the THD of the 9 level multilevel inverter. The THD of the 9 MLI is 15.58% at 50Hz frequency for single cycle. Cascaded H Bridge Multilevel Asymmetrical Single phase Eleven LEVEL INVERTER:

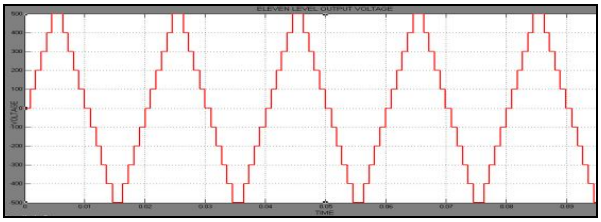

Fig.10 Output voltage of eleven level cascaded a symmetrical single phase multilevel inverter.

Here the same configuration we get eleven level output voltage.

This the output voltage graph of 11-level cascaded H bridge single phase multilevel inverter and obtain output 500V and peak to peak voltage is +500V to -500V

Connected five single phase inverter in cascaded manner to get 11-level inverter output

When compared to 9-level inverter for 11- level inverter we will get less harmonics or riple distortion due to which we will get partial or pure sinusoidal waveform.

Advantage:

- To obtain ouslity output voltage/current waveforms.
- To get minimum amount of ripple content.
- To get high switching frequency.

THD ANALYSIS:

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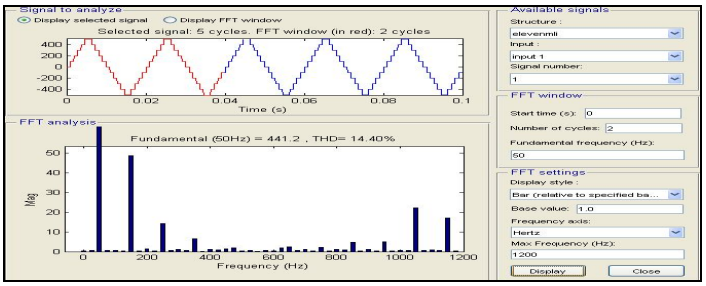

Fig.11 THD of 11 level multilevel inverter

The above graph represents the THD of the 11 level multilevel inverter. The THD of the 11 MLI is 14.40% at the simulation time of 0.0 to 0.04 at 50Hz frequency for two cycles.

Cascaded H Bridge MULTILEVEL ASYMMETRICAL Single phase Fifteen LEVEL INVERTER:

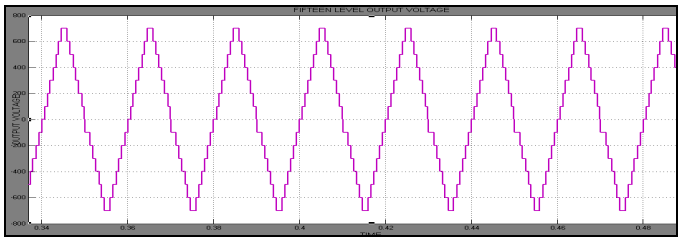

Fig.12 output voltage graph of 15-level cascaded H bridge single phase multilevel inverter

This is the output voltage graph of 15-level cascaded H bridge single phase multilevel inverter and obtain output 700V and peak to peak voltage is +700V to -700V

Connected seven single phase inverter in cascaded manner to get 15-level inverter output

When compared to 11-level inverter for 15- level inverter we will get less harmonics or riple distortion due to which we will get partial or pure sinusoidal waveform.

Advantage:

- To obtain outlet output voltage/current waveforms.
- To get minimum amount of ripple content.
- To get high switching frequency.

THD ANALYSIS:

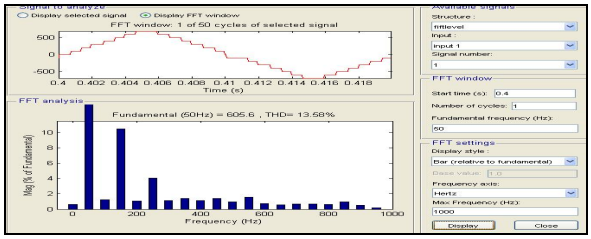

Fig.13 THD of 13 level multilevel inverter

The above graph represents the THD of the 15 level multilevel inverter. The THD of the 15 MLI is 13.56% at 50Hz frequency for single cycle.

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Cascaded H Bridge MULTILEVEL ASYMMETRICAL Three PHASES Five LEVEL INVERTER with Grid connection:

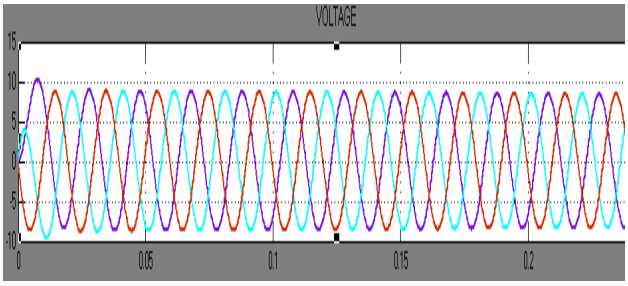

Fig.14 Grid voltage for cascaded H bridge multilevel asymmetrical three phase five level inverter with grid connection

This is a 3- phase grid output voltage across the five level inverter with grid connection.The obtained output voltage across the grid is 10V.

Cascaded H Bridge MULTILEVEL ASYMMETRICAL Three phase Seven LEVEL INVERTER with Grid connection:

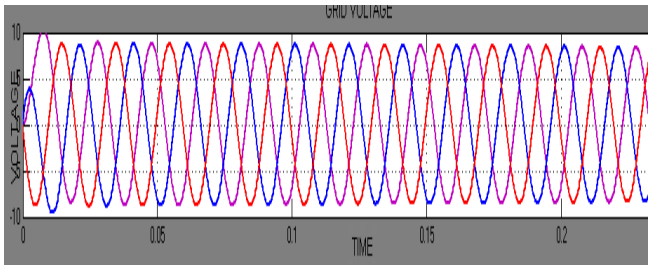

Fig.15 Grid voltage for cascaded H bridge multilevel asymmetrical three phase five level inverter with grid connection

Grid voltage for Cascaded H Bridge Multilevel Asymmetrical Three phase Seven Level inverter with Grid connection shown in fig 15.

This is a 3- phase grid output voltage across the seven level inverter with grid connection. The obtained output voltage across the grid is 10V.The figure shows the Grid voltage for Cascaded H Bridge Multilevel Asymmetrical Three phase Five Level and Seven level inverters with Grid connected Systems.

Table 2. Total harmonic distortion at different levels.

Level	Total Harmonic Distortion (THD)%
5	20.31
7	16.99
9	15.58
11	14.40
15	13.58

VIII. CONCLUSION

Multi level cascaded H bridge inverters from five levels to fifteen levels have been simulated using MATLAB/ Simulink. The result obtained from CHB multilevel inverter (MLI) has low stress, high conversion efficiency and can also be easily

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interfaced with renewable energy sources (PV, Fuel cell etc.). Asymmetrical CHB multilevel inverter uses least number of devices to produce higher voltage level. As number of level increases, the THD content approaches to small value as expected. Thus it eliminates the need for filter. Though, THD decreases with increase in number of levels, some lower or higher harmonic contents remain dominant in each level. From simulation it is observed that the % of THD increases in three phase compare to single phase symmetrical & asymmetrical configurations.

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