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A Low Power High Sensitivity CMOS Multivibrator Based Voltage to Frequency Convertor

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ABSTRACT: This paper presents a low power, high sensitivity CMOS multivibrator based voltage to frequency convertor. Which can be used for analog front-end interfacing of sensors in wireless sensor network applications. The proposed circuit is designed in 180 nm CMOS technology with 1.8V power supply. It operates at input voltage ranges from .6 V to 1.8 V and the output frequency ranges from 94.22MHz to 256.18 MHz. The peak total power consumption observed is 281.2 μW.

KEYWORDS: VFC; analog circuits; low power CMOS design; WSN.

I. INTRODUCTION

Wireless sensor networks (WSNs) constitute the new model of miniaturization exhibiting an ever-increasing broad variety of wireless sensing applications including medical, home security, military, environmental monitoring, chemical biological detection or precision agriculture [1]. Typically, a wireless sensor node consists of sensing, computing, communication, actuation, and power components. Within the field of sensing, today's market is advancing towards the so called smart sensors, i.e. integrated intelligent sensor systems that contain on a single chip microsensors (or microsensor arrays) next to all the related sensor electronics for the signal conditioning, processing and conversion necessary to interface the microcontroller [2].

For the realization of these smart sensor systems, CMOS technology is a preferential choice due to the capability of co integration of sensors and sensor electronics, both analogue and digital. Therefore, at present, research challenges are focused on the implementation of low cost high performance CMOS smart sensors. Furthermore, due to the limitations of power sources, wireless sensor network applications require low voltage, low power electronic circuits to maximize the lifetime of the battery operated systems [4].

In conventional systems, as shown in Fig. 1.1 (a), the sensor signal is converted to the voltage domain and then digitized by means of a standard A/D. Due to the extensive use of microcontroller based measurement systems, voltage to frequency conversion is a suitable alternative to the standard analogue-to-digital (A/D) conversion to digitize the conditioned sensor signal (quasi digital sensors): a frequency output signal can be directly interfaced to the microcontroller, which performs the A/D conversion using its internal timers, as shown in Fig 1.1 (b). This simple approach offers several advantages like high noise immunity, ease of transmission, and high accuracy of the frequency to code conversion [2].

Voltage-to-frequency converters (VFCs) are, by definition, first-order oscillators whose input is an analog voltage Vin and whose output is a frequency signal fo linearly proportional to its input voltage, that is, fo = KVin. There are two common

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VFC architectures: 1. the charge balance VFC and 2. the multivibrator VFC[6] . Their differences can be seen as a different role of the control circuit.

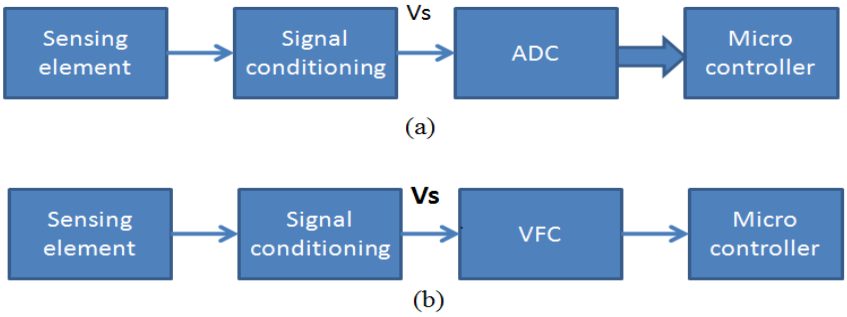

Fig.1.1 (a) Conventional sensing system using ADC and (b) Sensing system using V/F converter

This paper deals with the implementation and performance analysis of a CMOS multivibrator based voltage to frequency converter in 180 nm technology. The rest of the paper is organized as follows. Section II describes the circuit description and the design considerations of the proposed CMOS multivibrator based VFC, Section III describes the simulation results, Section IV concludes the paper.

II CMOS MULTIVIBRATOR BASED VOLTAGE TO FREQUENCY CONVERTOR

A. Circuit description

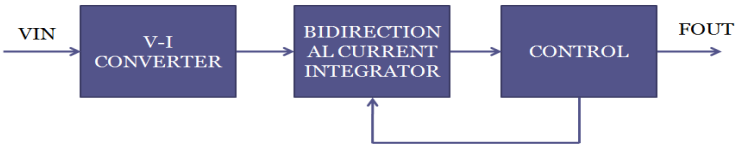

Fig.2.1 Multivibrator based VFC architechture

The basic block diagram of the multivibrator based voltage to frequency converter is shown in the Fig. 2.1. In this type of VFC, the conversion mainly involves two steps, first the input voltage to current conversion and then current to frequency conversion [6]. The complete schematic diagram of the proposed VFC is shown in the Fig 2.2. voltage VI is first converted in to corresponding current signal VI/R1 through the resistor R1 with a linear voltage to current convertor formed by transistors Q1-Q7 and resistor R1[7]. Is1 is the bias current. The current IF is given by

$IF = I_{S1} + VI/R1$ (1)

This current IF is mirrored through transistor Q8 with a gain 1/M. The scaled current IF/M alternately charges and discharges a grounded capacitor C1 through transmission gates between the stable limits VH and VL.

The control circuitry is used to generate the control signals SDW and SUP, is based on a voltage window comparator formed by two comparators as shown in the Fig. 2.3. The voltage window comparator [8] compares the capacitor voltage

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Vcap with two constant boundary voltages VH and VL. The output of comparators VCH and VCL are given to RS latch, to generate stable control signals SUP and SDW.

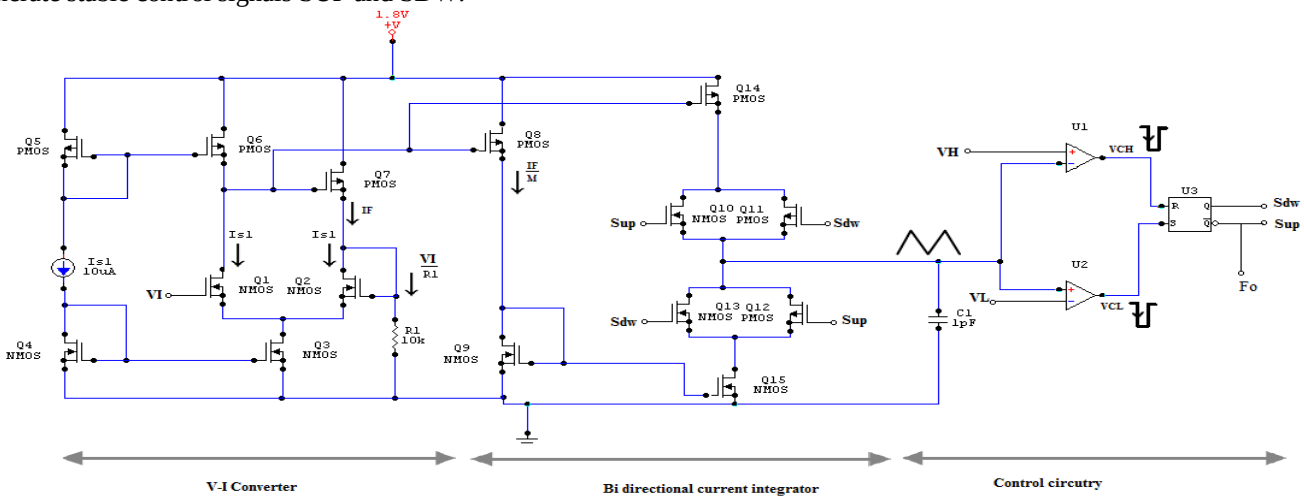

Fig.2.2 Complete schematic diagram of the CMOS multivibrator based VFC

When Vcap charges up to VH, the comparator 1 output switches to 0, ie VCH=0 resetting the RS latch; hence SUP and SDW, switching the capacitor to its discharge phase. When Vcap discharge to VL, the VCL=0. Thus, activating set S, hence SUP =1 and SDW=0 again switching the capacitor to its charging phase. This process repeats with a frequency of oscillation FO given by,

$$F_O = IF / [M \times 2 \times (V_H - V_L)] = [I_{S1} + VI/R1] / [M \times 2 \times (V_H - V_L) \times C] \quad (2)$$

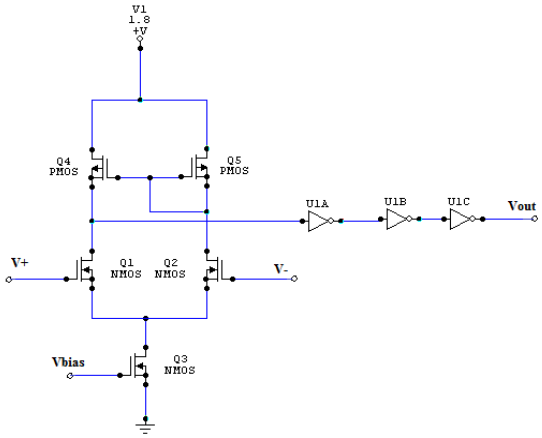

Fig.2.3 (a) Complete schematic diagram of the CMOS multivibrator based VFC

B. Design Considerations

The VFC of Fig. 2.2 has been designed in a 180nm CMOS technology, with a single 1.8 V supply. The biasing current Is1 is set to 10µA and introduced to the circuit through simple current mirrors formed by PMOS Q5-Q6 = (5µm/0.18µm) with 1:1 gain and NMOS Q4- Q3= (2µ/0.18µm) with 1:2 gain. The input voltage range VI can have voltage values ranging from

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0.6 V to 1.8 V. The pair transistors sizes Q1, Q2 are (20µm/0.18µm) to obtain better matching and negligible offset. The resistance R1 is fixed to 10K. Therefore, IF = 10µA + (VI/10K). Transistors Q7-Q8 are cascoded transistors, with a 2:1 scaling ratio and sizes (10µm/0.18µm) and (5µm/0.18µm). Transistors Q9, Q15= (2µm/0.18µm) constitute a high swing cascade current mirror, in order to improve the current mirroring performance while allowing low voltage operation.

The transmission gates, identical for the charging and discharging paths, are simple parallel NMOS/PMOS with sizes (2µm/0.18µm) and (5µm/0.18µm) respectively. The integrating capacitor is fixed to 1pF. The comparator limits are set to VL = 0.22V and VH = 0.4V, so that the capacitor voltage Vcap varies from 0.22V to 0.4V, values that keep the cascode transistors Q14-Q15 properly working in their saturation regions. The comparators are simple differential pairs followed by inverters, as shown in Fig. 3.2, biased to provide a fast time response <1.5ns that do not degrade the linearity performance. Finally, a simple NOR-based RS latch has been used as the final control logic.

II. SIMULATION RESULTS

The CMOS multivibrator based voltage to frequency converter discussed has been simulated using Cadence Virtuoso in 180nm technology, and the output frequency for different input voltages and total power consumption is measured. The input range of the voltage to frequency converter is obtained at 0.6V to 1.8V. The complete output waveforms obtained after simulation is shown in the Fig. 3.1.

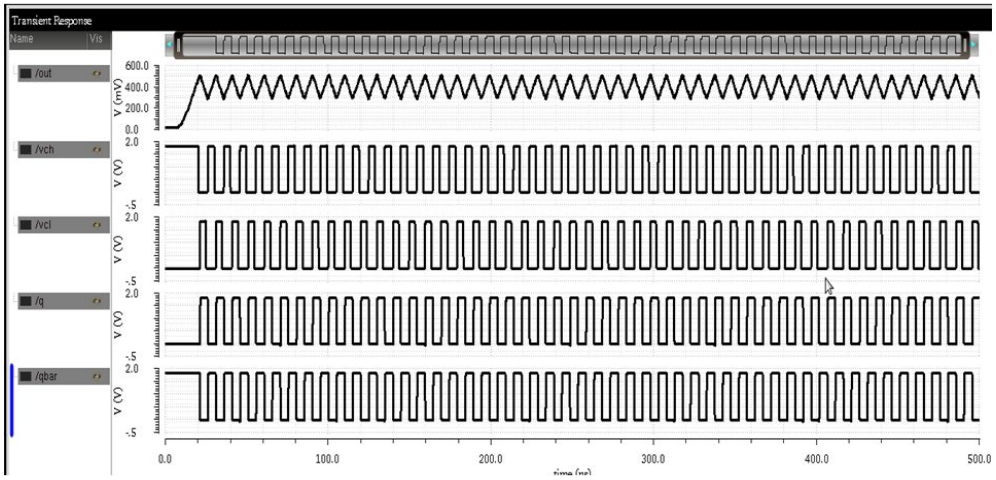

Fig.3.1 Intermediate and output waveforms of the proposed VFC

The capacitor voltage Vcap and the output frequency for VI=0.6V and VI=1.8V are shown in the Fig.3.2 and Fig.3.3 respectively. The output frequency obtained for corresponding input voltages are tabulated below. The total peak total power consumption of the voltage to frequency converter is observed as 281.2µW.

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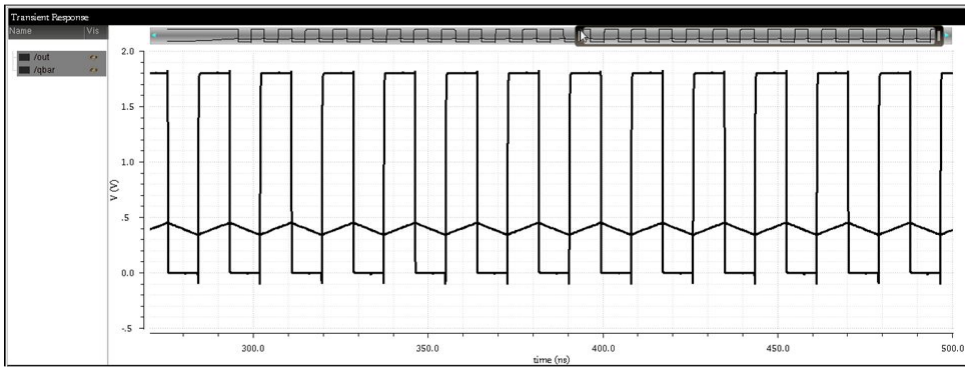

Fig.3.3 Vcap and FO for VI=0.6V

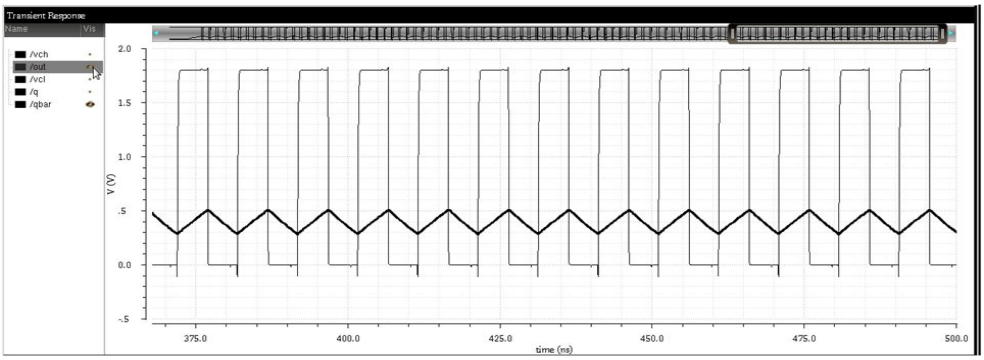

Fig.3.3 Vcap and FO for VI=1.8V

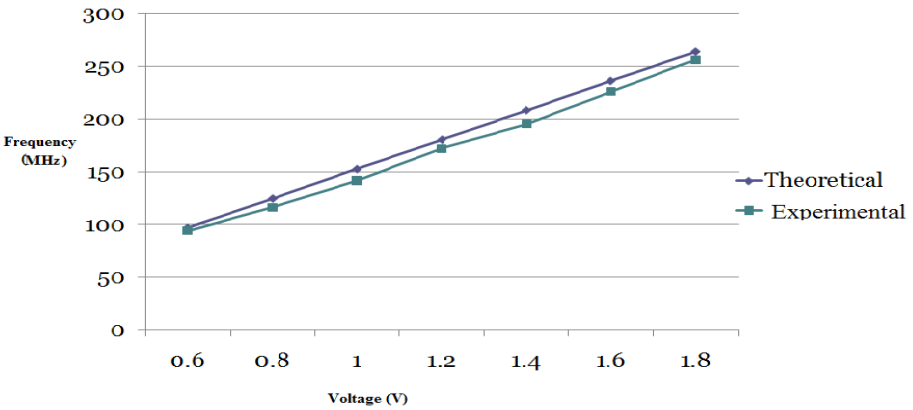

Fig.3.4 Input voltage Vs Frequency

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Voltage (V)	THEORETICAL FREQUENCY (MHz)	OBTAINED OUTPUT FREQUENCY (MHz)
0.6	97.22	95.22
0.8	125	117.42
1	152.77	142.18
1.2	180.55	175.23
1.4	208.33	198.18
1.6	236.11	229.35
1.8	263.88	258.36

Table 3.1 Theoretical and obtained output frequencies for VFC

IV. CONCLUSION

A simple multivibrator based voltage to frequency converter has been presented focusing on the present day increasing demand for low-cost, high performance, low-power, interface electronics targeting wireless sensor networks applications. The voltage to frequency converter is designed in 180nm technology with 1.8V power supply. The acceptable input range for the proposed VFC is 0.6V to 1.8V. It exhibits high performance in terms of sensitivity and consumes less power with respect to the previously reported alternatives.

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