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A New Reversible 'SMT' Gate and its Application to Design Low Power Circuits

Monika Tiwari[1], G.R. Mishra[2] , O.P.Singh[2]

M.Tech Student, Dept. of E.C.E, Amity University, Lucknow (U.P.), India[1]

Associate Professor, Dept. of E.C.E, Amity University, Lucknow (U.P.), India[2]

ABSTRACT: Reversible logic concept gaining much attention of researchers due to its characteristics of generating loss-less system. Reversible logic technology do not erase information hence no heat dissipation. In this paper a new reversible SMT logic gate has been proposed .The proposed three inputs, three outputs reversible logic based SMT gate has designed for Logical, Boolean and Arithmetical functions. This gate needs only one clock cycle to perform multifunctional operation and produce no garbage output. In the present investigation reversible half adder and half subtractor gate has been successfully realized by SMT gate. It produces zero garbage outputs. The proper coding proves that the proposed gates are fulfilling the requirement of reversible logic gate. In present paper different properties of SMT gate has been simulated using VHDL.

KEYWORDS: Reversible logic, Reversible gate, Power dissipation, SMT gate, Half-adder and half subtractor

I. INTRODUCTION

Energy dissipation is one of the major issues in present day technology. Present day Computing Systems are using processors which are faster, smaller and more complex than their predecessors. Arithmetic and logic unit is one of the most power consuming components .So low power ALU design to be a multi-dimensional problem. It provides common functions for arithmetic and logic operations. The half-adder and half subs tractor are the most used ALU operations. Most used ALU operations are ADDITION, AND and OR etc. Out of these additions has a highest frequency as dominating to other ALU operations.

Arithmetic and logic operation corresponds to the flipping of bits at very high clock frequencies in the range of gigahertz/terahertz. During such operations, some input and output bits are erased every time a new logic operation/switching (function) is performed. R Laundauer[1] has shown that the amount of energy (heat) dissipated, during such operation, called as irreversible operation is given by KTln2 for a single bit irreversible operation , where K is the Boltmann's constant ($1.3807 X 10^{-23} Jk^{-1}$) and T is the operating temperature (300K). KTln2 is approximately $2.8X10^{-21}$ J, which is small but non-negligible considering next generation computing system. This energy consumption is the main concern of next generation computing systems. Earlier work of Bennet[2] shows that energy consumption and heat dissipation can be reduced by use of reversible logic gates. To achieve energy efficient computing systems performance, we must continue to reduce the energy dissipation from each logic operation. Literature survey shows that several reversible logic gates have been developed over the years which may be used to overcome the above constraints. Reversible computation in a system can be performed only when the system comprises of reversible gates.

This paper is organized in five sections. Introduction and basic reversible logic concepts are explained in section I. The proposed reversible SMT gate and its application and truth-table are given in section II, III and IV. Result and analysis are provided in section V and the paper is concluded in section VI. In this paper, a new reversible logic gate SMT has been proposed which may be used to implement any Boolean logic function which is shown in figure1. The present reversible gate is named as Singh Mishra Tiwari (SMT) Gate. This gate require only one clock cycle and produces no extra garbage output it adheres to the theoretical minimum as established in [3],[4].

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DESIGN CONSTRAINTS FOR REVERSIBLE LOGIC CIRCUITS :

The following are the important design constraints for reversible logic circuits.

- Reversible logic gates do not allow fan-outs.
- Reversible logic circuits should have minimum quantum cost.
- The design can be optimized so as to produce minimum number of garbage outputs.
- The reversible logic circuits must use minimum number of constant inputs.
- The reversible logic circuits must use a minimum logic depth or gate levels.

II. SINGH MISHRA TIWARI GATE

A reversible SMT gate design should satisfy the following conditions:

A. Condition 1

A reversible logic gate should have some characteristics such as equal number of input and output signals, one to one mapping between inputs and outputs also known as " Bijective Conditions"[5]

B. Condition 2

Each output function must be equal to 1 for its half of the inputs, known as "Balance Conditions"[6]-[8].

C. Condition 3

By inversing output, we must be able to reproduce mapped input called as "Dual" or Inversing Conditions"[9].

Testing of above reversible logic gate properties has been studied on the 3 input, 3 output SMT gate. Truth Table 1 and simulated result shown in figure 3 of SMT Gate shows that it satisfied all the conditions of the Reversible logic as discussed above.

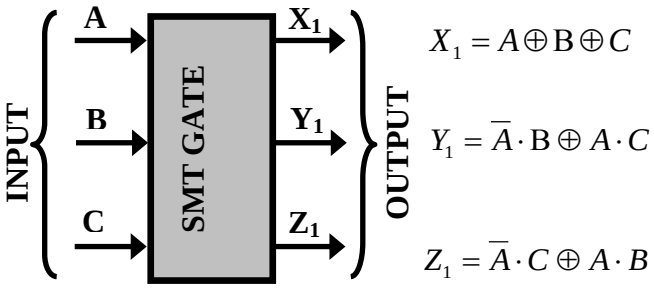

Figure 1 – SMT Gate

III. APPLICATION OF SMT GATE

This proposed 3-bit SMT gate satisfying the entire reversibility conditions.SMT gate can be programmed to implement NOT, Coping gate, XOR gate .This gate also work as half adder and half subs tractor. The proposed 3-bit SMT gate is designed for the first time and implements the logical operations, which are the most fundamental component for designing any digital circuits.

A. Half Adder

SMT gate work as half adder and half subs tractor at a time. The half adder produces a sum and carry, where

$$SUM = A \oplus B$$

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$$CARRY = A \cdot B$$

B. Half Subtractor

Thus proposed SMT gate also work as half subs-tractor. The half subtractor produces a difference and borrows, where

$$DIFFERENCE = A \oplus B$$

$$BORROW = \overline{A} \cdot B$$

Thus proposed SMT gate can be converted into Reversible Half adder and Half subs-tractor gate as shown in figure 2, by putting third input to '0'i.e., C = '0'. It has been found that the proposed reversible half adder and half subtractor is better than previous reversible half adder and half subtractor as reported by previous researchers [10]-[16] in term of number of garbage outputs.

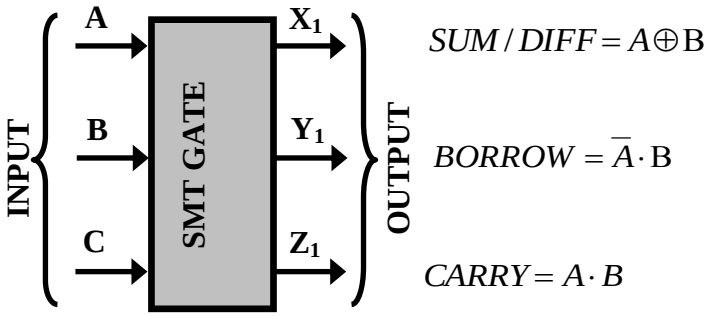

FIGURE 2: SMT Gate as half-adder and half subtractor

C. SMT Gate as Logic gates

Basic building blocks of any digital circuits required NOT, AND, OR etc logic implementation. SMT gate can be programmed to implement NOT, AND, OR and XOR operation without producing any garbage output.

IV. TRUTH-TABLE OF SMT GATE

Truth-table of SMT gate shown in table 1 which contain 3-input and 3-output.Truth-table of SMT gate satisfied all the conditions of the reversible logic. It satisfied the bijective conditions, Balance condition and Inverse Conditions.

A	B	C	X_1	Y_1	Z_1
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	1	1	0

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0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	0	0	1
1	1	1	1	1	1

TRUTH TABLE-1

V. VHDL SIMULATION RESULTS

Proposed SMT gate shown in figure 1 is simulated using Modelsim simulator and synthesized for Xilinx ISE Design suite 14.4. Figure 3 shows the simulated waveform of the proposed 3-bit SMT gate using reversible logic. The waveforms show that the proposed circuit work well according to the function table shown in table1.It is clear from waveform that if input A,B,C is taken 0,1,1 respectively then corresponding output is found 0,1,1 which proves well the validity of the circuit. Figure 4 and 5 provides the synthesized circuits of the proposed SMT reversible gates.

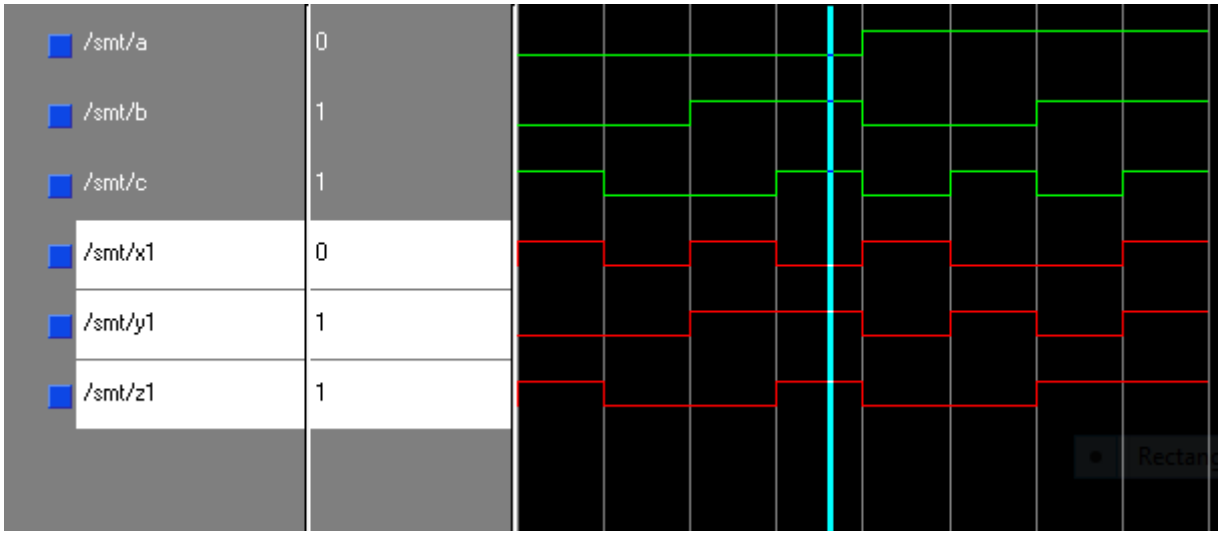

Figure 3: SMT Gate VHDL Simulation

Figure 4 provides the synthesized technology schematic circuit of the proposed SMT reversible gate which clearly indicates that the present proposed SMT gate can be designed using less number of gates as compared to the earlier 3-input reversible gates.

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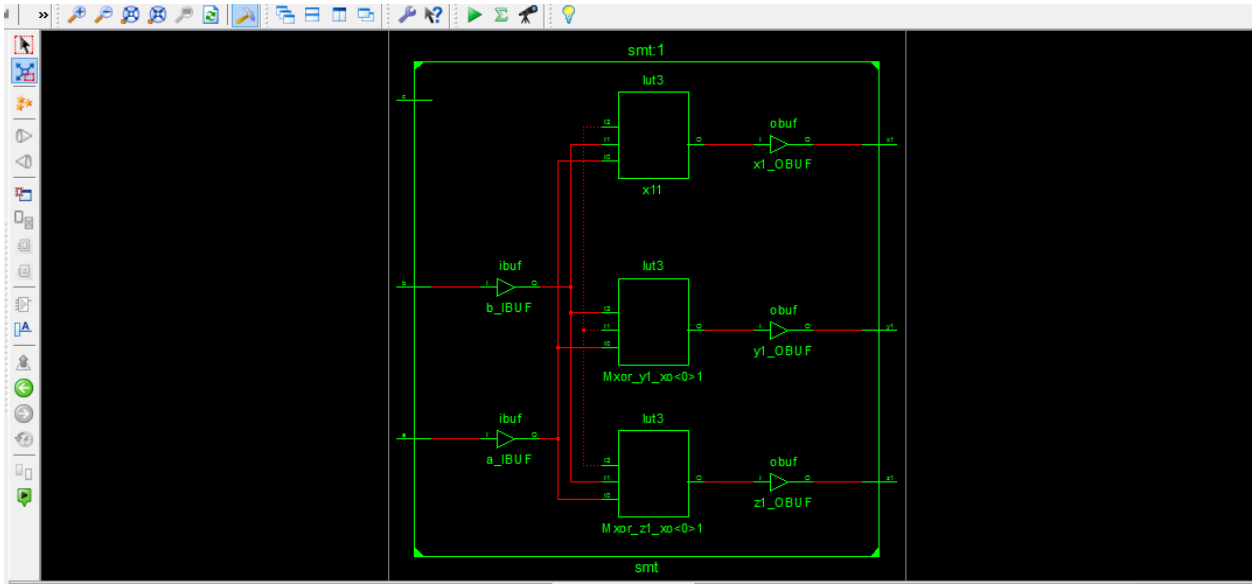

Figure 4: Technology schematic circuit of SMT Gate

Figure 5 provides the synthesized RTL schematic circuit of the proposed SMT reversible gate. It helps to understand the circuit better in term of component for hardware designing of the present proposed circuit.

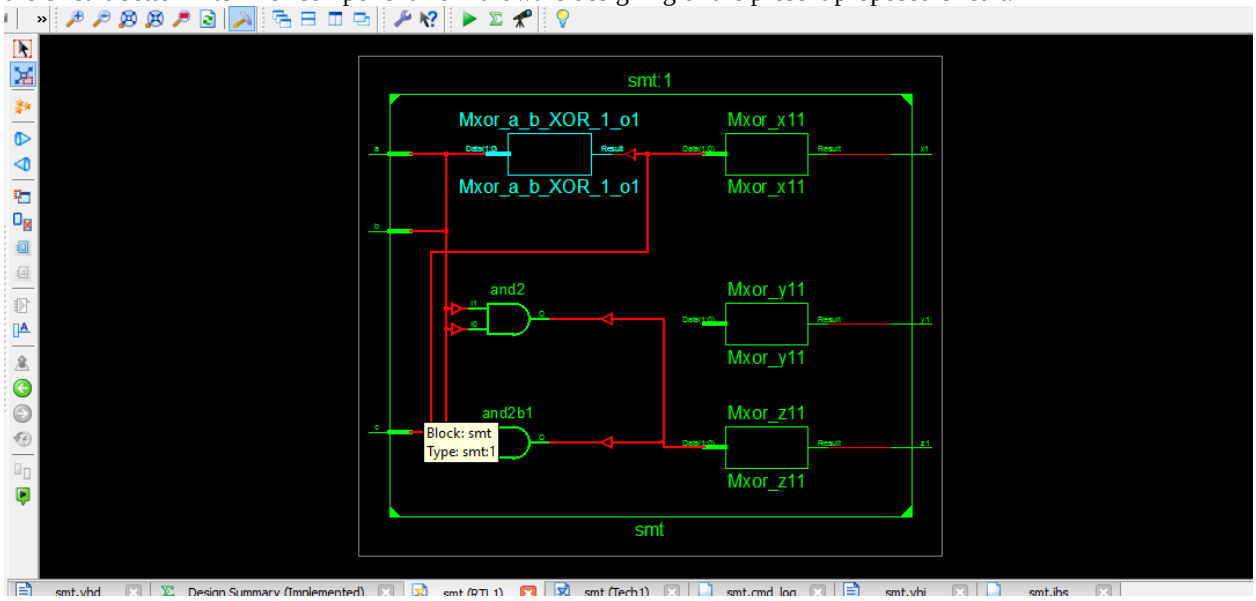

Figure 5: RTL schematic circuit of SMT Gate

VI. CONCLUSION AND FUTURE WORK

The proposed 3-bit SMT gate is designed for the first time and implements all the logical operations very well, which are the most fundamental components for designing of any digital circuits. Since all the logical operations are executed in a single clock using single gate, hence the speed of the proposed gate is also fast. This gate can be programmed for

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multifunctional operation without producing any garbage output. The proposed gate will give a platform to the engineers and scientist to explore the possibilities of designing multifunctional programmable reversible circuit for low power digital applications in future. We can say with positive hope that the future is the age of the reversible logic technology. It is a duty of industry to adopt such new and challenging technology to design the respective ICs which has property of low power dissipation hence durable and flexible ICs for low voltage high speed applications.

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