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A Novel Approach to Condense the Leakage Power in Deep Submicron Circuits by Sleep Methods

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ABSTRACT: It is very important for any circuit to dissipate low power**.** As the low power dissipation circuits are most popular now a days when the scaling of the circuit increases the leakage power also increases rapidly in the circuit. So, for decreasing these kinds of leakages and to provide a better power efficiency there are many types of power gating techniques. In this paper a novel approach to analyse the different types of flip-flops using different types of power gated circuits using low power VLSI design techniques are presented. And also the comparison results between all the methods also presented. The power gating techniques used in this paper are Fine-grain power gating, Coarse-grain power gating. Different stack methods used in this paper are sleepy stack, Dual sleep and Dual stack method.

I. INTRODUCTION

The scaling of process technologies to nanometer regime has resulted in a rapid increase in leakage power dissipation. Hence, it has become extremely important to develop design techniques to reduce static power dissipation during periods of inactivity. The power reduction must be achieved without trading-off performance which makes it harder to reduce leakage during normal (runtime) operation. On the other hand, there are several techniques for reducing leakage power in *sleep* or *standby* mode. Power gating is one such well known technique where a *sleep transistor* is added between actual ground rail and circuit ground (called *virtual ground*). This device is turned-off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance. Power gating technique uses high Vt sleep transistors which cut off VDD from a circuit block when the block is not switching. The sleep transistor sizing is a significant invent parameter. This technique, also known as MTCMOS, or Multi-Threshold CMOS reduces stand-by or leakage power, and also enables Iddq testing.

Power gating have an effect on design planning more than clock gating. It increase time delays as power gated modes have to be securely entered and departure. Architectural exchanges exist between designing for the quantity of seepage power saving in low power modes and the energy dissipation to enter and exit the low power modes. Finishing the blocks can be accomplished either by software or hardware. Driver software can programmed the power down operations. Hardware timers can be used. A devoted power management controller is another option.

An externally controlled power supply is a basic form of power gating to accomplish long term outflow power reduction. To lock off the block for small intervals of time, internal power gating is more payable. CMOS switches that offer power to the circuitry are controlled by power gating controllers. Outputs of the power gated slab discharges slowly. Hence output voltage levels use more time in threshold voltage level. This can lead to big short circuit current.

Power gating utilizes low-escape PMOS transistors as header switches to close off power supplies to parts of a design in standby or sleep mode. NMOS footer switches can also be used as sleep transistors. Adding the sleep transistors tears the chip's power arrangement into a stable power network connected to the power supply and a effective power network that forces the cells and can be turned off.

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The worth of this difficult power network is significant to the success of a power-gating design. Two of the most important constraints are the IR-drop and the penalties in silicon area and routing resources. Power gating can be realized using cell- or cluster-based (or fine grain) approaches or a distributed coarse-grained approach.

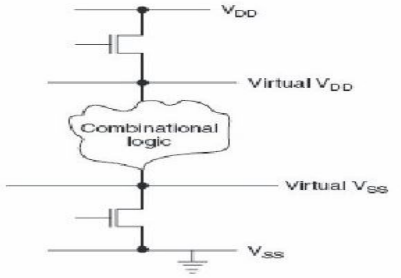

Fig1: Basic Power Gating Circuit

II. PARAMETERS OF POWER GATE CIRCUIT

Power gating operation has extra considerations for timing closure implementation. The subsequent parameters need to be considered and their values carefully chosen for a successful implementation of this methodology.

1. *Power gate Size*: The power gate Size should be selected to hold the quantity of switching current at any given time. The gate must be bigger such that there is no measurable voltage (IR) drop due to the gate. As a rule of thumb, the gate dimension is selected to be around 3 times the switching capacitance. Designers can also select between header (P-MOS) and footer (N-MOS) gate. Usually footer gates lean to be smaller in vicinity for the same switching current. Dynamic power study tools can accurately measure the switching current and also predict the Size for the power gate.
2. *Gate control slew rate*: In power gating, this is an important constraint that determines the power gating efficiency. When the slew rate is huge, it takes more time to switch off and switch-on the circuit and therefore can manipulate the power gating efficiency. Slew rate is controlled during buffering the gate control Signal.
3. *Simultaneous switching capacitance*: This important restriction refers to the amount of circuit that can be switched simultaneously without affecting the power network integrity. If a large amount of the circuit is switched simultaneously, the resulting "rush current" can compromise the power network integrity. The circuit needs to be switched in stage in order to prevent this.
4. *Power gate leakage*: Since power gates are made of vigorous transistors, leakage reduction is an important consideration to maximize power savings.

i) Power Gating Method-1

This is a Fine-grain power gating technique. Adding a sleep transistor to every cell that is to be turned off requires a huge area penalty, and independently gating the power of every cluster of cells makes timing problem introduced by inter-cluster voltage deviation that are difficult to determine. Fine-grain power gating summarizes the switching transistor as a element of the standard cell logic. Switching transistors are planned by either the library IP vendor or standard cell designer. Regularly these cell designs match to the normal standard cell rules and can easily be handled by EDA tools for functioning.

The dimension of the gate control is designed considering the most terrible case situation that will need the circuit to toggle during every clock cycle, resulting in an enormous area impact. Some of the current designs implement the fine-grain power gating selectively, but only for the low Vt cells. If the equipment allows multiple Vt libraries, the use of low Vt devices smallest in the design (20%), so that the area contact can be reduced. When using power gates on the low Vt cells the output must be separated if the next stage is a high Vt cell. If not it can cause the neighbouring high Vt cell to have outflow when output goes to an unidentified state due to power gating.

Gate control slew rate restraint is achieved by having a barrier sharing tree for the control Signals. The buffers must be chosen from a set of always on buffers (buffers without the gate control Signal) designed with high Vt cells. The

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intrinsic difference between when a cell switches off with respect to another, minimizes the run current during switch-on and switch-off.

Typically the gating transistor is designed as a high Vt device. Coarse-grain power gating suggests additional flexibility by optimizing the power gating cells where there is low switching activity. Leakage optimization has to be done at the common grain level, swapping the low leakage cell for the high leakage one. Fine-grain power gating is an elegant methodology resulting in up to 10 times leakage reduction. This type of power drop makes it an attractive technique if the power reduction requirement is not satisfied by multiple Vt optimization alone.

ii) Power Gating Method-II

This is also called Coarse-grain power gating technique. The coarse-grained process applies the grid manner sleep transistor which drives cells locally through shared effective power networks. This approach is less sensitive to PVT variation, introduces less IR-drop variation, and enforces a little area slide than the cell- or cluster-based operations. In coarse-grain power gating, the power-gating transistor is a division of the power distribution network rather than the standard cell.

There are two ways of implementing a coarse-grain structure:

1. *Ring-based*: The power gates are positioned around the boundary of the module that is being switched-off as a ring. Special corner cells are used to revolve the power Signals around the corners.
2. *Column-based*: The power gates are inserted within the module with the cells adjoined to each other in the form of columns. The universal power is the higher layers of metal, while the switched power is the lower layers.

III.Power Gating for Delay Reduction

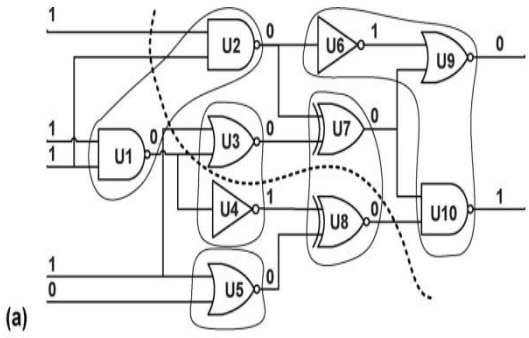

Fig2: Device without Power gating.

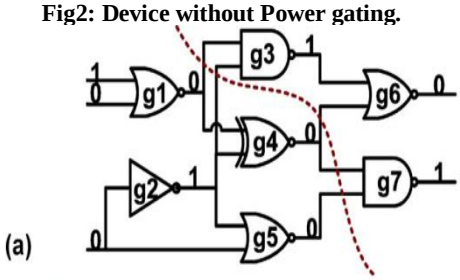

Fig3: Device with Power gating with reduced area & Power using clustering network formation.

The work presented a logic clustering based explanation to the trouble of controlling/optimizing the power gating parameters. The key devise consideration in the power mode transitions are minimizing the wakeup delay, the peak current, and the total Size of sleep transistors. This work examined the relations between the three parameters, and solved the problem of finding logic clusters and their wakeup schedule that minimize the wakeup delay even as satisfying the peak current and performance loss constraints.

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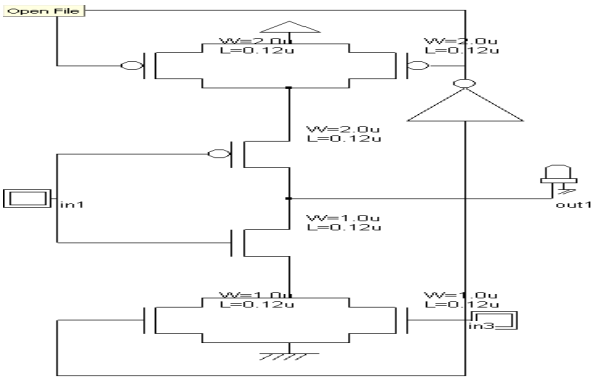

Fig4: Sleepy stack

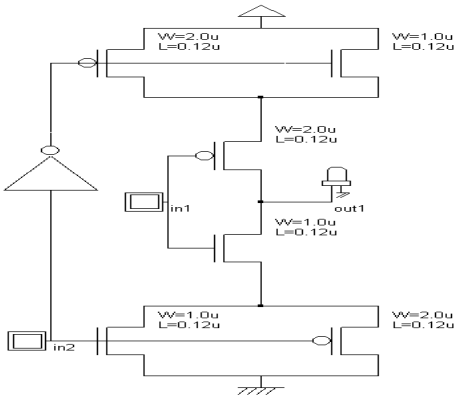

Fig5: Dual Sleep Method

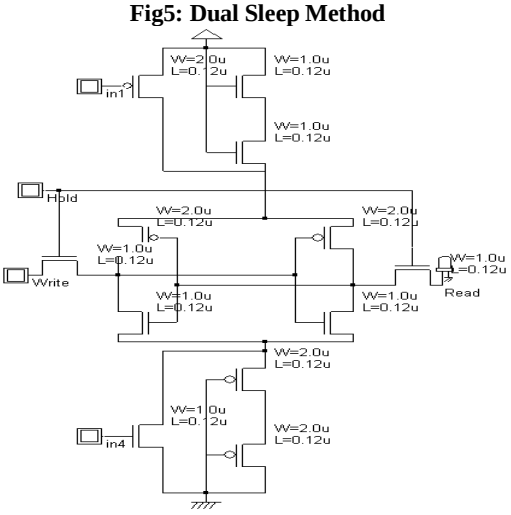

Fig6: Dual Stack Approach

A variant of the sleep approach, the zigzag approach, decreases wake- up slide caused by sleep transistors by appointment of alternating sleep transistors assuming a particular pre-selected input vector [6]. Another method for leakage power reduction is the stack approach, which forces a pile effect by breaking down an existing transistor into two half Size transistors [7]. The divided transistor enhance delay significantly and could control the usefulness of the method. The sleepy stack approach (Fig. 2) joins the sleep and stack approaches [2, 3]. The sleepy stack technique

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divides existing transistor into two half Size transistors like the stack method. Then sleep transistors are inserted in parallel to one of the divided transistors. During sleep mode, sleep transistors are bowed off and stacked transistors hold back leakage current while saving state. Each sleep transistor, leaved in parallel to the one of the stacked transistors, decreases resistance of the lane, so delay is reduced throughout active mode. But, the area consequence is a significant matter for this approach because every transistor is substituted by three transistors and since extra wires are added for S and S', which are sleep Signals. Another technique called Dual sleep approach [8] (Fig. 3) uses the benefit of using the two extra pull- up and two extra pull-down transistor in sleep mode either in OFF state or in ON state. Because the dual sleep portion can be made common to all logic circuitry, less number of transistors needed to apply a certain logic circuit.

Proposed method

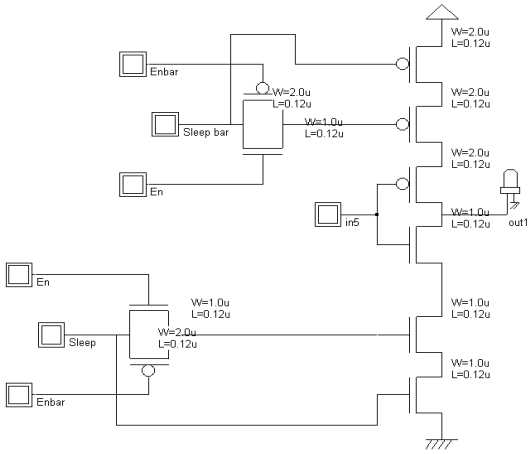

Fig.7 Power gating based sleep technique

The Above mentioned Sleep Circuit has three modes of operations
I. Active mode
2. Standby mode
3. Sleep to active mode transition
In active mode, the sleep Signal of the transistor is held at logic' 1 ' and both the sleep transistors M I and M2 (En and EnBar Transistors from the bottom side) remain ON. In this case both transistors offer very low resistance and virtual ground (VGND) node potential is pulled down to the ground potential, making the logic difference between the logic circuitry approximately equal to the supply voltage.
There are several benefits of combining stacked sleep transistors. First the magnitude of power supply fluctuations sleep mode during mode transitions will be reduced because these transitions are gradual. Second, while conventional power gating uses a high- threshold device as a sleep transistor to minimize leakage, a stacked sleep structures can achieve the same effect with a normal threshold device
In active mode, the sleep Signal of the transistor is held at logic' 1 ' and both the sleep transistors NMOS1 and NMOS2 (NMOS Transistors used for sleep Purpose from the Bottom of the circuit) remain ON and control transistor is OFF by giving logic O. In this case both transistors offer very low resistance and virtual ground (VGND) node potential is pulled down to the ground potential, making the logic difference between the logic circuitry approximately equal to the supply Voltage. And leakage current is reduced by the stacking effect, turning both NMOS1 and NMOS2 sleep transistors OFF. And vice versa for the header switch.

Positive potential at the intermediate node has four effects:

- Gate to source voltage of NMOS1 (VgNMOS1) becomes negative.

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- -Negative body -to-source potential (Vdsl) of NMOS1 decreases, resulting in less drain induced barrier lowering.
- -Drain-to-source potential (VdNMOS2) of NMOS2 is less compared to NMOS1, because most of the voltage drops across the NMOS1 in sleep mode.

This significantly reduces the drain barrier lowering. The analysed design gives major contribution in sleep to active mode in terms of peak of sleep mode compared to stacking power gating. Sleep mode occurs when circuit is going from sleep to active and vice versa. In first stage sleep transistor (NMOS1) working as diode by tum on the control transistor M I which is connected across the drain and gate of the sleep transistor (NMOS1). Due to this drain to source current of the sleep transistor drops in a quadratic manner. This reduces the voltage fluctuation on the ground and power net and it also reduces the circuit wakeup time. So in sleep to active transition mode, we are turning ON transistor NMOS1 initially after small duration of time NMOS2 will be turned ON to reduce the GBN. In second stage control transistor is off that sleep transistor works normally.

During sleep to active mode transition, transistor NMOS1 is turned ON and transistor NMOS2 is turned ON after a small duration of time (6 T). The logic circuit is isolated from the ground for a short duration as the transistor NMOS2 is turned OFF. During this duration, the GBN can be greatly reduced by controlling the intermediate node voltage VGND2 and operating the transistor NMOS2 in triode region.
The intermediate node (VGND2) voltage can by

Inserting proper amount of delay, that is less than the discharging time of the NMOS1 transistor. Proper selection of the capacitance C2. Leakage current is reduced by the stacking effect, turning both NMOS1 and NMOS2 sleep transistors OFF. This raises the intermediate node voltage VGND2 to positive values due to small drain current. Positive potential at the intermediate node has four effects:

Gate to source voltage of NMOS1 (VgNMOS1) becomes negative. Negative body- to- source potential (VbNMOS1) of NMOS1 causes more body effect Drain- to- source potential (Vdsl) of NMOS1 decreases, resulting in less drain induced barrier lowering.

Drain-to-source potential (VdNMOS2) of NMOS2 is less compared to NMOS1, because most of the voltage drops across the NMOS1 in sleep mode this significantly reduces the drain induced barrier lowering.

Performance evaluation of different techniques used

Method	Area	Power
Dual Sleep	16 x 13µm	4.267µW
Sleepy Stack	16 x 13µm	4.59µW
Dual Stack	47 x 23µm	0.36µW
Proposed	23 x 13µm	0.21µW

V. CONCLUSIONS

In nanometer scale CMOS technology, sub threshold leakage power consumption is a great challenge. Although previous approaches are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, designers choose techniques based upon technology and design criteria. In this paper, we provide novel circuit structure named “Dual stack” as a new remedy for designer in terms of static power and dynamic powers. Unlike the sleep transistor technique, the dual stack technique retains the original state. The dual stack approach shows the least speed power product among all methods. Therefore, the dual stack technique provides new ways to designers who require ultra-low leakage power consumption with much less speed power product. Especially it shows nearly 50-60% of power than the existing normal or conventional flip-flops. So, it can be used for future integrated circuits for

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BIOGRAPHY

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