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A Novel Circuit Model of Small-Signal Amplifier Developed by Using BJT-JFET-BJT in Triple Darlington Configuration

SachchidaNand Shukla[1] and Susmrita Srivastava[2]

[1]Associate Professor, [2]Research Scholar, Department of Physics and Electronics,

Dr. Ram Manohar Lohia Avadh University, Faizabad - 224001, U.P., India.

E-mail: sachida_shukla@yahoo.co.in

Abstract: Two distinct configurations of small-signal amplifiers, consisting hybrid combination of BJT-FET-BJT in Triple Darlington topology, are proposed and qualitatively analyzed perhaps for the first time. The first proposed amplifier crops high voltage with moderate current gain and bandwidth in 1-15mV input signal range at 1 KHz frequency. However, the second amplifier is configured by creating certain modifications in the first circuit. This amplifier produces about double voltage and current gain than the first amplifier circuit with almost half bandwidth in 1-4mV input-signal-range at 1 KHz frequency. Both the amplifier circuits include two additional biasing resistances. Variations in voltage gain as a function of frequency and different biasing resistances, temperature dependency of performance parameters, bandwidth and total harmonic distortion of the amplifiers are also perused. The proposed amplifiers can be successfully implemented as high power gain small-signal amplifiers in audio-frequency-range because of the obtained values of the current and voltage gains which are higher than unity.

Key words: Small-signal amplifiers, Darlington amplifiers, Common Source JFET amplifiers

I. INTRODUCTION

One of the important concepts in electronics is the process of amplification through Darlington pair which is considered to be a prominent configuration due to its wide range of application [1]-[5]. The flexible application-range of this vital configuration is extended from small-signal amplifiers to power amplifier circuits [1]-[5]. However, a major drawback is associated with small-signal Darlington pair amplifier i.e. at higher frequencies its response becomes poor than that of a single transistor amplifier [3]-[5]. Various attempts have been made to defeat this problem by proposing different modifications in Darlington's composite unit as well as in respective amplifier circuits [6]-[10]. These efforts include the use of Field Effect Transistors in paired unit [11]-[13], experimentation with Triple Darlington's topology [5], [14]-[16] or the inclusion of some extra biasing resistances in respective circuits [3]-[4], [12], [15]-[16]. However, use of dissimilar active devices or hybrid combination of active devices in Darlington's topology (such as Darlington's unit with BJT and FET or BJT and MOSFET etc.) is still an area of electronic circuit designers to work with [11]-[13], [17].

If two identical NPN or PNP transistors are coupled as to form a CC/CE Darlington pair, the current gain of this composite unit of transistors is theoretically considered to be identical to the product of current gains of the individual transistors while the voltage gain climbs down to a considerable limit [3]-[5], [9], [15]-[16]. However, the input resistance of Darlington pair amplifier is much higher and output resistance is lower than that of a single-stage Emitter Follower [1], [3]-[5], [9], [15]-[16]. Similarly, if two identical FETs are coupled as to form a common source JFET Darlington pair amplifier, the input impedance of this configuration is found much higher than that of a BJT amplifier with generally low voltage gain (with inverted output waveform) and improved band width [18].

Though the qualitative properties of BJTs and FETs are entirely different [1]-[2], [11], [19], nevertheless in the present manuscript, authors have proposed two novel circuit models of small-signal amplifiers using hybrid combination of BJT, JFET and BJT in Triple Darlington topology. The proposed amplifiers are well suited for the stages requiring high voltage with moderate range bandwidth and current gain.

The present paper is described in four sections. Section I gives the Introduction of the Darlington's topologies and the idea behind proposed circuits. Section II describes the configuration and component details of the proposed amplifiers. Section III contains the observational details and related discussions whereas the last section IV concludes the proposed work followed by references.

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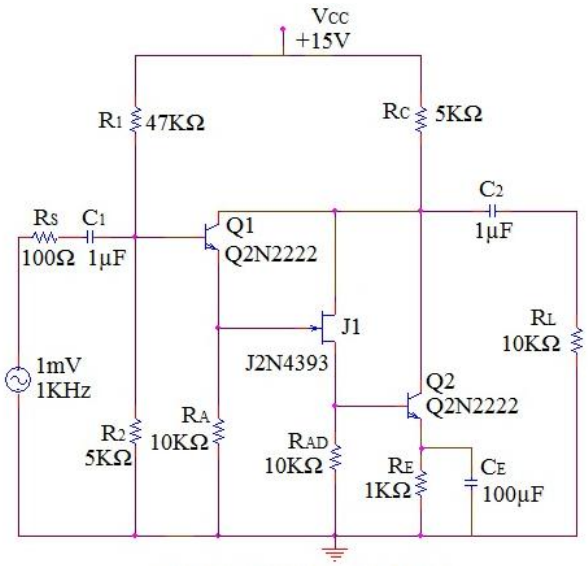
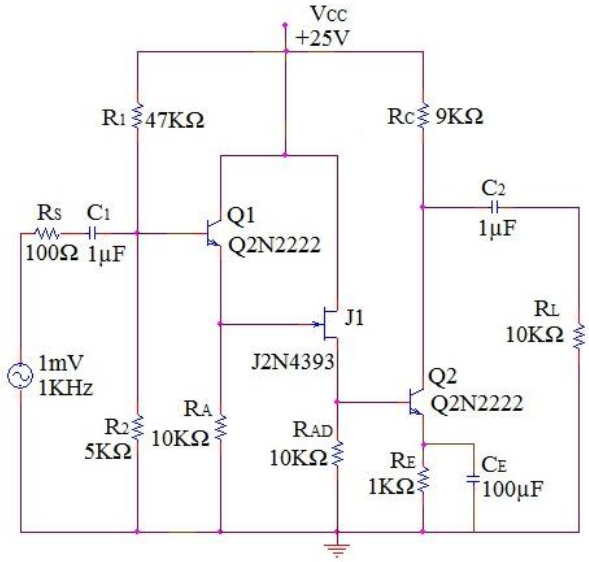
II. EXPERIMENTAL CIRCUITS



Circuit-1: Proposed Amplifier-1



Circuit-2: Proposed Amplifier-2

The present study starts with a small-signal amplifier having compound unit of BJT-JFET-BJT in Triple Darlington topology [5], [10], [14]-[16]. Respective configuration and biasing idea is depicted as Circuit-1. However, the second proposed amplifier, depicted as Circuit-2, is obtained by implementing minor changes in the proposed amplifier Circuit-1. In this amplifier of Circuit-2, Q1 (NPN transistor Q2N2222) and J1 (N-channel JFET J2N4393) are directly connected with DC power supply and the value of R_C is enhanced to 9KΩ. Assembly of Q1, J1 and Q2 in both the proposed amplifiers constitutes a Triple Darlington composite unit.

The proposed amplifier of Circuit-1 is biased with +15V whereas Circuit-2 is biased with +25V DC supply using potential divider network. Various biasing parameters and their respective values in context of the present study are listed in Table-I.

TABLE I
COMPONENT DETAILS OF THE CIRCUITS UNDER DISCUSSION

COMPONENTS	**DESCRIPTION**	**CIRCUIT-1** (Proposed Amplifier-1)	**CIRCUIT-2** (Proposed Amplifier-2)
Q1	NPN BJT (β=255.9)	Q2N2222	Q2N2222
J1	N-Channel JFET (V_{TH}= -1.422)	J2N4393	J2N4393
Q2	NPN BJT (β=255.9)	Q2N2222	Q2N2222
R_S	Source Resistance	100Ω	100Ω
R_1	Biasing Resistance	47KΩ	47KΩ
R_2	Biasing Resistance	5KΩ	5KΩ
R_C	Collector Biasing Resistance	5KΩ	9KΩ
R_E	Emitter Biasing Resistance	1KΩ	1KΩ
R_A	Added Biasing Resistance	10KΩ	10KΩ
R_{AD}	Added Biasing Resistance	10KΩ	10KΩ
R_L	Load Resistance	10KΩ	10KΩ
C_1 , C_2	Coupling Capacitors	1µF	1µF
C_E	Emitter By-pass Capacitor	100µF	100µF
Supply	DC Biasing Supply	+15V DC	+25V DC
AC Signal	Input AC Signal range for distortion-less output at 1KHz input frequency	1-15mV (1KHz)	1-4mV (1KHz)

Respective observations related to the proposed circuits are carried out by feeding them with 1V AC input signal source. From this AC source, a small and distortion less signal of 1mV amplitude at 1 KHz frequency is drawn as input for amplification purpose. All the observations are furnished through 'Student Version-9.2 PSpice Simulation Software' [5], [10], [15]-[16], [20].

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III. RESULTS AND DISCUSSIONS

Amplifiers of Circuit-1 and 2 are found to provide fair and distortion-less results for 1-15mV and 1-4mV AC input signals respectively at the parameter values of Table-I.

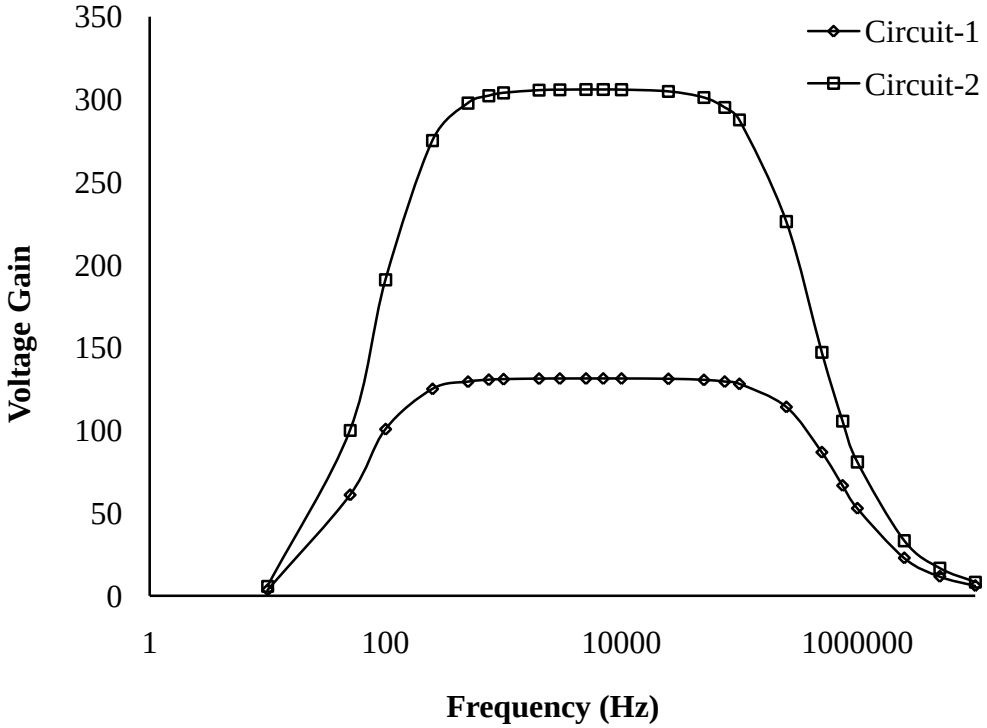

Fig.1. Variation of Voltage gain with Frequency

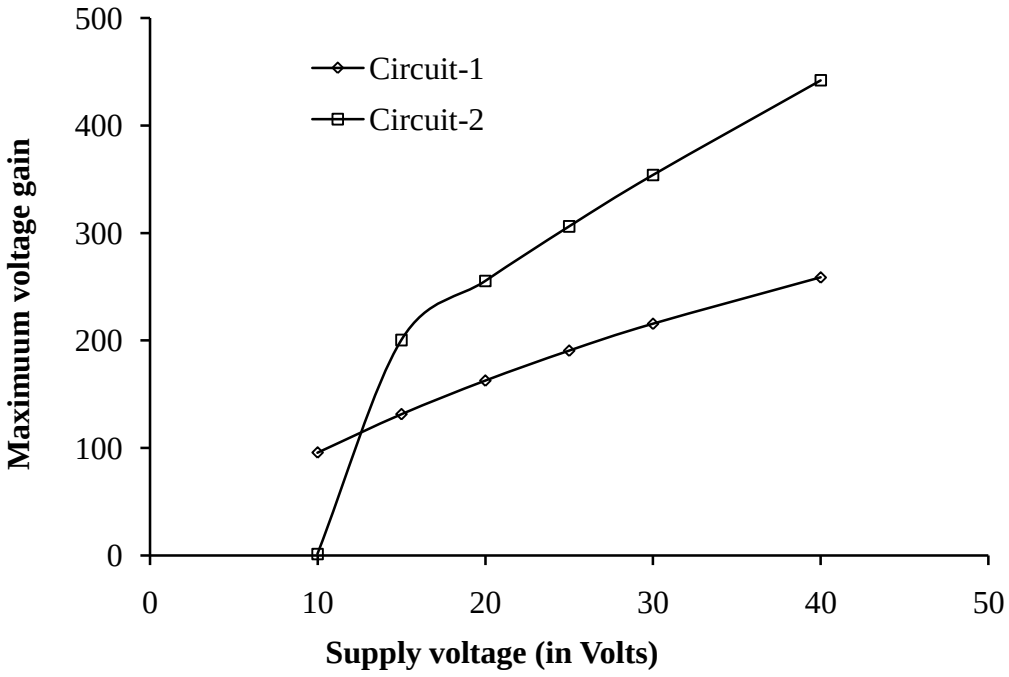

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Fig.2. Variation of Maximum voltage gain with V_{CC}

Variation of voltage gain as a function of frequency for both the amplifiers is depicted in Fig.1. It is found that the proposed amplifier of Circuit-1 produces 131.388 maximum voltage gain, 60.248 maximum current gain and 440.671KHz bandwidth (with lower cut-off frequency f_L=83.954Hz and upper cut-off frequency f_H=440.755KHz), 13.975µA peak output current and 139.582 mV peak output voltage. However, the proposed amplifier of Circuit-2 produces 306.071 maximum voltage gain, 141.033 maximum current gain, 274.700KHz bandwidth (f_L=124.470Hz and f_H=274.825KHz), 30.812µA peak output current and 308.115 mV peak output voltage. Both the proposed amplifiers possess phase reversal in their output waveform.

Total Harmonic Distortion (THD) percentage is also calculated for both the proposed amplifiers for 10 significant harmonic terms using established formulae [1]-[2], [21]. For first proposed amplifier of Circuit-1, THD is found to be 0.84% whereas it is recorded as 1.21% for the proposed amplifier of Circuit-2. Mentioned values of THDs for both the proposed amplifeirs are falling in the permissible limit for small-signal amplifiers [1]-[2]. This clearly suggests that the modifications made in Circuit-1 to obtain the Proposed amplifier of Circuit-2 has almost doubled the corresponding values of maximum voltage and current gains (of Circuit-2) but on the cost of reduced frequency band and significantly enhanced THD. In addition, the proposed small-signal amplifiers (of Circuit-1 and Circuit-2) having hybrid combination of BJT-FET-BJT in Triple Darlington topology produce improved voltage and current gains than that was designed by Tiwari et.al.[11] using compound unit of BJT-FET in Darlington pair configuration.

Variation of maximum voltage gain with DC supply voltage is depicted in Fig.2. Figure suggests that the voltage gain for both the amplifiers rises nonlinearly at increasing values of V_{CC} [10]-[11], [14]-[16]. This happens perhaps due the fact that on increasing biasing supply V_{CC}, the saturation current of BJT driven Triple Darlington composite unit increases which in turn enhances the voltage and current across load resistance R_L and hence the overall voltage gain of the respective amplifier circuits. The maximum permissible range of DC supply voltage for the distortion-less output corresponding to proposed amplifiers is 10-40V but at 10V the voltage gain for Circuit-2 is only 1.3376.

TABLE II
VARIATION OF MAXIMUM VOLTAGE GAIN, MAXIMUM CURRENT GAIN AND BANDWIDTH WITH TEMPERATURE

TEMP. °C	CIRCUIT-1 (Proposed Amplifier-1)			CIRCUIT-2 (Proposed Amplifier-2)		
	Maximum Voltage Gain $A_{V(MAX)}$	Maximum Current Gain $A_{I(MAX)}$	Bandwidth KHz	Maximum Voltage Gain $A_{V(MAX)}$	Maximum Current Gain $A_{I(MAX)}$	Bandwidth KHz
-30	130.141	59.564	530.157	324.440	149.354	432.248
-20	130.639	59.815	506.788	321.147	147.869	404.027
-10	131.004	60.004	501.223	317.879	146.392	385.865
0	131.248	60.136	484.402	314.640	144.925	356.078
10	131.383	60.217	468.082	311.436	143.471	325.957
27	131.388	60.248	440.671	306.071	141.033	274.700
50	131.007	60.108	400.315	9.676	4.4596	559.735
80	129.957	59.664	353.930	0.428	0.197	542.943

Variation of voltage gain, current gain and bandwidth with temperature is also measured and listed in Table-II. It is observed for proposed amplifier of Circuit-1 that the bandwidth gradually decreases with increasing temperature whereas maximum voltage and current gain both increases up to a critical temperature of 27°C thereafter decreases at higher temperature. However for proposed amplifier of Circuit-2, all the three performance parameters (voltage gain, current gain and bandwidth) decrease with increasing temperature up to a critical value of 27°C. Beyond this critical temperature both varieties of gains suddenly drop to considerably low value and continue to fall at increasing temperature whereas the bandwidth bears a zigzag nature i.e. increases at 50°C and again decreases at 80°C.

Variation of maximum voltage gain as a function of emitter resistance R_E is traced in Fig.3. Voltage gain decreases almost exponentially at increasing values of emitter resistance R_E for both the proposed amplifiers (Circuit-1 and Circuit-2) [1]-[2], [14]-[16], [19], [21]. It is to be noted that the Circuit-1 produces considerable voltage gain in 1-30KΩ range of R_E while this range for Circuit-2 is limited to 1-100KΩ. It is also observed that in absence of R_E or the RC network of R_E-C_E, the voltage gain falls to an insignificant value with the disappearance of phase reversal in output waveforms.

Similar to R_E, the maximum voltage gain of proposed amplifiers also depends highly on the collector resistance R_C [1]-[2], [10], [14]-[16], [19], [21]. Its variation with R_C is depicted in Fig.4. Voltage gain for both the amplifiers of Circuit-1 and

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Circuit-2 increases almost exponentially at increasing values of Collector resistance. However after 7KΩ of R_C for Circuit-1 and 10KΩ for Circuit-2 amplifier voltage gain falls down below unity with distorted output.

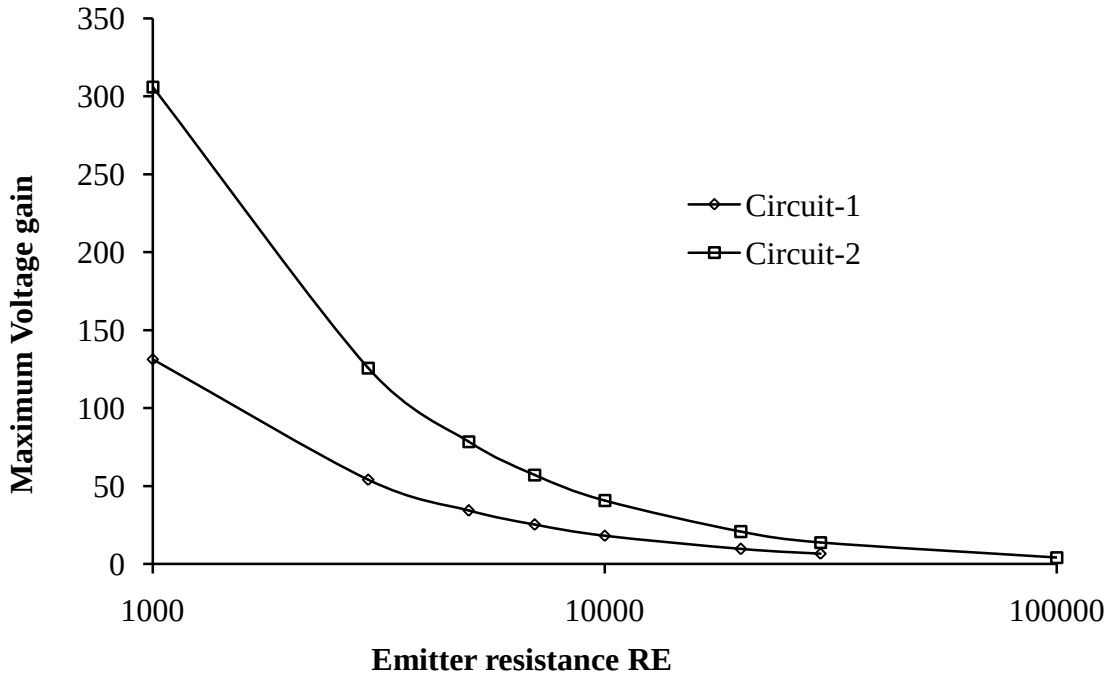

Fig.3. Variation of Maximum voltage gain with R_E

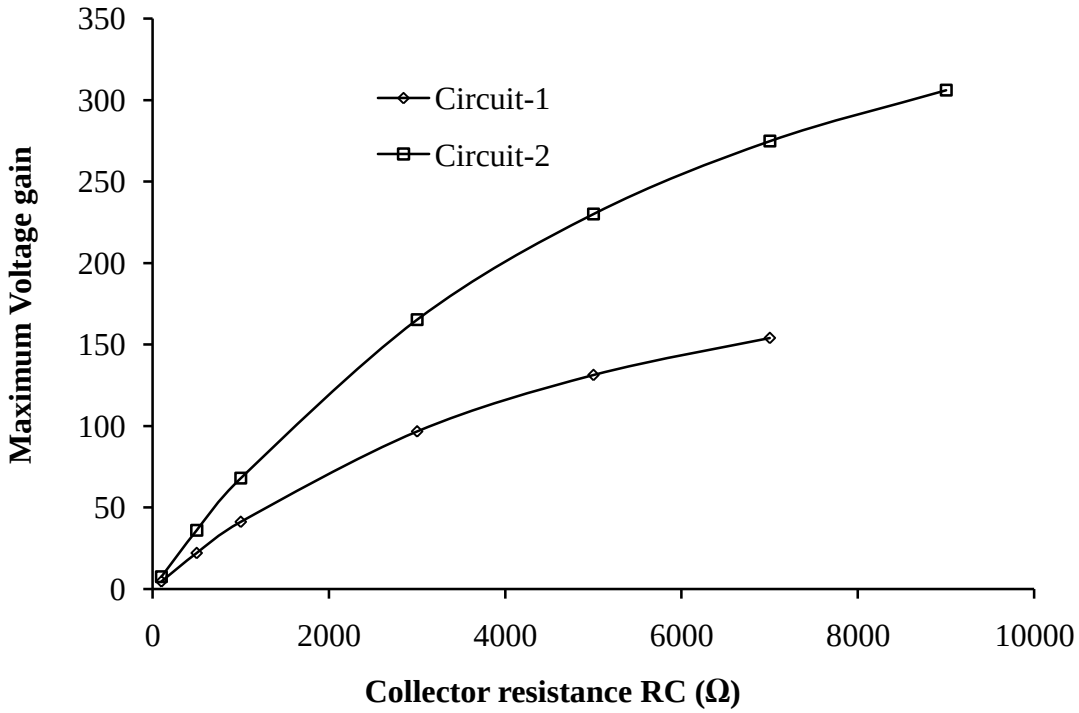

Fig.4. Variation of Maximum voltage gain with R_C

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In fact polarity of the composite unit of Darlington pair is determined by the driver device [21]. For example, a Darlington pair consisting NPN-BJT followed by N-Channel-JFET principally behaves like NPN-BJT driven Darlington unit. This is why the overall property of composite unit in proposed amplifiers (having BJT-JFET-BJT in Triple Darlington configuration) seems to be inclined more towards BJT (NPN) driven CE Darlington's system. Therefore the effect of R_E and R_C on the voltage gain (Fig.3 and Fig.4) for proposed amplifiers can be explained on the basis of r_e equivalent model of RC coupled CE Transistor configuration. This model suggests that the overall voltage gain of the proposed circuits can be estimated by $A_V \approx R_C/R_E$. Hence increasing emitter resistance R_E (at fixed R_C), the overall voltage gain A_V decreases whereas increasing R_C (at fixed R_E), the overall voltage gain A_V increases almost exponentially.

Variation of Maximum voltage gain with added resistances R_A and R_{AD} is shown in Fig.5. It is noticed that increasing the value of R_A, voltage gain increases leisurely for both the proposed amplifiers of Circuit-1 and Circuit-2. The Circuit-1 amplifier is found to produce distortion-less response in 500Ω-1MΩ range of R_A whereas this range for Circuit-2 amplifier is 1KΩ-100KΩ. After 1MΩ value of R_A for Circuit-1 and 100KΩ for Circuit-2 amplifier the respective output waveforms shows distortion. It is also noticed that in absence of added resistance R_A, voltage gain of both the amplifiers of Circuit-1 and Circuit-2 falls down to an insignificant value.

Similarly for increasing values of R_{AD}, voltage gain corresponding to both the proposed amplifiers initially increases nonlinearly, thereafter, it acquires a peak value and then falls down to a limiting point. Maxim of the voltage gain corresponding to R_{AD} for Circuit-1 amplifier is observed to be 133.155 at 25KΩ which falls down to 113.711 at 1MΩ. However for Circuit-2 the observed peak value of voltage gain is 307.474 at 7KΩ which climbs down to 294.833 at 25KΩ. Circuit-1 amplifier brings a distortion-less response in 2KΩ-1MΩ range of R_{AD} while this range of R_{AD} for Circuit-2 amplifier is 1KΩ-25KΩ.

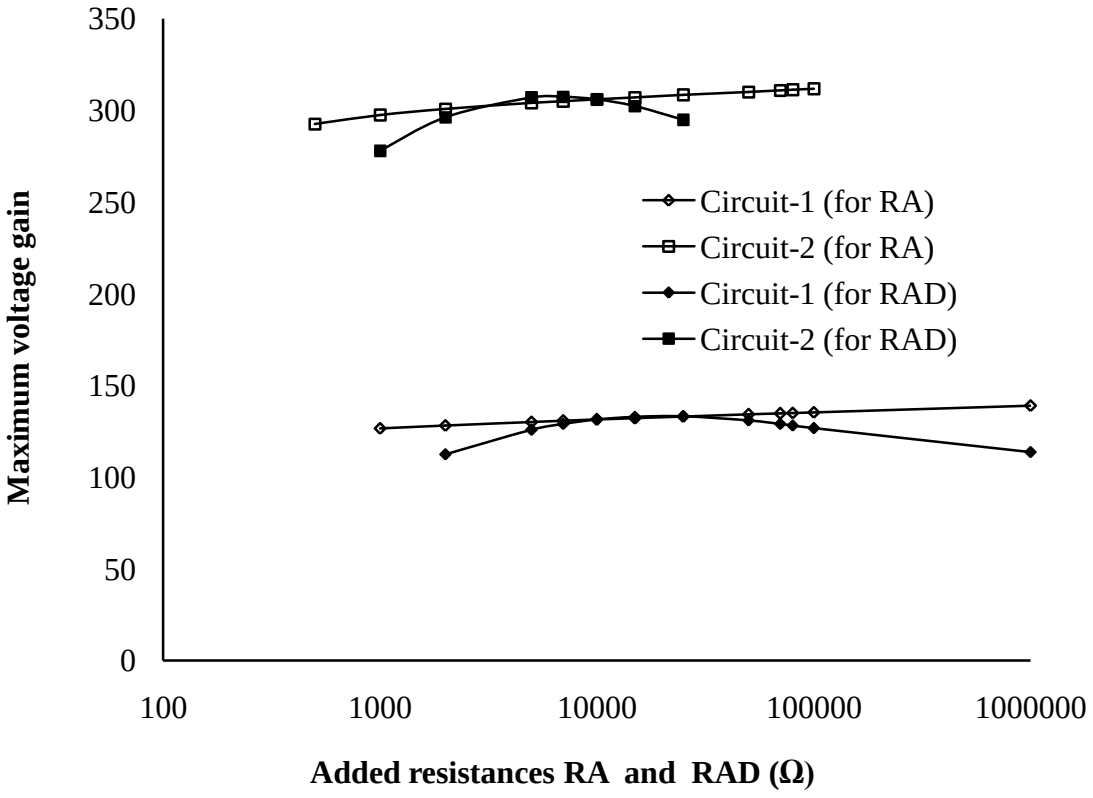

Fig.5. Variation of Maximum voltage gain with R_A and R_{AD}

It is observed that the voltage across added resistance R_{AD} increases while current through it decreases to a considerable amount when the value of R_{AD} is increased after a critical limit of 25KΩ for Circuit-1 and 7KΩ for Circuit-2. This in turn increases the forward biasing status of Base-Emitter junction of the transistor Q2. Due to this the current and voltage across R_E considerably increases and causes a significant reduction in the voltage across load resistance R_L and hence the overall voltage gain of the respective amplifiers.

It is also noticed that in absence of added resistance R_{AD}, maximum voltage gain drops to an insignificant value 3.19 for amplifier of Circuit-1with distortion in output waveforms whereas for Circuit-2 amplifier it drops to 110.27 in absence of R_{AD} with corresponding current gain 50.60 and 169.392KHz bandwidth (with f_L=75.541Hz and f_H=169.468KHz). However if R_A and R_{AD} both are simultaneously removed from the proposed circuits, voltage and current gains drop below unity and the output waveform clamps towards positive side of the reference axis.

During the qualitative analysis when biasing resistance R_1 of the potential divider network of Circuit-1 amplifier was removed, Voltage gain of the respective circuit dropped to 61.019, Current gain to 24.532 whereas bandwidth increased to 1.628MHz (with f_L=344.447KHz and f_H=1.972MHz) with significant increase in THD. However, when R_1 was removed from the amplifier of Circuit-2 its Voltage gain climbed down to 9.955, Current gain to 4.7201 whereas bandwidth increased to 6.210MHz (with f_L=98.764KHz and f_H=6.309MHz) with considerable rise in THD. On the other hand when R_2 was removed from the configuration of the proposed circuits, the maximum voltage and current gains of respective amplifiers climbed down below unity with undistorted output waveforms.

Variation of maximum voltage gain with load resistance R_L is also observed but not shown in form of figure. It is observed that voltage gain rises almost linearly to 100KΩ value of R_L for both the amplifiers and then tends to acquire a saturation level. This rising and saturation tendency of the voltage gain with R_L is well in accordance of the usual behaviour of small signal audio amplifiers [1]-[2], [14]-[16], [19].

IV. CONCLUSIONS

As a novel approach, a unique combination of BJT-FET-BJT is used in Triple Darlington configuration to explore two discrete circuits of small-signal amplifiers using RC coupling. At 1KHz input frequency, the proposed amplifier of Circuit-1 can effectively process small-signals ranging below 15mV in the frequency band of 83.954Hz to 440.755KHz whereas the proposed amplifier of Circuit-2 is able to process small-signals ranging below 4mV in 124.47Hz to 274.825KHz frequency band.

The proposed small-signal audio amplifiers are free from the problem of poor response of conventional small-signal Darlington pair or Triple Darlington amplifiers at higher order frequencies in the permissible frequency band.

With moderate range bandwidths, proposed amplifier of Circuit-1 generates only 0.84% harmonic distortion while the proposed amplifier of Circuit-2 generates 1.21% harmonic distortion but both the amplifiers simultaneously produces high voltage and current gains of considerable amount. High voltage as well as current gains of the proposed amplifiers logically set their power gain greater than unity. All these features together make these amplifiers fabulously unique in respective class of small signal audio amplifiers.

The proposed amplifiers show a considerable response for V_{CC}, R_E, R_C and R_L almost in the same way as is usually observed for small-signal RC coupled CE amplifiers. On the other hand the proposed amplifier of Circuit-1 provides an optimum performance in 1KΩ–1MΩ for additional biasing resistances R_A whereas this range for R_{AD} is 2KΩ–1MΩ. Similarly the optimum performance range for Circuit-2 amplifier corresponding to R_A is 500Ω–100KΩ while that for R_{AD} it is 1KΩ–25KΩ.

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Biography

SachchidaNand Shukla received his M.Sc. and Ph.D. Degrees in Physics (Electronics) from Dr. Ram Manohar Lohia Avadh University, Faizabad in 1988 and 1991 respectively. Presently he is working as Associate Professor in the Department of Physics and Electronics of Dr. Ram Manohar Lohia Avadh University, Faizabad, U.P., India and actively engaged in researches related to Circuit designing and simulation. In last five years he published 30 research papers in International/National journals and Conference Proceedings on various topics of his current research interest.

Susmrita Srivastava received her M.Sc. degree in Electronics from Department of Physics and Electronics of Dr. Ram Manohar Lohia Avadh University, Faizabad, U.P., India in 2008. Presently she is pursuing for her Ph.D. degree in Electronics and published 12 research papers on various topics of Circuit designing and simulation in International /National journals and Conference Proceedings.