ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 7, July 2016

A Novel Thirteen-Level Inverter Using a Single DC Source

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ABSTRACT:A novel thirteen-level inverter is proposed in this paper. It is based on the PUC inverter; however, whereas the latter makes uses of separate DC sources, the proposed inverter is constituted of two series-connected capacitors. This offers the benefit of combining advantages of NPC and PUC inverters. It, also, allows the possibility of generating thirteen voltage levels while using a single DC source. The proposed inverter has, hence, a reduced impact on loads systems resulting on a good energetic efficiency while using an optimized count of switches and passive components. A hysteresis control technique is designed to draw a nearly sinusoidal load current and voltage which allows avoiding use of expensive and bulky filters. The whole system was performed in Matlab Simulink environment. The proposed system was verified through simulation.

KEYWORDS: Multilevel Inverter, PUC topology, Harmonics, Hysteresis Control

I.INTRODUCTION

Classical two level inverters produce a huge amount of harmonics which results on a high waveforms distortion. The latter can harm loads once bulky and expensive filters are not used. Hence, in this kind of technology, inverters are considered as polluting converters which requires additional hardware to operate in an unpolluted environment.

Multilevel inverters have been proposed to palliate this drawback. By the advent of the nonpolluting technology, three level converters were proposed. Their total harmonics distortion was limited; however, the use of filters is still required albeit their sizes are becoming smaller.

Researches have been focused into developing converters which have the ability to synthesize waveforms with large number of voltage levels [1-6]. This allows improving harmonics spectrum in order to fulfill standards without additional investment. It allows, by the same, to attain high voltages by reducing the semiconductors stress. The power conversion is then performed with high energetic efficiency.

The multilevel Packed U Cells (PUC) topology was first proposed in [4]. It can be classified as a mid-point between the flying capacitor [5] and the cascaded H-bridge inverters topologies [6]. Moreover, it makes use of small power devices count while generating large voltage levels.

The 7-Level PUC [7-10] converter makes use of six power devices and two separated DC sources. Once two power switches and one separated DC source are added, the PUC topology generates, then, fifteen voltage levels. The proposed converter generates, however, thirteen but it offer the advantage of a DC-bus based on series-connected sources. The hysteresis control technique has proven to be suitable solution for all the applications of current controlled voltage source inverters where performance requirements are more demanding, such as active filters, drives and high-performance ac power conditioners.

The proposed converter associated to the hysteresis control technique allows drawing a nearly sinusoidal current with a smooth voltage waveform. The reduced harmonics distortion results on a high energetic efficiency of the power inverter. Dynamics of the proposed system were verified through simulation performed in Matlab Simulink environment.

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II.PRESENTATION OF THE PROPOSED INVERTER

The proposed inverter has several configurations in which eight power switches are used. Figure 1.a presents a configuration in which Three DC sources are used, whereas, the configuration of figure 1.b makes use of two DC sources and two capacitors. On the other side, in figure 1.c, two DC sources and one capacitor are used. The very competitive configuration is depicted in figure 1.d.

The possible operating states are shown in figure 2. One can remarks the two redundant states, 7 and 7', which represents the zero voltage. The operation sequence of the proposed inverter describes the thirteen attainable voltages. Let E1 and E2 be equal to 150V, whereas, E3 is equal to 100V. Therefore, the DC bus is equal to 300V. The AC load is thereby fed by thirteen levels whose values are presents in table 1.

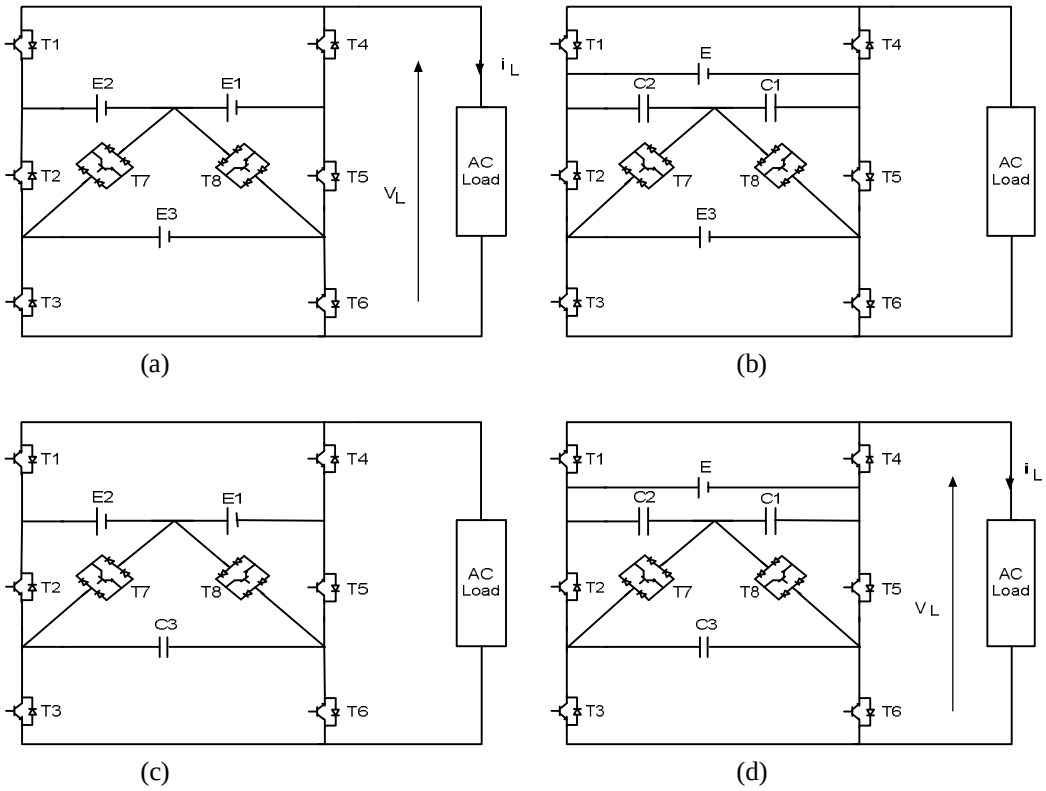

Figure 1. The proposed multilevel inverter with: (a) three DC sources required (b) two DC sources and two capacitors required (c) two DC sources and one capacitor required (d) one DC source and three capacitors required

Table 1. Switching table of the proposed inverter

State	DC sources combination	Load voltage value (V)	Switches pulses							
			T1	T2	T3	T4	T5	T6	T7	T8
1	E1+E2	300	1	0	0	0	1	1	0	0
2	E2+E3	250	1	0	0	0	0	1	1	0
3	E1+E2-E3	200	1	0	1	0	1	0	0	0
4	E2	150	1	0	0	0	0	1	0	1
5	E3	100	1	1	0	0	0	1	0	0
6	E2-E3	50	1	0	1	0	0	0	0	1
7	0	0	0	0	0	1	1	1	0	0
8	E3-E1	-50	0	0	0	1	0	1	1	0
9	-E3	-100	0	0	1	1	1	0	0	0
10	-E1	-150	0	0	1	1	0	0	1	0
11	E3-E1-E2	-200	0	1	0	1	0	1	0	0
12	-E1-E3	-250	0	0	1	1	0	0	0	1
13	-E1-E2	-300	0	1	1	1	0	0	0	0

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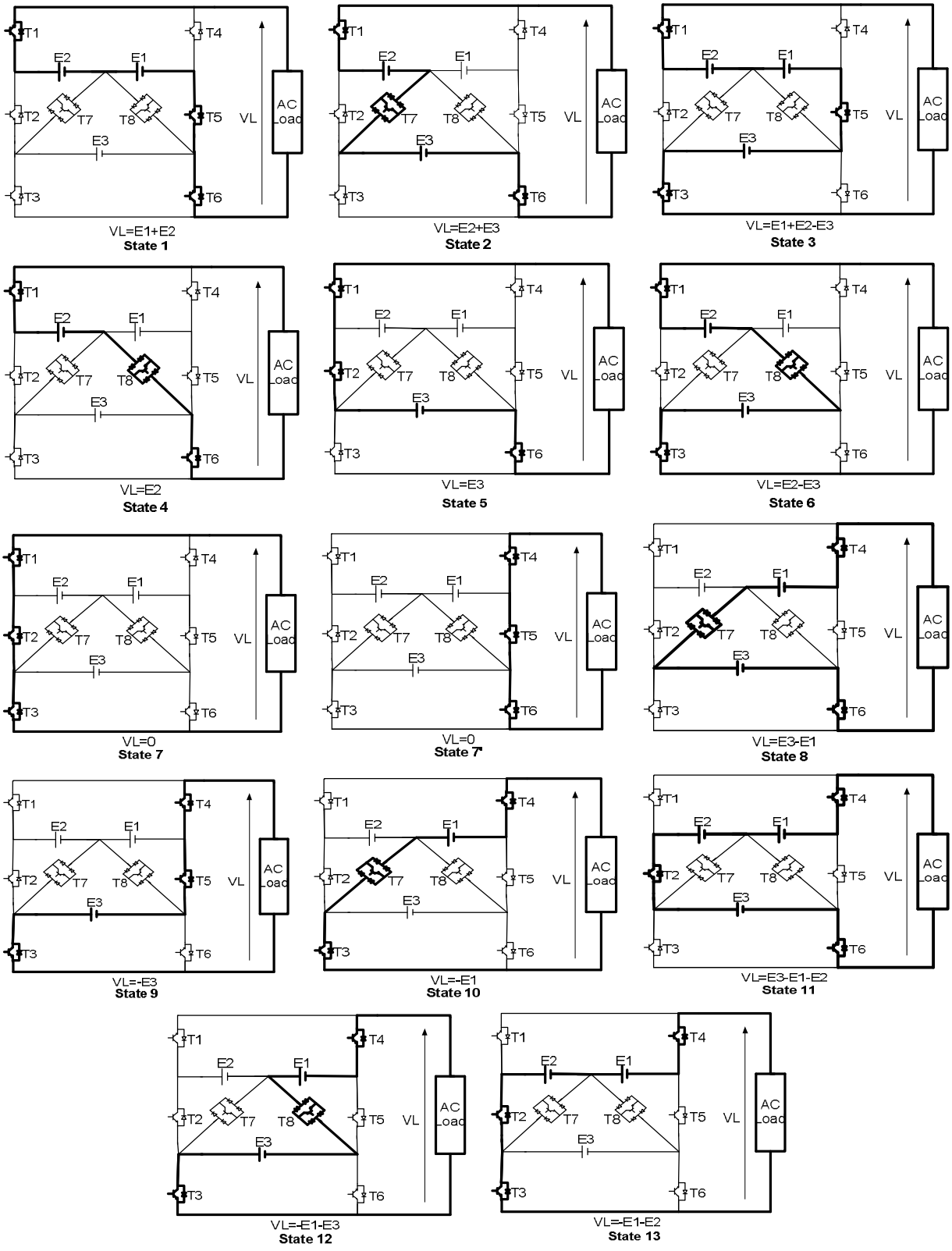

Figure 2. One cycle operating states of the proposed inverter

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III.CONTROL STRATEGY OF THE PROPOSED INVERTER

The study wil be limited to inverter of figure 1.d. This is due to the fact that this inverter is very optimized. It uses only a single DC source while generating thirteen voltage levels. The current load has to be maintained into twelve bands. The higher the number of bands, the more the load current will be sinusoidal. The actual value of load current is compared to its set-point in order to apply the appropriate voltage among the thirteen possible ones. In fact, the higher the error, the higher the applied voltage, and vice-versa. This procedure allows the load current to quickly pursue its set-point. The gate pulses of the power devices is subsequently given by the switching table depicted in table 1.

Figure 3 illustrates the proposed control technique. In this figure, « h » refers to the hysteresis band, whereas, « Δi » refers to the difference between actual load current and its reference. The « x » axis is subdivided into twelve bands while « y » axis is constituted of thirteen states. The control technique operates in two quadrants; the first applies positive output voltage, however, a negative voltage is applied in the second.

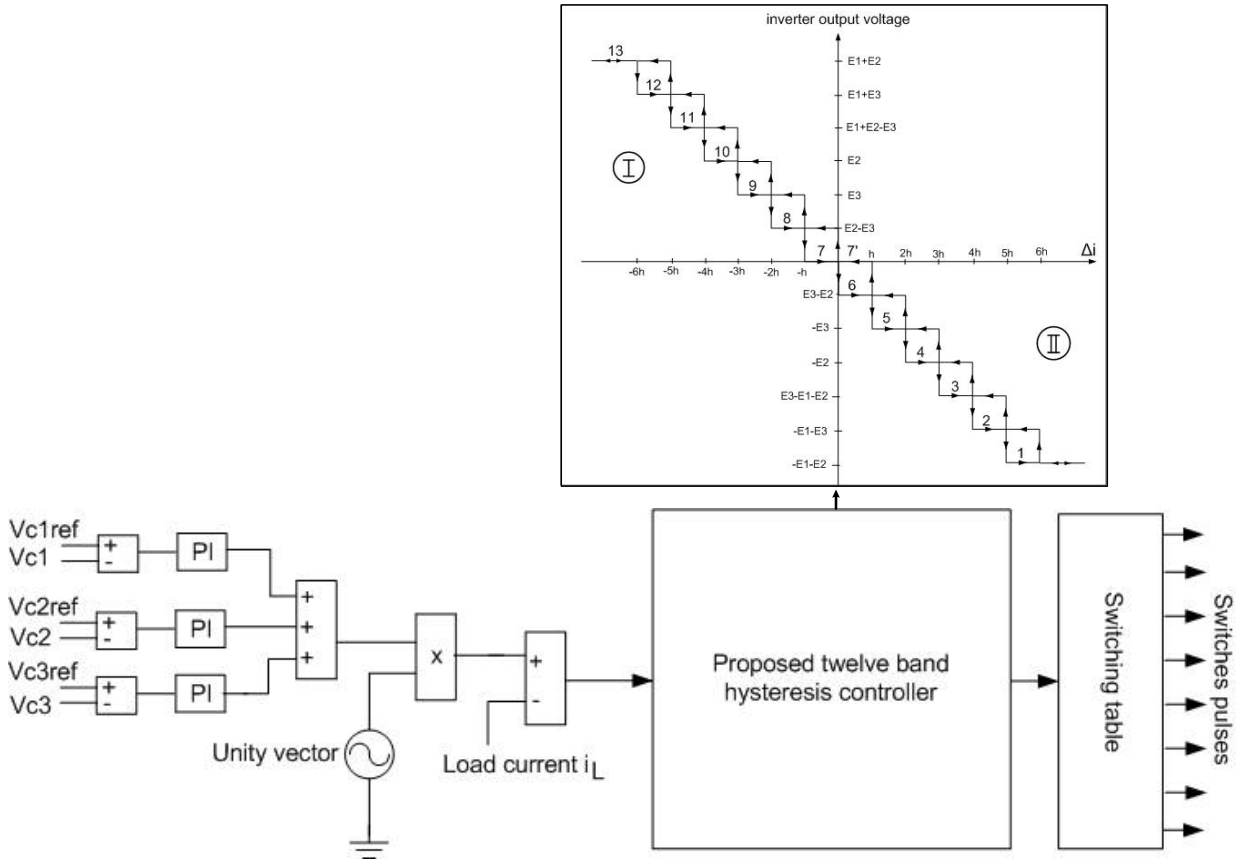

Figure 3.the proposed balancing technique of the proposed inverter

The AC load voltage reference can be generated by the following equation:

$$V_{an} = k_{p1}\tilde{i}_L + k_{i1}\int \tilde{i}_L dt \quad (1)$$

Where: $\tilde{i}_L = i_L^* - i_L$, i_L^* is the load current set-point.

The capacitor voltage is regulated using a PI controller such that:

$$i_L^* = \left(k_{p1}\tilde{v}_1 + k_{i1}\int \tilde{v}_1 dt\right) + \left(k_{p2}\tilde{v}_2 + k_{i2}\int \tilde{v}_2 dt\right) + \left(k_{p3}\tilde{v}_3 + k_{i3}\int \tilde{v}_3 dt\right) \quad (2)$$

Where: $\tilde{v}_1 = v_{c1}^* - v_{c1}$, $\tilde{v}_2 = v_{c2}^* - v_{c2}$, $\tilde{v}_3 = v_{c3}^* - v_{c3}$, v_{c1}^*, v_{c2}^* and v_{c3}^* are the capacitors voltages references.

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In order to generate thirteen levels across the load, the voltage set-point of capacitor C3 must be equal to the third of the DC bus voltage reference. However, the voltages of capacitors C1 and C2 has to be controlled to the half of the DC bus voltage. The DC bus is constituted from capacitors C1 and C2, whereas, C3 is considered as an auxiliary DC bus. As seen in the latter section, the thirteen voltage levels are therefore obtained using table 1. The proposed control technique is based on the twelve band hysteresis approach. Therefore, once actual load current is lower that its reference, a positive voltage is applied across the load. This leads to the rapprochement of the actual value and its set-point. Thereafter, the positive voltages (sector I in figure 3) are applied when the current error (Δi) is negative. Contrariwise, the negative voltages (sector II) are applied once the current error is positive.

IV. RESULT AND DISCUSSION

The simulation parameters are given in table 2.

Table 2. Simulation parameters

Load resistance	10Ω
Load inductance	10mH
Capacitors value	2000μF
Hysteresis band value	0.15

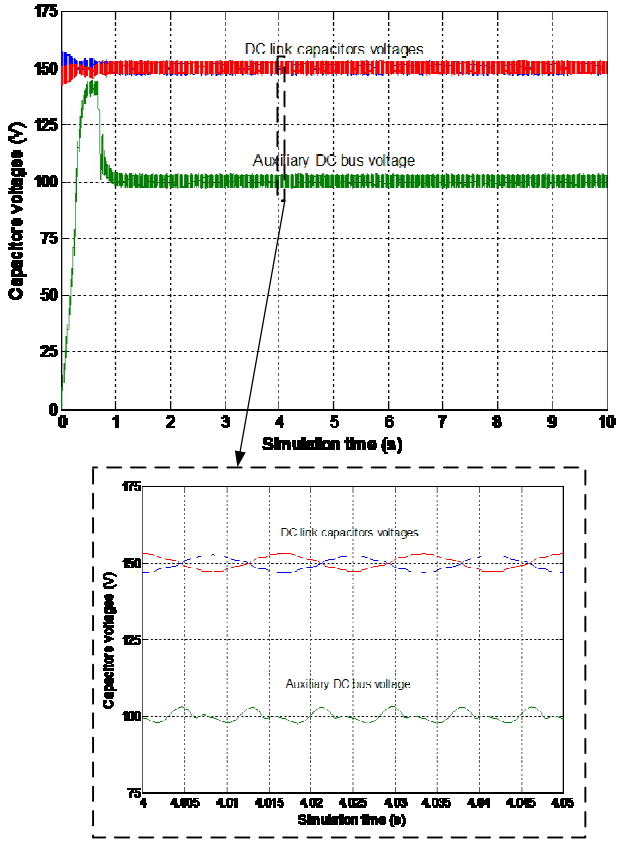

Figure 4. Capacitors voltages evolution

The DC bus voltage is chosen to be 300V so that the references of the different capacitors are set to 150V, for C1 and C2, and 100V for C3. Figure 4 illustrates that the voltages of the principal and auxiliary DC buses are well controlled

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around their set-point. Figure 5 shows the load voltage waveform. This staircase voltage allows drawing a perfect load current which is depicted in figure 6.

The harmonics contents are very reduced which means that load current is perfectly sinusoidal as depicted in figure 7. The total harmonics distortion is around 0.45% as shown in figure 7. A loop effect is given to illustrate the harmonics contents.

The switching frequency is sporadic, which is the main characteristic of any hysteresis controller. However, it can be limited at low frequencies by acting on the hysteresis band.These waveforms are obtained without using any filters which results on a high energetic efficiency.

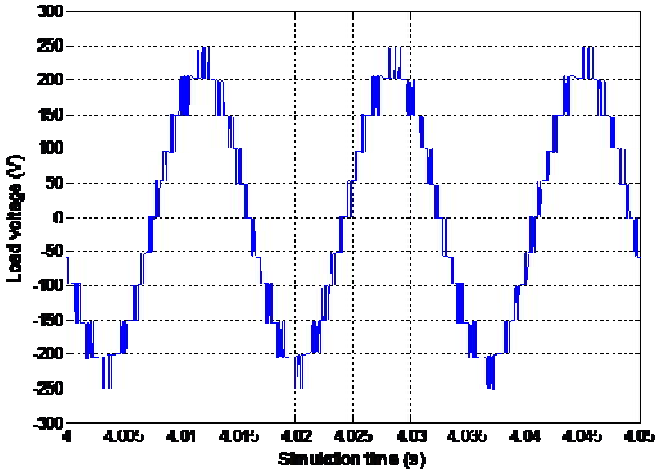

Figure 5. Load voltage waveform

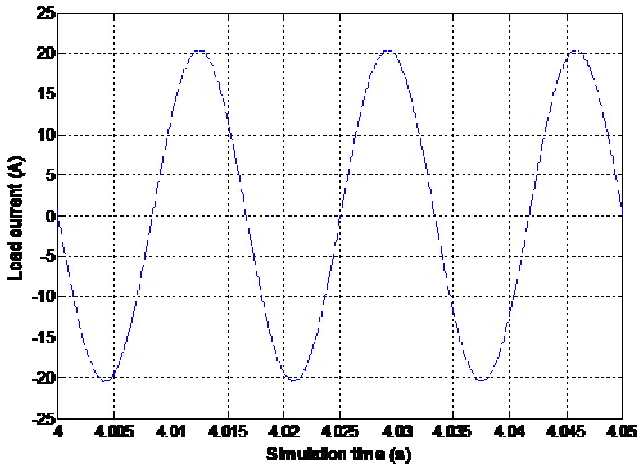

Figure 6. Load current waveform

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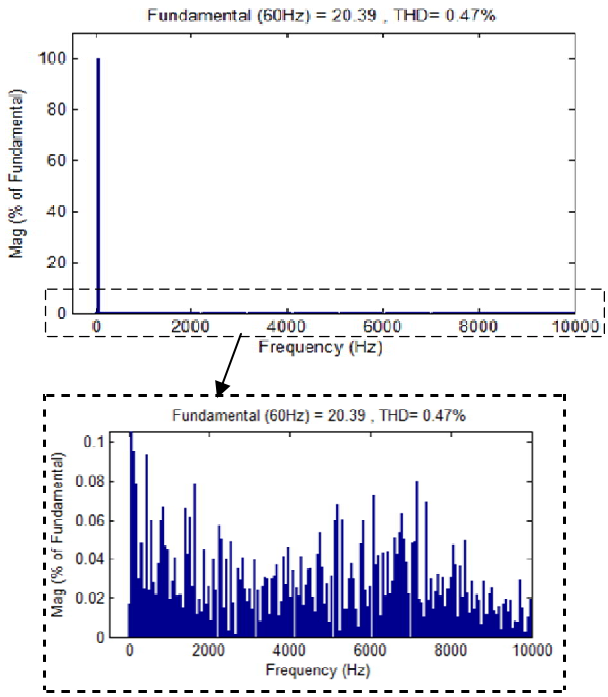

Figure 7. Harmonics spectrum of load current with loop effect

V.CONCLUSION

A novel thirteen level inverter is proposed in this paper. Associated to the proposed control technique, it allows a nearly sinusoidal current with a smooth voltage waveform while using a single DC source. With such waveforms, which are obtained without using any filters, the power conversion is performed with high energetic efficiency. Dynamics of the proposed system were verified by simulation results.

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