ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 9, September 2013

A PHASE SHIFTED GATING TECHNIQUE FOR THE SEMI BRIDGE LESS AC-DC CONVERTER WITH POWER FACTOR CORRECTION

MK.Jayavelu[1], K.Sarbham[2], G.Jayakrishna[3]

PG Student [PE&ED], Dept, of EEE, Siddhartha Engg College, Puttur, A.P, India[1]

Asst professor, Dept.of EEE, Siddhartha Engineering College, Puttur, A.P.India[2]

Professor, Dept.of EEE, Siddhartha Engineering College, Puttur, A.P, India[3]

ABSTRACT: the conventional method of converter boost the input voltage but power factor correction cannot be achieved properly in the input side but in the proposed semi bridge less converter boost the input voltage and achieved the power factor correction. The proposed converter features is higher efficiency, eliminate the input ripple. The detailed converter description, steady-state operation and experimental results of both conventional and proposed method are presented and analysed. The converter is applicable for the automotive level I and II but is ideally suitable for level I residential charging application.

Key Words: AC–DC power converters, boost converter, bridgeless power factor correction (PFC), current sensing, and plug-in hybrid electric vehicle (PHEV) charger.

I.INTRODUCTION

A Plug-in-hybrid electrical vehicle (PHEV) is a hybrid vehicle with a storage system that can be recharged by connecting a plug to an external power source. The power from the external is given to conventional circuit it covert AC to regulated DC supply and this DC supply is given to the battery storage system for storing the electrical energy, but main drawback of these conventional topologies is power factor correction not achieved properly in the input side but proposed boost converter eliminate the above drawback and this converter efficiency also high. These paper numbers of boost topologies listed below those are interleaved boost converter, bridgeless boost converter, the dual boost converter, the semi-bridgeless boost converter and the proposed phase-shifted semi-bridgeless (PSSB) boost converter.

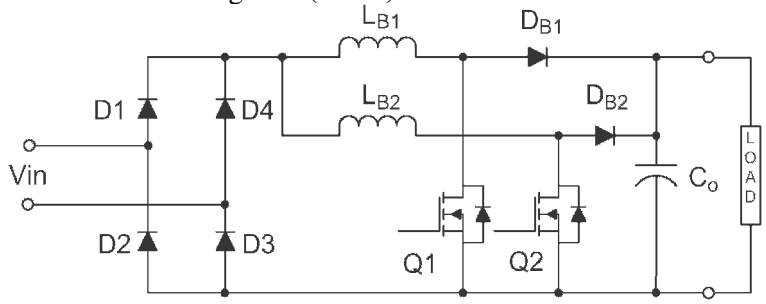

Fig .1 Interleaved PFC boost topology

The two stage cascaded PFC ac-dc and dc-dc converters is the common choice for PHEV battery chargers, where the power rating is high, lithium-ion batteries are used. But in single stage approach lead acid batteries are suited because it has large ripples in the output current.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 9, September 2013

II. INTERLEAVED PFC:

Interleaved boost converter is shown in Fig.1.The circuit contain four input diodes D1,D2,D3 and D4.In positive half cycles D1 and D3 are conducting and In negative half cycles D2 and D4 are conducting. So that input current is sum of the two inductor current as shown in fig. The input two inductor ripple currents are out of phase. Due to boost switching action input ripples are eliminated. Furthermore switching of the converter (two MOSFETs) are 180 deg out of phase with single PFC boost. The most drawback of this circuit is introduces smaller input current ripples and resultant heat management issue for the input diodes bridge rectifier. The capacitor used for the circuit is to eliminate the higher ripples.

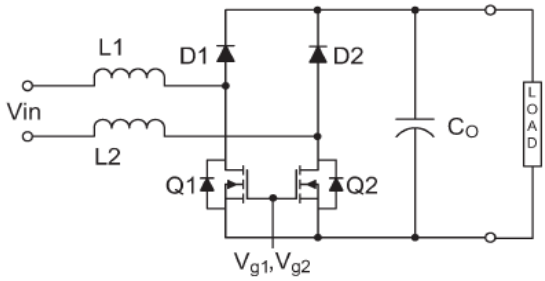

Fig.2 Bridgeless PFC boost Topology.

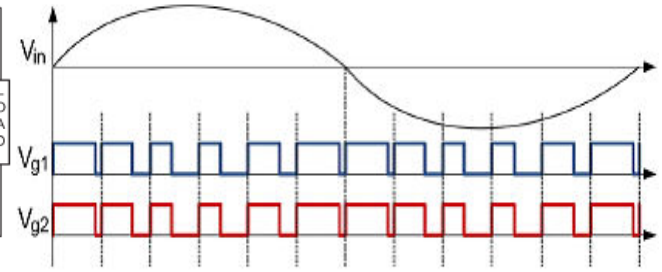

Fig.3 Gating scheme for the bridgeless PFC boost

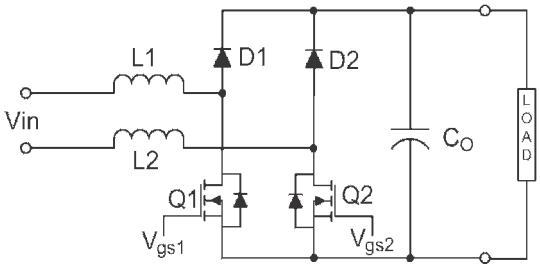

Fig.4 Dual-boost PFC topology.

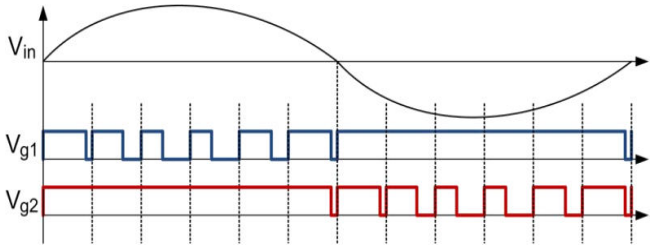

Fig.5 Gating scheme for the dual-boost topology.

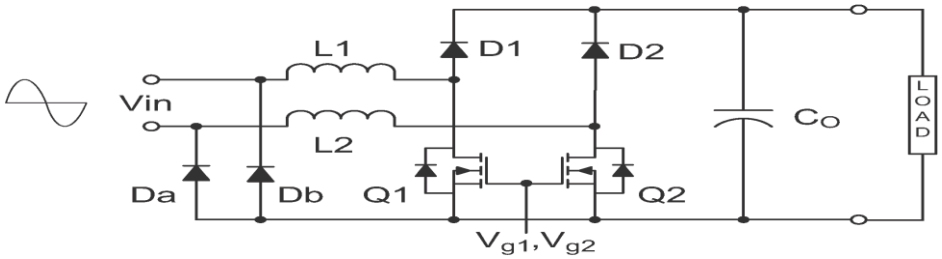

Fig .6 Semi bridgeless PFC boost topology.

III. BRIDGELESS PFC:

The bridgeless boost topology, as shown in Fig.2, is the second topology considered for this application.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 9, September 2013

Here gating signals are identical shown in fig 3.the two inductorsL1 and L2 at the input side are used to boost up the input voltage. This boost converter solves the heat management of the input diode rectifier bridge, but it introduces increased EMI [22]-[24].Another disadvantage this topology is the floating input line with respect to the PFC stage ground, which makes it impossible to sense the input voltage without a low-frequency transformer. The operation of this converter is same as the dual-boost which can be described in below.

IV. DUAL BOOST PFC:

The dual-boost converter, as shown in Fig.4. The operation can be analyzed in two stages When the AC input voltage goes positive, the gate of S1 is driven high and current flows from the input through the inductor, storing energy. When S1 turns off, energy in the inductor is released as current flows through D1, through the load and returns through the body diode of S2. During the-off time, the current through the inductor L (i.e., during this time the inductor discharges its energy) flows in to the boost diode D1 and close the circuit through the load. During the negative half cycle circuit operation is mirrored as shown in S2 turns on, current flows through the inductor, storing energy. When S2 turns off, energy is released as current flows through D2, through the load and back to the mains through the body diode of S1 back to the input mains. Note that the two Power MOSFETs are driven synchronously. The dual boost topology reduces the gate loss, and at light loads. The light-load efficiency improvement comes at the expense of the cost of an additional driver and increased controller complexity.

V. SEMI BRIDGELESS PFC:

The semi-bridgeless configuration, as shown in Fig.6 In addition to diodes Da and Db which are slow recovery diodes, resulting in two dc/dc boost circuits, one for each half-line cycle. During a positive half line cycle, the first dc/dc boost circuit, L1 -D1–Q2 is active through diode Db, which connects the ac source to the output ground. During a negative half-line cycle, the second dc/dc boost circuit, L2 -D2-Q1, is active through diode D3, which connects the ac source to the output ground. It should be noted that switches Q1and Q2, in both bridgeless PFC boost rectifiers can be driven with the same PWM signal, which significantly simplifies the implementation of the control circuit. The drawback of the bridgeless PFC boost rectifier in is that it requires an additional gate-drive transformer.

VI. PROPOSED CONVERTER:

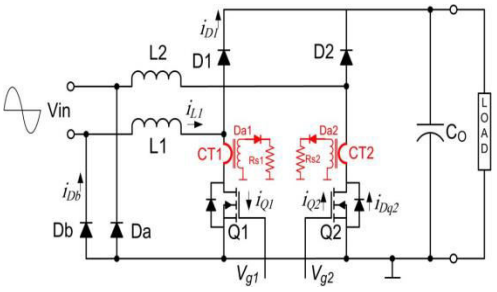

Fig .7 Proposed PSSB PFC boost topology.

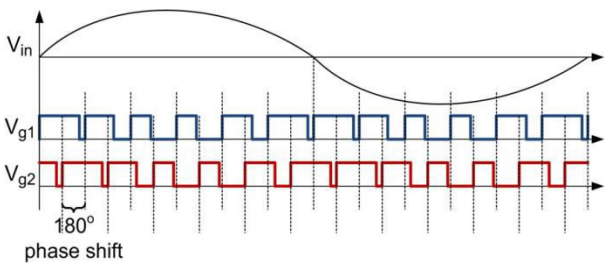

Fig.8 Gating scheme MOSFETs

The PSSB topology shown in Fig. 7 is proposed as a solution to simplify current sensing in bridgeless PFC boost applications using the current synthesizer sensing method [27]. The gating signals of the

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 9, September 2013

MOSFETS are 180 deg out of phase shown in Fig.8, these proposed topologies over come all the above problems like input electromagnetic interference (EMI), heat management issue for the input diode bridge rectifiers and power factor correction problems. The main purpose of gate drive transformer is used for the proposed method is used to increase the power rating and isolate the circuit if any fault occur on the input side. The proposed converter steady state operation is described in the below section.

VII.CONVERTER STEADY-STATE OPERATION:

To analyze the circuit operation, the input line cycle is separated into positive and negative half-cycles, as explained below. In addition, the detailed circuit operation depends on the duty cycle. Positive half-cycle operation is provided for D > 0.5 in Section 1 and D < 0.5 in Section 2.

A. Positive Half-Cycle Operation:

Referring to Fig.7, during the positive half-cycle, when the ac input voltage is positive, Q1 turns on and current flows through L1 and Q1 and continues through Q2 and then L2, returning to the line while storing energy in L1 and L2. When Q1 turns off, the energy stored in L1 and L2 is released as current flows through D1, through the load, and returns through the body diode of Q2/partially through Db back to the input.

B. Negative Half-Cycle Operation:

Referring to Fig. 7, during the negative half-cycle, when the ac input voltage is negative, Q2 turns on and current flows through L2 and Q2 and continues through Q1 and then L1, returning to the line while storing energy in L2 and L1. When Q2 turns off, the energy stored in L2 and L1 is released as current flows through D2, through the load, and returns split between the body diode of Q1 and Da back to the input.

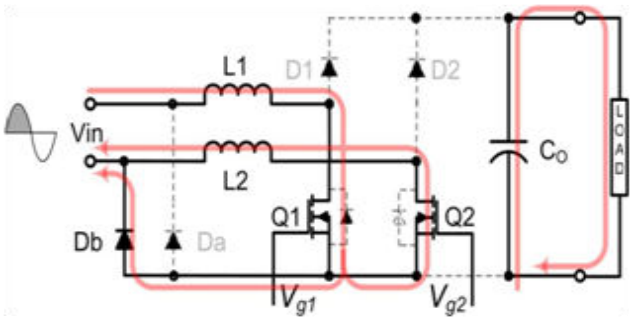

Fig: 9: Intervals 1 and 3:Q1 and Q2 on

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 9, September 2013

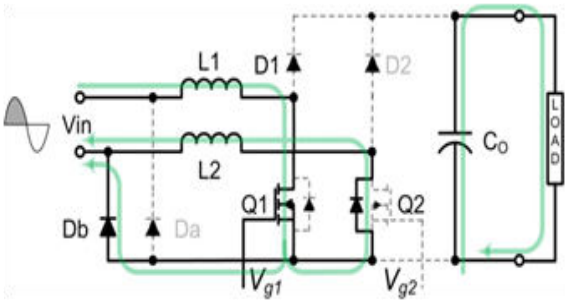

Fig: 10: interval 2:Q1on body diode Q2 conducting.

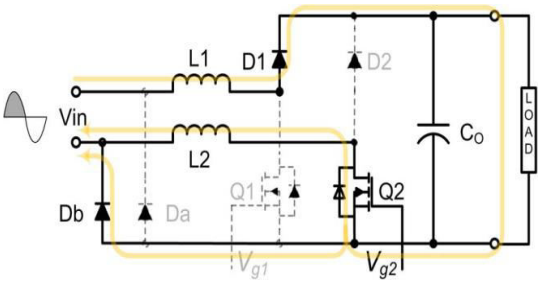

Fig. 11. Interval 4: Q1 off and Q2 on.

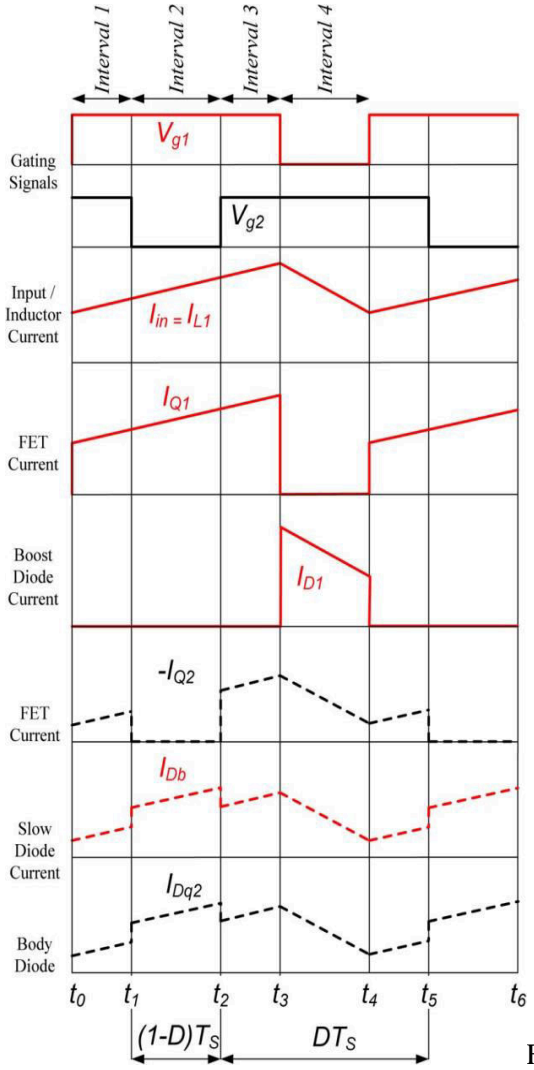

Fig. 12 PSSB boost converter steady state Waveform when D>0.5

C. Detailed Positive Half-Cycle Operation and Analysis for Duty cycle > 0.5:

The detailed operation of the proposed converter depends on the duty cycle. During any half-cycle, the converter duty cycle is either greater than 0.5 (when the input voltage is smaller than half of the output voltage) or smaller than 0.5 (when the input voltage is greater than half of the output voltage). The three unique operating interval circuits of the proposed converter are provided in Figs. 9–11 for duty cycles larger than 0.5 during the positive half-cycle input. Waveforms of the proposed converter during positive half-cycle operation with $D > 0.5$ are shown in Fig.12. To simplify the analysis, it is assumed that the current splits between the bridge diode, the body diode, and the MOSFET channel equally. The intervals of operation are explained here.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 9, September 2013

Interval 1 [$t_0 - t_1$]: At t_0 ,Q1/ Q2 are on, as shown in Fig.9 During this interval, the current in series inductances L1 and L2 increases linearly and stores the energy in these inductors. The energy stored in Co provides energy to the load. The return current is split among Db, Dq2, and Q2.

Interval 2 [$t_1 - t_2$]: At t_1 , Q1 is on, and Q2 is off, as shown in Fig.10 During this interval, the current in series inductances L1 and L2 continues to increase linearly and store the energy in these inductors. The energy stored in Co provides the load energy. The return current is split only between Db and Dq2.

Interval 3 [$t_2 - t_3$]: At t2, Q1/Q2 are on again, and interval 1 is repeated, as shown in Fig. 9. During this interval, the current in series inductances L1 and L2 increases linearly and stores the energy in these inductors. The return current is again split among Db, Dq2, and Q2.

Interval 4 [$t_3 - t_4$]: At t3, Q1 is off, and Q2 is on, as shown in Fig. 11. During this interval, the energy stored in L1 and L2 is released to the output through L1, D1, partially Q2, Dq2, L2, and Db.

D. Detailed Positive Half-Cycle Operation and Analysis for Duty cycle < 0.5:

The three unique operating interval circuits of the proposed converter are given in Figs. 13–15 for duty cycles less than 0.5 during the positive half-cycle. The waveforms of the proposed converter during these conditions are shown in Fig. 16. The intervals of operation are explained here.

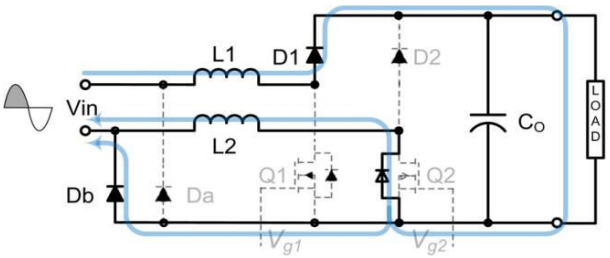

Fig. 13. Intervals 1and 3: Q1 and Q2 off, body diode of Q2 conducting.

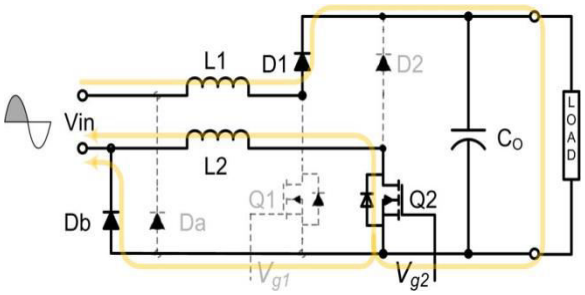

Fig. 15. Interval 4: Q1 off and Q2 on.

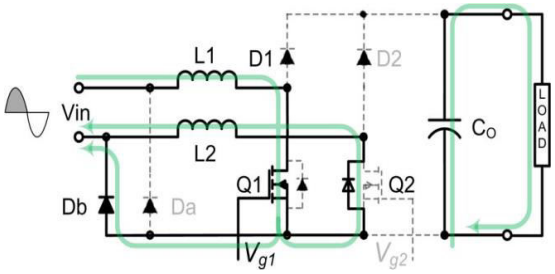

Fig. 14 Interval 2: Q1 on, body diode of Q2 conducting.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 9, September 2013

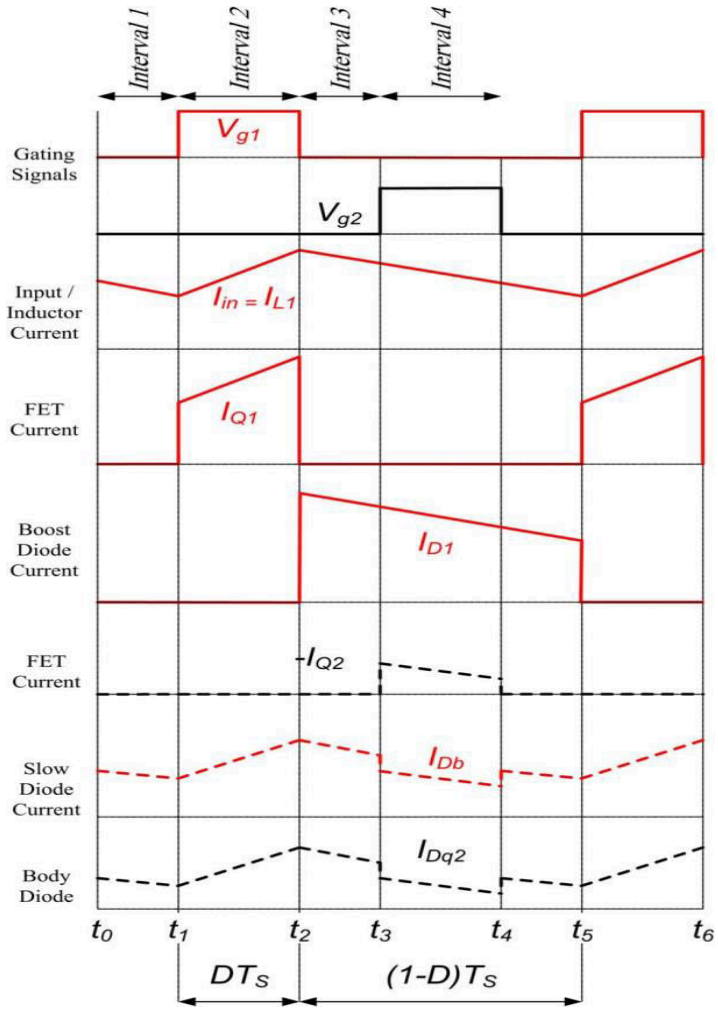

Fig. 16 PSSB boost converter steady-state wave form for $D < 0.5$

Interval 1 [$t_0 - t_1$]: At t_0, Q1/ Q2 are off, as shown in Fig. 13. During this interval, the energy stored in L1 and L2 is released to the output through L1, D1, partially Dq2, L2, and Db.

Interval 2 [$t_1 - t_2$]: At t_1 , Q1 is on, and Q2 is off, as shown in Fig. 14. During this interval, the current in series inductances L1 and L2 continues to increase linearly and store the energy in these inductors. The energy stored in Co provides energy to the load. The return current is split only between Db and Dq2.

Interval 3 [$t_2 - t_3$]: At t_2 , Q1/Q2 are off again, and interval 1 is repeated, as shown in Fig. 13. During this interval, the current in series inductances L1 and L2 decreases linearly, and the energy in these inductors are released. The energy stored in L1 and L2 is released to the output through L1, D1, partially Dq2, L2, and Db.

Interval 4 [$t_3 - t_4$]: At t_3 , Q1 is off, and Q2 is on, as shown in Fig. 15. During this interval, the energy stored in L1 and L2 is released to the output through L1, D1, partially Q2, Dq2, L2, and Db.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 9, September 2013

The operation of the converter during the negative input voltage half-cycle is similar to the operation of the converter during the positive input voltage half-cycle.

VIII.EXPERIMENTAL RESULTS:

The proposed PSSB boost PFC converter was designed In MATLAB R2009a software.

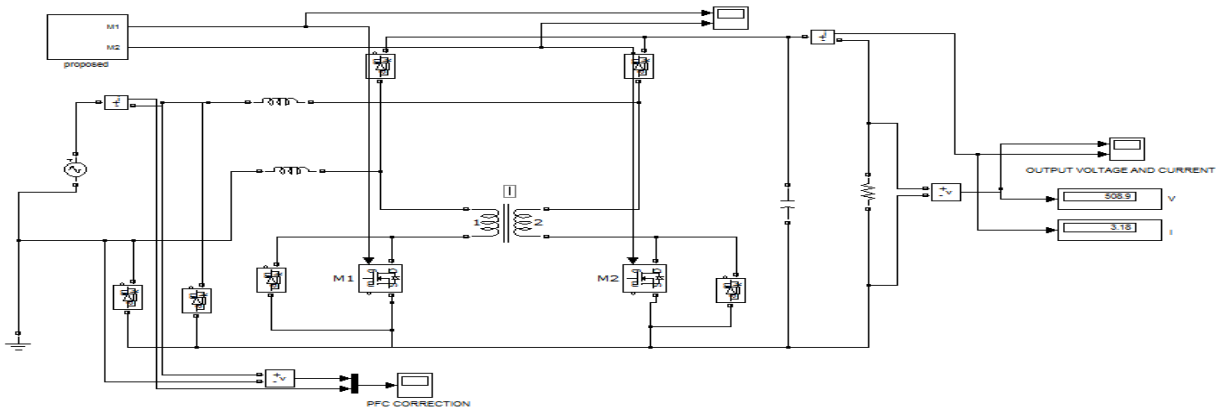

Fig .17 proposed methods of unique current-sensing circuits implemented with the bridgeless PFC boost topology.

The efficiency of the phase-shifted bridgeless boost converter, interleaved boost converter, and conventional bridgeless boost converter are provided and in Fig.17 120V to 240 V input at 60Hz MOSFET1 & MOSFET2 operating at 180 Deg out phase shift operation. The duty cycle of 0.6 to1% of each MOSFET switching's. In proposed method the two MOSFETs are operated at 180 deg out of phase it enables the usage of advanced current synthesizing method. This phase shifting techniques cannot be used either the bridgeless or dual boost topology because all controllers available for these topologies require full input current shape sensing. Finally proposed topology achieved the power factor correction at input side and boosts the output voltage with higher efficiency at the output side.

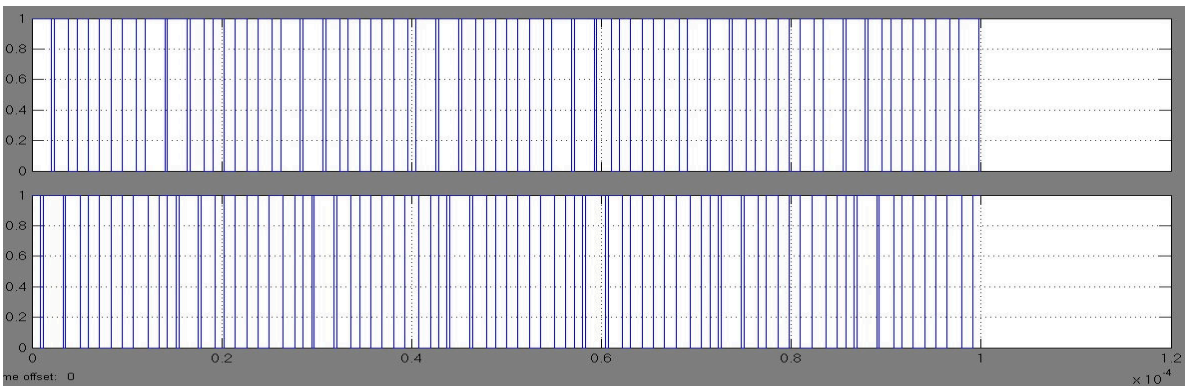

Fig.18 The proposed MOSFET1 & MOSFET2 switching sequence.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 9, September 2013

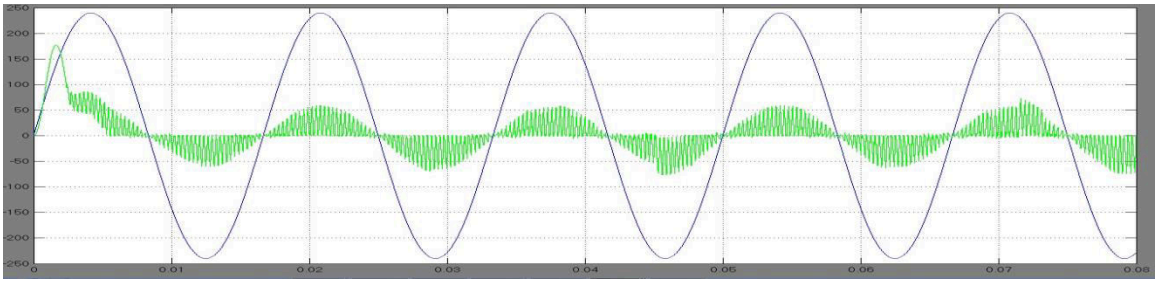

Fig.19 the Proposed PSSB PFC boost converter input voltage and current waveform.

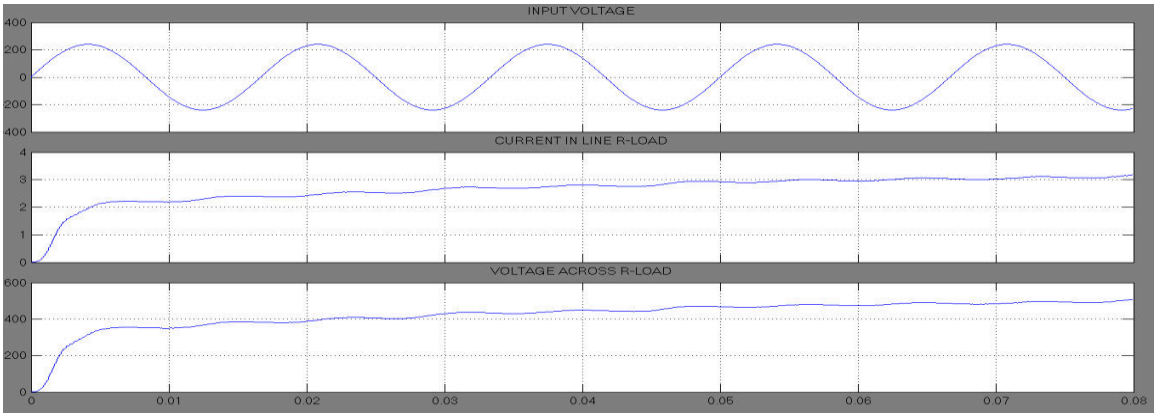

Fig.20 The Proposed methods of unique current-sensing circuits implemented with the bridgeless PFC boost topology final result.

IX.CONCLUSION

A high-performance PSSB ac–dc boost PFC converter topology has been proposed to simplify t he current-sensing technique for t he semi-bridgeless PFC converter. The converter features high efficiency at light-load and low-line conditions, which is critical to minimize the charger size, cost, charging time, and amount and cost of electricity drawn from the utility.Theconverter power factor was also provided at full load for 120V and 240 V input. The power factor is greater than 0.99 from 50% load to full load. The proposed converter achieves a peak efficiency of 98.8% at 265 V input and 1 kW output power.

REFERENCES

[1] Y. J. Lee, A. Khaligh, and A. Emadi, "Advanced integrated bidirectional AC–DC and DC–DC converter for plug-in hybrid electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 58, no. 8, pp. 3970–3980, Oct. 2009.

[2] K. Morrow, D. Karner, and J. Francfort, "Plug-in hybrid electric vehicle charging infrastructure review," U.S. Dept. Energy—Veh. Technol. Program, Washington, DC, 2008.

[3] L. Petersen and M. Andersen, "Two-stage power factor corrected power supplies: The low component- stress approach," in *Proc. IEEE APEC*, 2002, vol. 2, pp. 1195–1201.

[4] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review o single phase improved power quality AC–DC converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003.

[5] M. O'Loughlin, "An interleaved PFC preregulator for high-power converters," in *Proc. Texas Instrum. Power Supply Design Semin.*, 2007, pp. 5-1–5-14.

[6] Y. Jang and M. M. Jovanovic, "Interleaved boost converter with intrinsic voltage-doubler characteristic for universal-line PFC front end," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1394–1401, Jul. 2007.