

A Single Dc Source Based Cascaded H-Bridge 5-Level Inverter

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Abstract— This paper presents a cascaded H-bridge multilevel inverter for Electric Vehicle (EV) and Hybrid Electric Vehicle (HEV) application. These new type of inverter are suitable for the high power application due to that the synthesized waveform with better harmonics and output waveform. In this, two H-Bridge inverter are connected in series in which the second H-bridge inverter uses capacitor and this capacitor acts as a DC sources whenever the DC supply is absent the modified PWM techniques is to be developed to reduce the switching losses and also to reduce the total number of switches. To develop the model of the multilevel inverter, a simulation is done by using the MATLAB/SIMULINK software.

Keywords— Cascaded H-Bridge multilevel inverter (CHB), Pulse Width Modulation (PWM), Hybrid Electric vehicle (HEV), Harmonics elimination.

I. INTRODUCTION

A multilevel inverter is a power electronics converter is recently applicable for high voltage and high power application such as flexible AC transmission system (FACTS) and AC motor drives [3]. Also, power electronics technologies have provided an important improvement in the renewable energy application. In recent year the multilevel inverter has gained due to some advantages in lower switching loss, high voltage capability and lower harmonics [1]-[3]. In several topologies for multilevel inverter have been proposed; the diode-clamped [4],[5], flying capacitor[6], and cascade H-Bridge[7] structures.

In the development of improved power electronics because of increasing oil prices and environmental concern, Hybrid Electric Vehicle(HEVs) and Electric Vehicles(EVs) are gained increased attention due to their higher efficiencies and lower emission[10]-[12] and motor applications. In the HEV are typically combines smaller internal combustion engines of a conventional vehicle with a battery pack and an electric motor to drive the vehicle. And the EV are typically used to recharge the

batteries and an electric motor. The batteries need to charge regularly. Both HEV and EV is need a power inverter and a traction drive motor to drive the traction motor in the requirement of the power inverter includes high peak power and low continuous power ratings. The power inverter is as currently available for HEVs use a dc-dc boost converter is to boost the battery voltage for a three phase inverter.

There are several pulse width modulation (PWM) techniques are known. Here, we concern only in HPWM topologies in this paper. The advantages of the topologies are[9]

- 1.To reduce the switching losses.
- 2.To improve the efficiency of the system.
3. To regulate the frequency and ac voltage.

Section II discussed about operation principle of the hybrid multilevel inverter, section III deals with the hybrid pulse width modulation techniques. Section IV is focused on the simulation results using MATLAB/SIMULINK. Section V deals with the conclusion.

II. OPERATION PRINCIPLE OF THE HYBRID MULTILEVEL INVERTER

The multilevel inverters have some gained much attention in the due to the medium voltage and high power application because of their some advantages, such as low harmonics, low voltage stress on power switches and EMI output. The advantages of using multilevel inverter are:[7]

1. Harmonics distortion is very low
2. Reduced switching losses.
3. Efficiency is increased
4. High voltage capability with voltage limited devices.

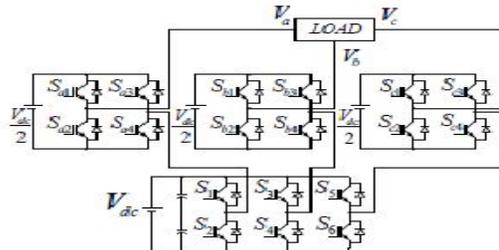


Fig.1. Five level three phase cascaded hybrid multilevel inverter.

A simplified three phase cascaded hybrid multilevel inverter are shown in Fig.1. Single phase topology of hybrid multilevel inverter is shown the Fig.2; the bottom is one leg of the standard three-leg inverter with a dc power sources (V_{dc}), and the top is a hybrid in series with each standard leg that the hybrid inverter can use a separate dc power sources($V_{dc}/2$).

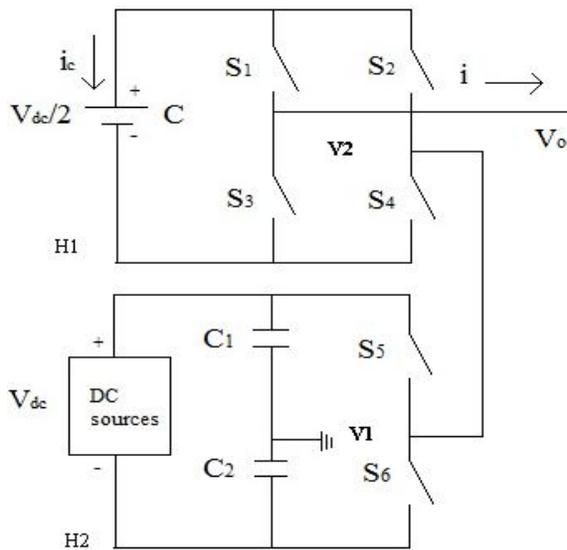


Fig.2. Single phase cascaded five level inverter

The output voltage v_1 of the bottom inverter (H2) is either $+0.5V_{dc}$ (Sa5 closed) or $-0.5V_{dc}$ (Sa6 closed). This bridge H2 is connected in series with a full H-bridge (H1) which is supplied by a capacitor. If the capacitor is kept charged to $0.5V_{dc}$, then the output voltage of the H-bridge (H1) is $+0.5V_{dc}$ (Sa1, Sa4 closed), 0 (Sa1, Sa2 closed or Sa3, Sa4 closed), or $-0.5V_{dc}$ (Sa2, Sa3 closed). When the output voltage $v = v_1 + v_2$ is required to be zero, we can either set $v_1 = +0.5V_{dc}$ and $v_2 = -0.5V_{dc}$ or $v_1 = -0.5V_{dc}$ and $v_2 = +0.5V_{dc}$.

If Sa1, Sa4 are closed ($v_2 = +0.5V_{dc}$) along with Sa6 closed ($v_1 = -0.5V_{dc}$), then the capacitor is discharging and $v = v_1 + v_2 = 0$. On the other hand, if Sa2, Sa3 are closed ($v_2 = -0.5V_{dc}$) and Sa5 is also closed ($v_1 = +0.5V_{dc}$), then the capacitor is charging and $v = v_1 + v_2 = 0$. The case $i < 0$ is accomplished by simply reversing the switch positions of the $i > 0$ case for charging and discharging of the capacitor. During the period the output voltage is zero, either the switches Sa1, Sa4 and Sa6 are closed or the switches Sa2, Sa3 and Sa5 are closed depending on the capacitor is charging and discharging.

Fig.3. shows the output waveform for the hybrid multilevel inverter. It is well known that a two level inverter, such as the one shown in Fig 3, generates an output voltage with two different values (levels), VC and “zero,” with respect to the negative terminal of the dc source (“0”), while a three-level module, Fig2.5. Generates three different voltages at the output ($2V_c$, V_c , and “zero”). The different positions of the ideal switches are implemented with a number of semiconductors that are in direct relation with the output voltage number of levels. Multilevel inverters are implemented with small dc sources to form a staircase ac waveform, which follows a given reference template. For example, having two dc sources with magnitudes equal to $2V$ each, a composed 5-level waveform can be obtained (two positive, two negatives, and zero with respect to the middle point between the five sources).

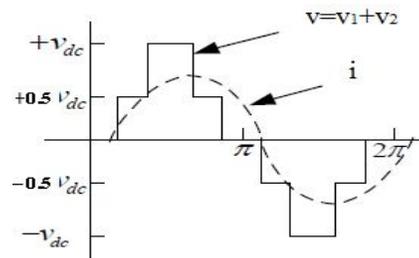


Fig.3. Output waveform of the hybrid multilevel inverter

TABLE I SWITCHING STRATEGY

Voltage	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆
-V _{dc}	0	1	1	0	0	1
-0.5V _{dc}	0	1	1	0	0	0
0	1	0	0	1	0	1
0	0	1	1	0	1	0
0.5V _{dc}	1	0	0	1	0	0
V _{dc}	1	0	0	1	1	0

In practical, if a single chip is used to generate the PWM signals, it is normally have one carrier signal with six PWM channels. The hybrid multilevel inverter requires the 12 PWM channels for both main and auxiliary inverter. Therefore, the reference signal of sinusoidal PWM used for auxiliary inverter is modified by using the equation (1)-(4) and the multiplexing signals from (3) and (4) are used to fabricate PWM signal by using the logic diagram are shown in the figure 4 and table 1.

$$f(t) = m_a \sin(\omega t) \quad \dots\dots (1)$$

$$\frac{T_p}{T_c} = \begin{cases} 2(f(t) - \frac{1}{2}); \frac{1}{2} \leq f(t) \leq 1 \\ 2(\frac{1}{2} - f(t)); 0 \leq f(t) \leq \frac{1}{2} \end{cases} \quad \dots\dots(2)$$

$$A_1 = \begin{cases} 1; f(x) \geq 0 \\ 1; f(x) < 0 \end{cases} \quad \dots\dots (3)$$

$$A_2 = \begin{cases} 1; |f(t)| \geq \frac{1}{2} \\ 1; |f(t)| < \frac{1}{2} \end{cases} \quad \dots\dots (4)$$

Where,

f(t) is a reference signal,

Ma is Modulation index,

A1 is a multiplexing index #1,

A2 is a multiplexing index #2,

Tp/Tc is a pulse width of PWM

III. HYBRID PULSE WIDTH MODULATION FOR CASCADED FIVE LEVEL INVERTER

In PWM technique pulses of unequal widths are generated. The pulse is generated by comparing a sinusoidal wave (modulating signal) of frequency 50HZ against a triangular wave (carrier signal) is shown in Fig 4. Each comparison gives one if the modulating signal is greater than the triangular carrier else zero. PWM is categorized into various types among which the technique employed in this paper is sinusoidal pulse width modulation(SPWM) because it reduces harmonic content. From the Fig 2 the main inverter refers to H2 bridge and the auxiliary inverter refers to H1 bridge. Since the low switching losses during PWM operation is required, the main inverter will operate only at square wave mode and auxiliary inverter will operate at PWM mode as depicted in Fig 5. In this topology, for generating the switching pulses multicarrier phase shifted pulse width modulation. In the multicarrier modulation, the amplitude and frequency of all triangular carriers are the same as well as the phase shifts between adjacent carriers.

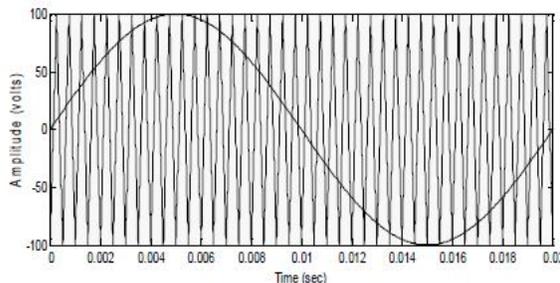


Fig.4. Generating pulse using SPWM

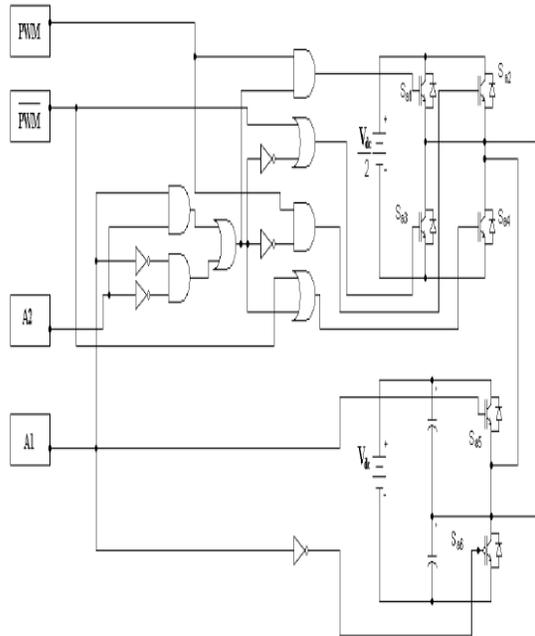


Fig.5. Logic diagram for control signal

S _n	Hybrid PWM mixing operator
S _{a1}	A1
S _{a2}	$\overline{A1}$
S _{a3}	$PWM \cdot ((A2 \cdot A1) + ((A2) \cdot (A1)))$
S _{a4}	$\overline{PWM} + ((A2 \cdot A1) + (\overline{A2} \cdot \overline{A1}))$
S _{a5}	$\overline{PWM} + ((A2 \cdot A1) + (\overline{A2} \cdot A1))$
S _{a6}	$\overline{PWM} + ((A2 \cdot A1) + (A2 \cdot \overline{A1}))$

Table.2. Generating of PWM signals for the five level inverter

IV. SIMULATION RESULTS

PSIM (Powersim) and MATLAB/Simulink are utilized to create the simulation model three phase inverter are shown in Fig. 6..MATLAB/Simulink is used to simulate the control signals and PSIM acts as a hardware prototype. This simulation model could offer the simplicity of a changing control scheme and simple to transfer the control model from simulation to implementation in a

single chip. Fundamental output voltages can be controlled by changing a modulation index *ma* of referent signal; also, the fundamental output frequency can be adjusted by changing frequency of the referent signal. The simulation results of the proposed hybrid multilevel inverter are illustrated in Fig. 6-8

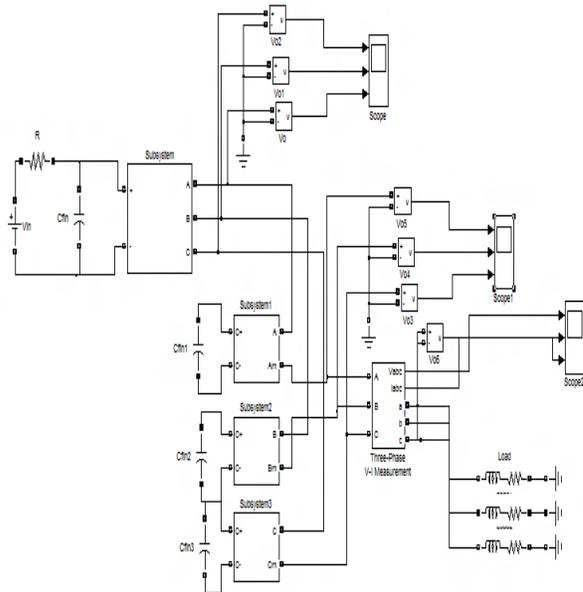


Fig.6.Simulation model of 3Φ 5-level inverter using MATLAB

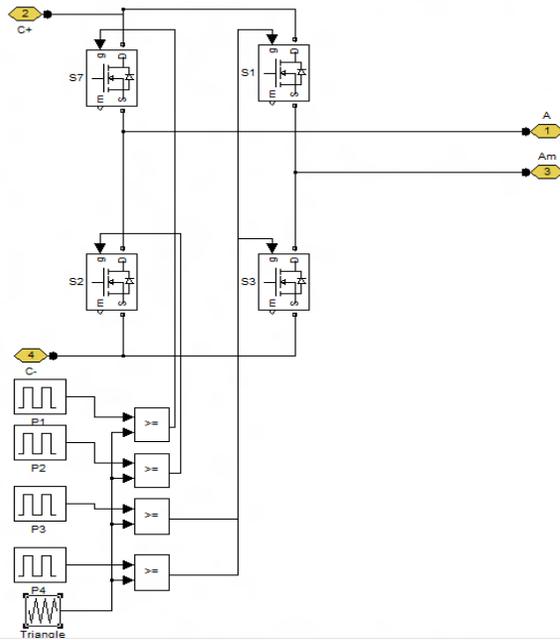


Fig.7. Simulation model for the subsystems

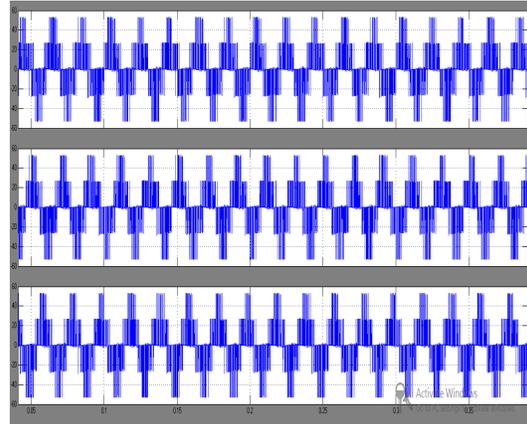


Fig.9. Three phase five level H-bridge inverter

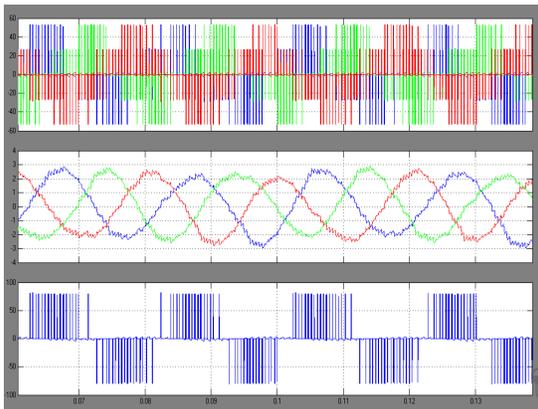


Fig.8. Line to Line output voltage and output current of the hybrid system

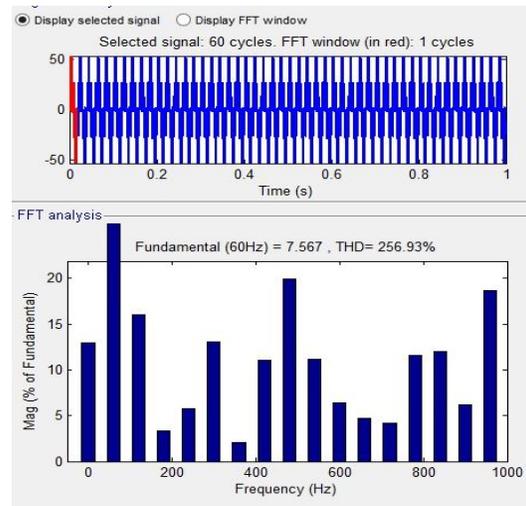


Fig.10. Displayed selected signal for five level inverter

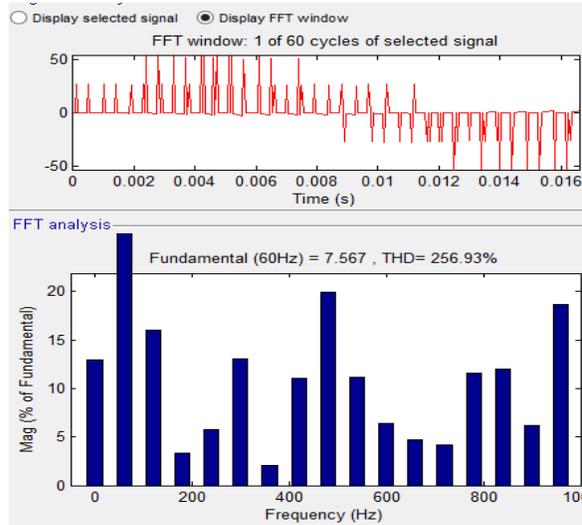


Fig.11. FFT analysis of five level inverter

V. CONCLUSION

In the Present Work , performance of cascaded five level inverter using hybrid pulse width modulation technique has been analyzed. The topology used in this technique reduces the number of power switches and switching losses. In the Cascaded H-bridge multilevel inverter is popular in the multilevel inverter family. Out of various PWM techniques level gives a good harmonic performance. The modified PWM technique has also been developed to reduce switching losses. Also, the proposed method can reduce the number of required power switches compared to the cascaded multilevel inverter. From the FFT analysis we get minimum THD of 256.93% and the fundamental frequency 7.567Hz shows performance of the cascaded hybrid five level inverter. The simulation results show that this hybrid five level inverter topology can be applied for high power applications. Thus the proposed method will reduce the cost, and also used only 6 switches, harmonic reduction and the heat losses.

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