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Analysis of Multipliers in VLSI

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Abstract: Low Power VLSI circuit have become important criterion for designing the energy efficient electronic designs for high performance and portable devices. In the majority of DSP application the critical operations are the multiplication. Multiplication is one of the basic arithmetic operations and requires substantially more hardware resources and processing time than addition and subtraction. In this paper comparative study of different multiplier is done for low power requirements and high speed.

INTRODUCTION

The multiplier plays a major role in dsp application. The present development in processor design aim at low power multiplier architecture using in their processor circuit. So the need for low power multiplier has increased, hence the designer concentrate more on low power efficient circuit design.

Generally the computational performance of dsp processor is affected by its multiplier performance. The low power and high speed vlsi can be implemented with different logic style. The three important considerations for vlsi design are power, area and delay .there are many proposed logic low power consideration and high speed and each

logic style has its own advantage in terms of speed and power.

The objective of good multiplier is to provide a physically compact, high speed and low power consumption unit. Being a core part of arithmetic processing unit multipliers are in extremely high demand on its speed and low power consumption. To reduce significant power consumption of multiplier designs it in good direction to reduce the no. of operation thereby reducing a dynamic power which is a major part of total power dissipation.

There are no. of techniques that to perform binary multiplication, low power multiplier using mac unit ,modified booth multiplier, and low power multiplier using spst are some of approaches to have hardware implementation of binary multiplier which are suitable for vlsi implementation at cmos level.

Firstly a one bit MAC unit is analysed. its delay in pipeline stages in the MAC unit is estimated based on which a control unit is designed to control the data flow between the MAC blocks for low power using a control logic that enables the pipelined stages at appropriate time. A conventional MAC unit consist of multiplier and an accumulator that contains the sum of previous consecutive products. The function of MAC unit is given by the following equation.

$$F = \sum A\ B$$

MAC is composed of an adder, multiplier and an accumulator. As speed is most important carry select and carry save adder are used [1]

In a single clock cycle the inputs for the MAC are to be fetched from memory location and fed to the multiplier block of the MAC. After performing multiplication the result is given to the adder which will accumulate the result into a, memory location [1] the design consist of one 17 bit register, one 8 bit Wallace tree multiplier,17 bit accumulator using ripple carry and two 18 bit accumulator register. here Wallace tree multiplier is used because it can increase the MAC unit design speed. Ripple carry adder (RCA) is used as an accumulator.

Wallace tree multiplier

Fig 1.shows the algorithm for 8*8 bits multiplication performed by Wallace tree multiplier. There are five stages to go through to complete the multiplication process [1].Each stage used half adder and full adder that are denoted by the red circle for the 1 bit half adder and the blue circle for the 1 bit full adder. First the rows are reduced using the half adder and full adder that are combined to build a carry save adder (CSA) until there were just two rows of partial products left, next remaining two rows are added using a fast carry propagate adder.

Carry save adder

If we add three or more operands simultaneously using two operand adders, the time consuming carry propagation must be repeated several times. If the no. of operands is k then carries have to propagate (k-i) times [1]. in the carry save addition we let the carry propagate only in last step, while in all the other steps we generate the partial sum and sequence of carries separately.

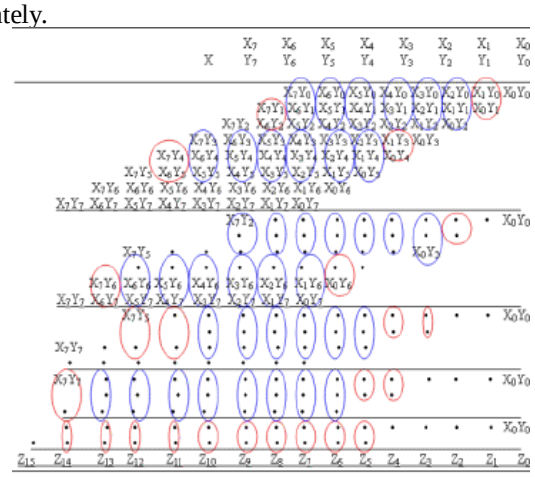


Figure 1. Algorithm for 8 bit X 8 bit Wallecetree Multiplier

A CSA is capable of reducing the no. of operands to be added from 3 to 2 without any carry propagation.

PRELIMINARIES

Block Enabling Technique

In MAC unit [2,4]data flows from the input register to the output register through multiple stages such as, adder stage and accumulator as shown in figure. Within the multiplier stages further there are multiple stages of addition. During each operation of multiplication and addition, the blocks in the pipeline may not be required to be on or enabled until the actual data gets in from the previous stage, in block enabling technique delay of each stage is checked and every block gets enabled only after the expected delay. For the entire Duration until the inputs are available ,the successive blocks are disabled thus saving power.

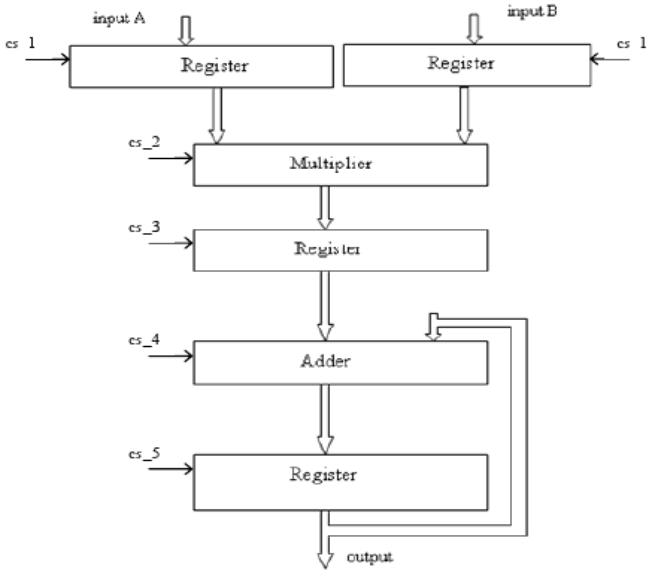
Pipelined block enable logic

Three pipelined stages of MAC with block enable logic is shown in figure.2 Here depending upon the delay of individual blocks, the control logic enables the clock ,power and logic pins of the block, thus saving power. Fig.3 shows the block schematic of the 1 bit full adder circuit with the enable. Each of the blocks in the MAC unit has an enable signal to save power. It is finding that the basic building block for any MAC unit are multiplier, adder, and register. Multiplier and adder blocks require full adder, and register require flip flop or latches. It is analysed that mux based full adder consumes very less power and also has minimum delay. In this work mux based full adder is considered

for implementation. The basic gate that is required to enable or disable the MAC is controlled using an AND gate. it is observed that delay reduces with increase in width. As the nand gate has delay, the blocks connected to the output of AND gate are disable until this time ,and these blocks are enabled only after the output are available, hence saving power.

Register in MAC unit stores data so there can be leakage current that affects power dissipation. Also the clock connected to the register cell also keeps changing and hence affects the dynamic power dissipation. The register cell is enabled with clock gating and power and delay is calculated.

Figure 2: Block diagram of MAC with block enabling technique.



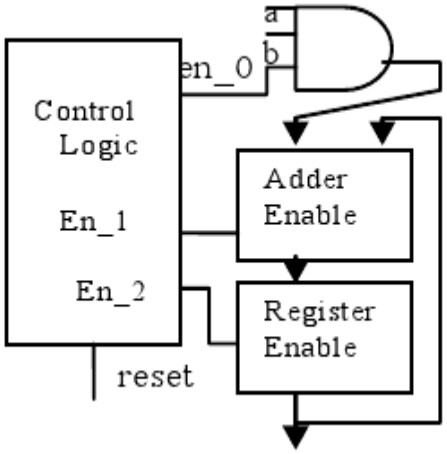


Figure:3 Control logic in MAC

BIT MAC

1 bit MAC unit is designed with clock gating and enable pin. from the result analysis carried out it is found that AND gate delay is .225ns,full adder delay is .4317ns and register delay is .6996ns. When the input is applied at 0ns,all the blocks are enabled simultaneously, the FA block would compute the result on unknown data until .225ns, and the register block would be receiving unknown data for .6567ns and hence there is wastage of power as these data s are not actual ones. Hence in this work it is incorporated a control signal that enable the blocks only after the outputs are available at their inputs. Hence we

call this technique as block enable technique. Based on the delay of each

block ,a control signal is generated to enable the blocks.

Table 3.1 and 3.2 depict the power and delay results obtained for the MAC with and without enable. From table 3.2 we find that power varies with input .MAC unit with all 0's consume less power than all 1's. The power calculation with enable is found to be more than the power without enable. If we neglect the power consumed by the control unit, then due to the enabling technique it is found that power consumption is reduced by 27% of actual power.

Spurious Power Suppression Technique

Another technique[3] we are analysing is spst. Now for the analysis we are applying an advanced version of Spurious Power Suppression Technique (SPST) on multipliers for high speed and low power purposes. When a portion of data does not affect the final computing results, the data controlling circuits of SPST latch this portion to avoid useless data transition occurring inside the arithmetic units, so that the useless spurious signals of arithmetic units are filter out. Modified Booth Algorithm is used in this project for multiplication which reduces the number of partial product to reregisters and using AND gates, to assert the data signals of multipliers after data transition. The simulation result shows that the SPST implementation with AND gates owns an extremely high flexibility on adjusting the data asserting time which not only facilitates the robustness of SPST but also leads to a significant speed improvement and power reduction. Readers also consult[5,6],

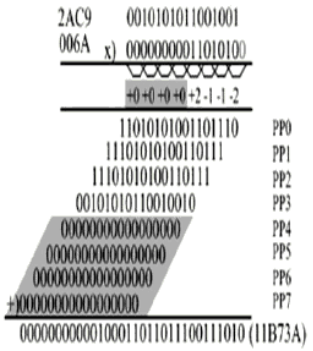


Figure 4 multiplier using modified booth encoding,where PP0 to PP7 denote the partial products.

Applying the SPST on the Modified Booth Encoder

In fig 4 shows a computing example of booth multiplying[5] two numbers 2AC9 and 006A where the shadow denotes that the numbers in this part of booth multiplication are all zero so that this part of the computations can be neglected. Saving those computations can significantly reduce the power consumption caused by the transient signals. According to the analysis of the multiplication shown in fig. the spst equipped modified Booth encoder is controlled by a detection unit. The detection unit has one of the two operands as its input to decide whether the Booth encoder calculates redundant computations.

B Applying the SPST on the Compression Tree

The spst equipped multiplier is shown in fig 5 .The PP generator generates five candidates of the partial products,i.e. {-2A,-A,0,A,2A}, which are then selected according to Booth encoding result of the operand. Moreover when the operand besides the Booth encoded one has a small absolute value, there are opportunities to reduce the spurious power dissipated in the compression tree. According to the redundancy analysis of the analysis of the additions, some of the adder in compression tree of the multiplier are replaced by the spst equipped adders, which are marked with oblique lines in fig 6,. The bit width of the MSP and LSP of each SPST equipped adder are also indicated in fraction values nearing the corresponding adder in fig 6 below-

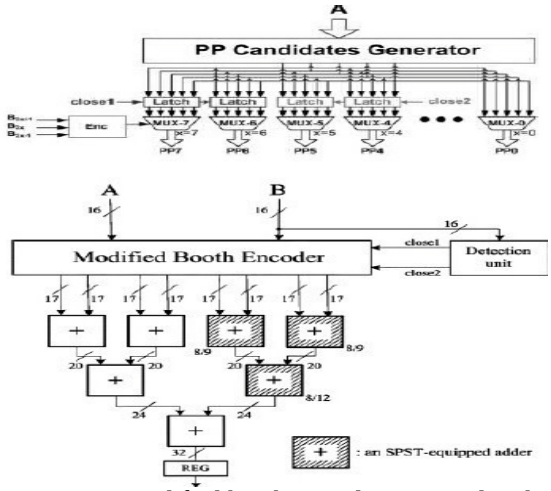


Figure 5: Modified booth Encoder equipped with SPST

COMPARISON , RESULTS AND DISCUSSION

Table 3: 1 bit MAC Power Calculations with varying inputs

	Power (W)		Power (W)	
	i/p=all 0s		i/p=all 1s	
Wn/ Wp	With Enable	With out Enable	With Enable	With out Enable
0.2	7.718 E-09	4.47 E -10	7.795 E -09	2.571 E -08
0.3	7.186 E-09	4.562 E -10	7.335 E -09	1.241 E -04
0.4	5.873 E-09	6.027 E -10	6.006 E -09	8.979 E -10
0.5	7.717 E-09	4.576 E -10	7.812 E -09	6.812 E -05

Table 3:2 bit MAC Power and delay with Pulse inputs

	Power (W)		Delay td (sec)	
	i/p a= Pulse		i/p a = Pulse	
Wn/ Wp	With Enable	With out Enable	With Enable	With out Enable
0.2	2.803 E -5	4.786 E -10	2.922 E -8	2.928 E -9
0.3	5.263 E -6	5.061 E -10	2.882 E -8	3.235 E -9
0.4	2.397 E-6	6.488 E -10	2.868 E -8	3.446 E -9
0.5	4.445 E-6	4.862 E -10	2.863 E -8	3.492 E -9

Table 3.3: Delay power and speed

Blocks	Power -watt	Delay -s	Speed Hz
1 bit register cell	0.2804n	0.0405n	24.69G
1 bit full adder	0.145n	0.0012n	833.33G
2X1 mux	0.00434n	0.00458n	218.34G
18 bit accumulator register	0.987n	0.0724n	13.81G
8X8 Wallace tree multiplier	0.332u	0.1152n	8.68G
MAC unit	0.007698m	0.437n	2.288G

Table 3.4: Simulation Results of Three Multiplier.

Design	Power/MHz (p.mw)	norm.P	Area (Tr.)	Max. freq.
SPST using Reg	0.0118	0.59	10544	142MHz
SPST using AND gate	0.0121	0.6	11028	200MHz
Tree MUL	0.0201	1	105444	200MHz

Table 3.5: Comparison of Multiplier

Parameter	MAC unit with Block enabling technique	Multiplier using SPST
Delay	0.437ns	5ns
Speed	2.288GHz	-
Power consumption	0.007698mw	0.0121mw

As shown in table 3.3, if we take the product of power and delay we find that MAC unit has almost negligible power delay product value, it indeed has a better performance in terms of the speed and power dissipation. It is analysed that total power consumption using TSMC 0.18 um is about .007698 mW for the MAC unit with enable. The delay for the MAC unit is 0.437 ns . The design speed is calculated from reciprocal of the delay which means 1/Delay time is equal to sped. Total speed for MAC unit using TSMC 0.18um is 2.288GHz.(3). In spst technique the spst has been applied on both the modified booth decoder and the compression tree of multipliers to enlarge the power reduction The simulation results of the original tree multiplier and the two spst–equipped multipliers with different implementing approaches is shown in table 3.4..[3] .In table 3.5 comparison of multipliers is given taking various parameters The power reduction is 40% also leads to 40% speed improvement when compared with former spst. This SPST dissipates only 0.0121 mW per MHz.

CONCLUSION

In this analysis is done on an 8*8 multiplier – accumulator (MAC) and is concluded that as compared to other full adder circuits, the MUX based full adder has the highest operational speed and less transistor count. Here power and delay calculated for the blocks.1 bit MAC unit is designed with enable to reduce the total power consumption based on block enable technique. The analysis also shows that the spst approach not only owns equivalent low power performance but also leads to a higher maximum speed .moreover the spst equipped multiplier also has better power efficiency when compared with the existing other multiplier.

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SHORT BIODATA OF ALL THE AUTHOR

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