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Design and Implemenation of High Speed 64-Bit Multiply and Accumulator Unit Using FPGA

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ABSTRACT: In this paper Design of high speed MAC unit based on Vedic multiplier algorithm. Generally MAC useful application such as Digital signal processing like FFT transform , Convolution and correlation. MAC is hardware based module therefore first design of multiplier block and second one is adder block. in this paper to implementation 64bit MAC with reduce the delay and increase the speed of system. The coding done by verilog-HDL and its synthesis and simulation on XILINX ISE.14.5 tool.

KEYWORDS: Vedic multiplier, adder, MAC

I. INTRODUCTION

Multiply accumulator consists of three main blocks, first one is multiplier, second one is adder and third one is accumulator. Multiplier is main important block of MAC unit. It is used in arithmetic operation for multiplication. Multiplier main key role in DSP application. More number of bits size of multiplication it is very difficult to multiplication and more delay therefore the speed is decreases. To improve the performance of high speed MAC unit but to reduce delay. Different method for design MAC unit with help of various multiplication techniques such as booth multiplier ,Wallace multiplier and vedic multiplier. The main key to the proposed MAC unit is to enhance the performance of MAC using Vedic Multiplier and to compare the array, Booth and Wallace tree multiplier in terms of computation required to generate the partial products and add the generated partial products to get the final result of the multiplication.

II. LITERATURE REVIEW

The proposed algorithm is design of Multiplier using vedic multiplier method and its application of Digital Signal processing.[1] NxN multiplier design using four N/2 bit multiplier, two N-bit full adder ,one half adder and N/2 bit full adder to add the sum and carry of half adder.[2] 16×16 array of array Multiplier using vedic multiplier this structure is hierarchical design algorithm is urdhva triyagbhyam sutra on vedic mathematics.[4] The delay of proposed MAC unit is 43.899 ns and Conventional MAC is 55.662 ns. The conventional and proposed MAC unit is coded on verilog-HDL and XILINX ISE simulator.[5] The simulation on Spartan-3e family using XILINX ISE tool and coding on verilog. The result of delay is proposed multiplier is 41.562 ns and binary multiplier is 94.087.[6]

III. ARCHITECTURE OF MAC UNIT

The shown fig. 1 is a block diagram of MAC unit. The function of the MAC unit is given by the following equation $F = \Sigma Ai \times Bi$. The inputs for the MAC are fetched from memory location and fed to multiplier block of the MAC unit, which will perform the operation of multiplication and give the result to adder block which will accumulate the result and then will store the result into a memory location. That whole process is to be achieved in a single clock cycle. Multiplication is an important function in arithmetic operation. Multiplication based operation such as multiply and accumulate unit (MAC) and Arithmetic and logic unit (ALU).

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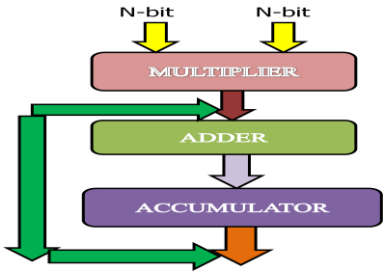

Figure:1 Architecture of MAC unit[1]

IV. OBJECTIVE

Main objective of design high performance MAC unit design based on vedic multiplier method using adder and to improve the speed of system with reduce delay. the vedic multiplier based sutra is Urdhva Tiryakbhyam (Vertical and Crosswise) multiplication. this method different of other multipliers. in this paper design of first 2,4,8,16,32-bit vedic multipliers with simple adder, also design 32bit and 64 bit MAC unit and to note down reading of speed and delay. This design of Vedic multiplier comparison of other multiplier.

V. VEDIC MATHEMATICS

Vedic mathematics is the name given to the ancient system of mathematics which was rediscovered from the vedas. It gives explanation of several mathematical terms including arithmetic, geometry, trigonometry and even calculus. it was constructed by Shri Bharati krsna theertaji (1884-1960), after his eight years of research on Vedas. He constructed 16 main sutras and 16 sub sutras. One method of multiplication is Urdhva Tiryakbhyam (Vertical and Crosswise) .The multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical and Crosswise) of ancient Indian Vedic mathematics. Urdhva Tiryakbhyam sutra is general multiplication formula applicable to all case of multiplication.

A. vedic Multiplier

The main purpose of Vedic Mathematics is to be able to solve complex calculations by simple techniques. The formula being very short makes them practically simple in implementation. Urdhva-tiryagbhyam (Vertically and crosswise) sutra is general formula applicable to multiplication operation**.** The strategy applied for developing a 64 x 64-bit Vedic multiplier is to design a 2 x 2- bit Vedic multiplier as a basic building module for the system. In the next stage of development a 4 x 4-bit multiplier is designed using 2 x 2-bit Vedic multiplier. Further in same manner 8 x 8, 16 x 16 and32 x 32- bit Vedic multiplier is designed. For the partial product addition for all stages of development a fast adders is used .Multiplier plays a very important role in today's digital circuits. The multiplier is based on an algorithm Urdhva Tiryagbhyam (Vertical and crosswise).This sutras shows how to handle multiplication of larger number (N X N bits) by breaking it into smaller sizes.

Advantages and Disadvantages

Advantages :

- Vedic multiplier is faster than the other multipliers.
- The area needed for vedic multiplier is very small as compared to other multiplier architecture.
- MAC is used in modern digital signal processing. MAC always lie in the critical path that determines the speed of the overall hardware systems.
- It is use in binary and decimal number multiplication and also use unsigned and signed number multiplication.

Disadvantages : For complex multiplications, even the system becomes complex.

B. **Architecture of Vedic multiplier:** This fig.2 is the basic block diagram of Vedic multiplier. vedic multiplier is vertical and crosswise multiplication and generated partial products therefore we need adder block than after Final output of multiplication.

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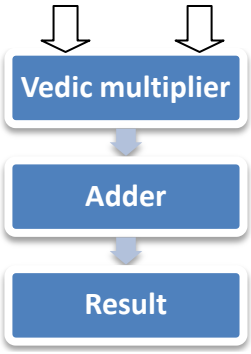

Figure:2 basic block diagram of Vedic multiplier

VI. DESIGN OF VEDIC MULTIPLIER

The first step in multiplication is vertical multiplication of LSB of both multiplicands, and then second step is crosswise multiplication and additions of the partial products. Third step involves vertical multiplication of MSB of the multiplicand and addition with the carry propagated from step 2.

C. **Design of 4x4 Bit Multiplier :** The 4X4 Multiplier is made by using four 2X2 multiplier blocks. The multiplicands are of bit size n=4 where as the result is of 8 bit size. The input is broken into smaller chunks of size n/2= 2, for both inputs, that is a and b. These newly formed chunks of 2 bits are given to 2X2 multiplier block to get the 4 bit result. The same method is followed for the multipliers of higher bits like 8,16 and 32 bits. here the shown this fig.3 is the 4×4 block diagram of vedic multiplier.

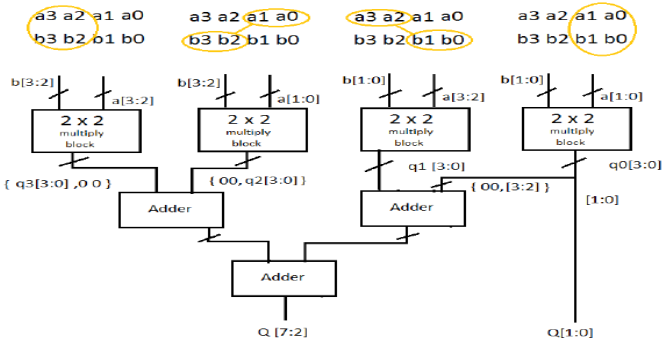

Figure:3 Block Diagram of 4x4 bit multiplier[2]

Example of 4x4 Vedic Multiplier : This fig.4 is multiplication of 4x4 bit vedic multiplier. This two 4-bit input multiplier first 2bit input multiplication by vertical and crosswise we start with LSB to MSB input multiplication and then addition of multiplication and to generated carry in previous one addition we added with next addition.

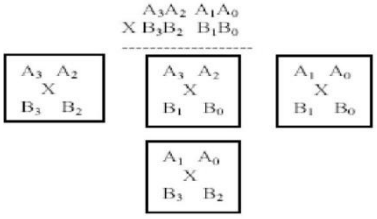

Figure:4. Multiplication of 4x4 bit vedic multiplier[3]

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The equation of 4×4 vedic multiplier are[4]
X= a3 a2 a1 a0…….. (1)
Y= b3 b2 b1 b0…….. (2)
P0= a0.b0…… (3)
P1= a1.b0+a0.b1…….. (4)
P2= a2.b0+a1.b1+a0.b2+P1(1)…… (5)
P3=a3.b0+a2.b1+a1.b2+a0b3+p2(2 to1)…… (6)
P4= a3b1+a2b2+a1b3+p3(2 to 1)…… (7)
P5=a3b2+a2b3+p4(2 to 1)……(8)
P6= a3b3+p5(2 to 1)……..(9)
Product= p6&p5(0) & p4(0) & p(3) &p(2) &P(1) &p(0) & concatenate

Here this fig.5 representation of basic steps of line diagram of multiplication of two 4x4 bit numbers Basic formula is vertical and crosswise multiplication through LSB to MSB multiplication. This steps use for decimal and binary data multiplication. Vedic multiplier use for unsigned and signed numbers.

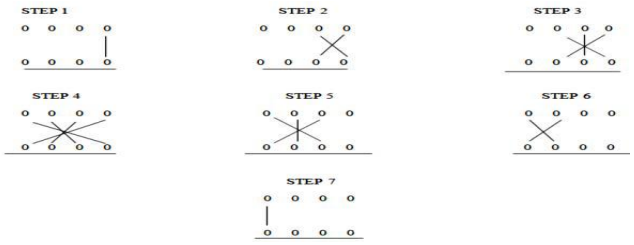

Figure:5 line Diagram for multiplication of two 4x4 bit number[5]

D.Design of 16x16 Bit Multiplier : This fig.6 to representation of block diagram of 16x16bit vedic multiplier using adder. Here two input given to 16-bit and we get the 32bit output data. first multiplication of 8bit two input data with help of vedic techniques and second addition of number of partial products. this method is very simple for increase numbers of bit size of multiplication.

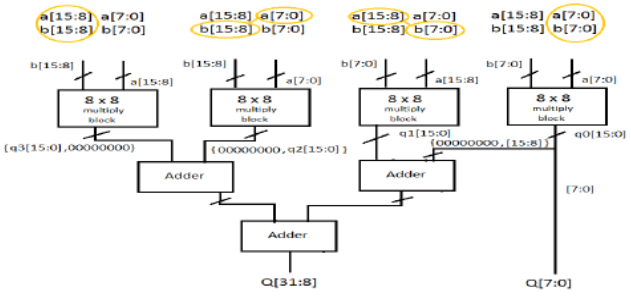

Figure:6 Block Diagram of 16x16 bit vedic multiplier[4]

E. Design of 32x32 Bit Multiplier: The 32x32bit Vedic multiplier module as shown in the block diagram in Fig.7 it is easily implemented by using four 4x4 bit Vedic multiplier modules as discussed in the previous section. It is analyze four block of 16x16bit multiplications, say a= a15 a14 a13 a12 a11 a10 a9 a8 a7 a6 a5 a4 a3 a2 a1 a0 and b= b15 b14 b13 b12 b11 b10 b9 b8 b7 b6 b5b4 b3 b2 b1b0.So total two 32 bit input give to 16x16bit multiplications. The output line for the multiplication result will be of 64 bits as –S63 to S0.

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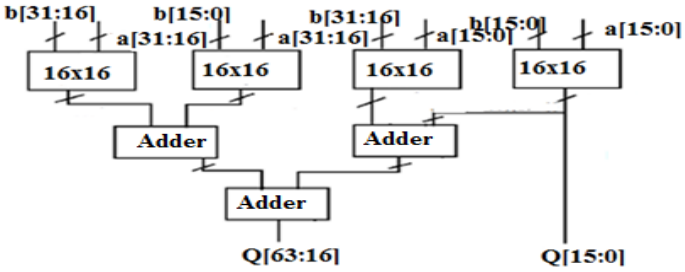

Figure:7 Block Diagram of 32x32 bit vedic multiplier[6]

F.Design of 64x64 Bit Multiplier: Number of bit width increase to increase partial products therefore its difficulty work of multiplication. here block diagram of 64x64 bit multiplier shown in fig.8 the design of 64bit vedic multiplier, first design 4 block 32x32bit data inputs and we get the 128 bit output data, second design of adder because to reduce the partial products of multiplication.

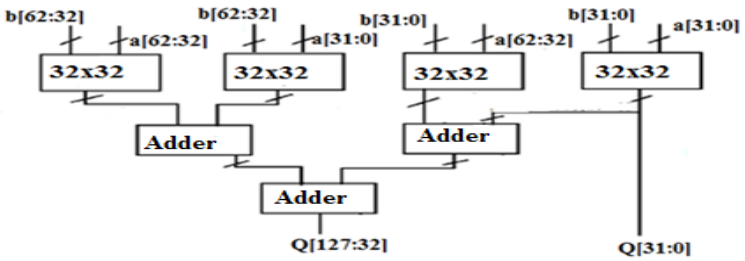

Figure:8 Block Diagram of 64x64 bit vedic multiplier[7]

G.Design of 64x64 Bit Multiplier with CLA adder: Here this fig.9 representation of 64-bit MAC unit with Carry look ahead adder. This adder is better for simple adder like half adder, full adder and ripple carry adder. main important work of adder to reduce partial product of multiplication. this process is similarly with above fig.8 but different for only adder.

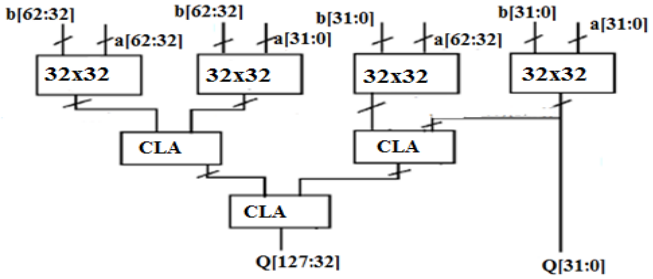

Figure:9 Block Diagram of 64x64 bit vedic multiplier with CLA adder[7]

VII. CARRY LOOK AHEAD ADDER

A Carry-Look ahead Adder is a type of adder used in digital Logic circuit. A Carry-Look ahead adder improves speed by reducing the amount of time required to determine Carry bits.

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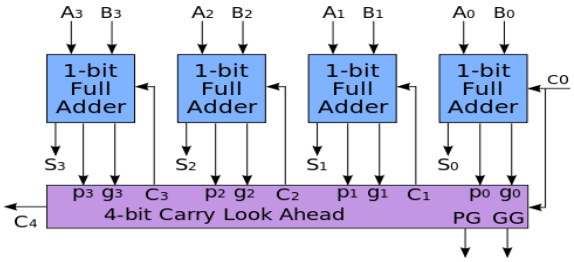

Figure:10 4-bit carry look ahead adder[8]

Carry look ahead logic uses the concepts of generating and Propagating Carries. Carry generation occurs when Ai=Bi, so when Ai=Bi=1, carry of 1 is produced and when Ai=Bi=0 ,a carry of 0 gets generated. On the other hand, carry propagation occurs when Ai not equal to Bi. The shown this fig.10 of 4-bit carry look ahead adder.

Boolean equation:[1]

Si = Pi XOR Ci …….. (1)

Ci+1 = Gi + Pi.Ci ……... (2)

Gi= Ai.Bi ……..(3)

Pi= Ai XOR Bi……..(4)

The equation of Gi and Pi representation of carry generated and propagated. Si and Ci+1 representation of sum and carry out. PG and GG representation of group of propagation and generation.

VIII. SIMULATION RESULT

The design is developed using verilog-HDL and Synthesized in XILINX-ISE-14.5 tool. Here simulation wave result of 64 bit MAC unit with CLA adder and with Simple adder. Another result of comparison of delay in 32-bit MAC unit CLA and without CLA. therefore the vedic multiplier is better performance compared with other multiplier. Simulation result shown in fig.11 ,12,13 and delay and speed comparison result shown in table.1,2,3,4.

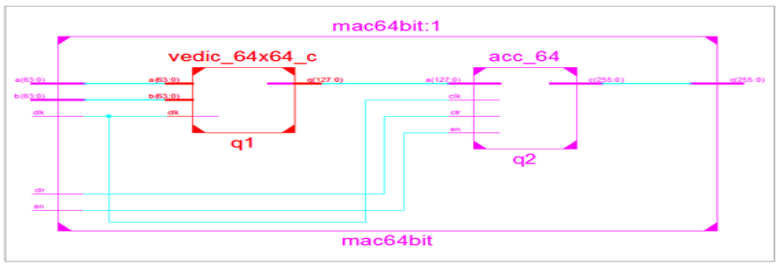

Figure:11 64bit MAC unit RTL Synthesis

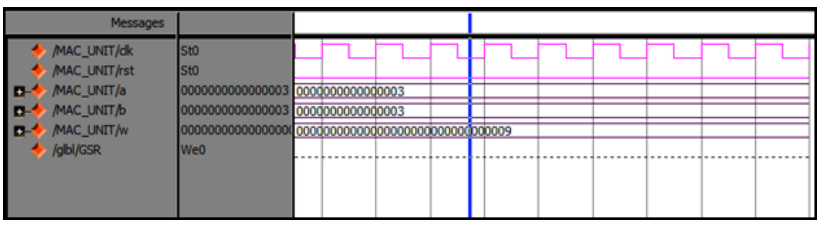

Figure:12 64bit MAC unit with CLA adder

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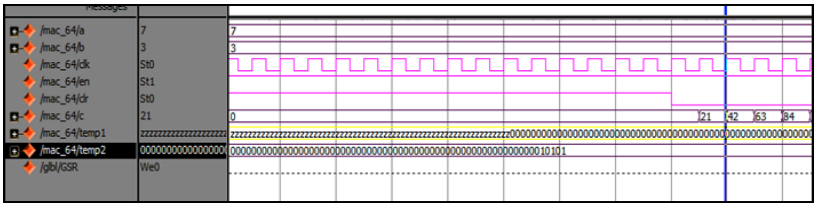

Figure:13 Simulation result of 64bitMAC unit

Table:1 Result for 32bit MAC and 64bit MAC unit

Sparatan-3 XC3S400,-5PQ208	**32-bit MAC**	**64-bit MAC**
Delay(ns)	10.471	17.639
Speed(Mhz)	95.50	56.69

Table:2 Result for 32bit MAC unit

Spartan-3E, XC3S500e, -5FG320	**32-bit MAC without CLA**	**32-bit MAC with CLA**
Delay(ns)	9.495	7.580
Speed(Mhz)	105.319	131.934

Table:3 Comparison of delay of 8×8 and 16×16 bit Multipliers

Spartan-3Family, XC3S400,-5 PQ 208	**Modified Booth Wallace multiplier[1]**		**Vedic multiplier**	
Bit size	8×8	16×16	8×8	16×16
Delay (ns)	25.756	59.238	24.065	31.738

Table:4 Comparison of 32-bit MAC unit

Spartan-6 Family	**32-bit MAC unit**	**32-bit Conventional MAC unit [7]**
Delay (ns)	4.182	43.899
Speed(MHz)	239.128	22.77

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IX. CONCLUSION

The Design of high speed 64 bit Multiplier and accumulator unit (MAC) is implementation in this research paper. The comparison of delay of vedic multiplier with other multiplier and also comparison result of 32bit MAC with other Conventional MAC unit. Therefore vedic multiplier is high performance compared to other multiplier. The design of 64bit MAC unit in FPGA used is XILINX spartan-3Family,device- XC3S400,speed-5and package PQ 208 and the design done by verilog-HDL used XILINX ISE simulator.

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