ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 1, January 2015

Design and Implementation of Super Class Integrated Qubit Fredkin Gate For Quantum Reversible Circuits

B.Pradeep, V.Vishnu Vardhan

M.Tech Student, Department of ECE, QIS College of Engineering and Technology, Ongole, India

Assistant professor, Department of ECE, QIS College of Engineering and Technology, Ongole, India

ABSTRACT: Reversible Logic is an emerging technology; it has hellocious applications in various fields. Reversible logic implementation reduces loss of entropy because of bit manipulations. Conservative reversible logic gate obeys reversible logic rules and also satisfies the property that there is equal number of 1s in the outputs as in the inputs. In this work, modified design of SCRL (Super Conservative Reversible Logic) gate for the design of reversible quantum circuit is presented. The proposed SCRL Integrated Qubit gate has 1 control input which swaps n-1 depending on control input. Barrel shifter forms an integral component of many computing systems. As an example of using the proposed SCRL gate to design efficient reversible quantum circuits, the design of reversible barrel shifter with *zero ancilla inputs and zero garbage outputs* is illustrated.

I. INTRODUCTION

Reversible Logic is an emerging technology; it has hellocious applications in various fields, such as Nano computing, DNA Computing QCA (Quantum Cellular Automata),Optical Computing etc.., Limitations of CMOS in Deep sub Micron Regime Leads to failure of Moore's law, leads to development of Reversible circuits. These are more immune to Information loss, this Information loss is in the form of energy dissipated for every bit change. Reversibility concept is an idea from Launder[2] , there is a minimum amount of energy required to change one bit of information, known as the Landauer's limit kT ln2 (0.69315).At25 °C, energy loss for one bit change is 0.0178 ev.Bennett [3]showed that loss is negligible if we implement reversible logic. So the primary goal of reversible computing is to minimize energy loss in computing devices and promote speed and density. We present VHDL representation for proposed design .In section II we represents Basic terminology of reversible logic and basic gates in Reversible logic .In section III we represent Proposed Work using Prior Work ,In section V conclusion .

II. TERMINOLOGY AND GATES

The multiple output Boolean function G(x1; x2;:::; xn) of n Boolean variables is called reversible if the number of inputs is equal to the number of outputs ,any output pattern has an only one input representation.

Basic Gates in reversible logic

The reversible gates used in this work are the NOT gate, the CNOT gate, the Toffoli gate and the Peres gate. Each reversible gate has the quantum cost and the delay associated with it. The NOT gate and the CNOT gate have the quantum cost of 1 and delay of 1 Δ; Control V control V + are the basic gates ,by using these gates many gates using reversible logic were designed to meet the requirement ,

A)FEYMAN GATE:.

This gate uses one CNOT Gate with quantum cost 1, Details of CNOT gate and Quantum Representation in fig 2

B)Control V and Control V+:

The controlled-V gate is shown in Fig. 3 In thecontrolled-V gate, when the control input l A=0 then thequbit B will pass through the controlled part unchanged, i.e., Q=B. When A=1 then the unitary operation V =is applied to the input B, i.e., Q=V(B).

Thecontrolled-V + gate is shown in Fig4. In the controlled-V + gate when the control input

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 1, January 2015

l A =0 then the qubit B willpass through the controlled part unchanged, i.e., we will haveQ=B. When A=1 then the unitary operation $V^{+} = V^{-1}$ isapplied to the input B, i.e., Q=V +(B).

C)Integrates Qubit Gates:
These are two bit quantum gates allows minimized construction of locally reversible logic structures.[2].

D)Fredkin Gate using IQ Gates[FG]:
By using IQ Representation for Fredkin Gate Reduces quantum cost to 5.Quantum Representation of Fredkin gate is in Fig7

E)Swap Gate:
Reduced implementation of the reversible Swap Gate[2], which is designed using two integrated qubit gates, and produces a swap of the two input values on the output gate. Previously, the swap gate was implemented using three Feynman gates which produced the outputs (P=A⊕(A⊕B) and Q=A⊕(A⊕B)⊕(A⊕B)which produces the swap, and incurred a quantum cost and delay of 3.The proposed implementation is accomplished with a quantum cost and delay of 2, was verified using VHDL, and is shown in Figure 5 and 6.

Fig :1 Quantum Representation of QNOT.

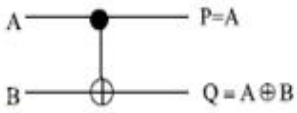

Fig:2 Quantum Representation of FEYMAN

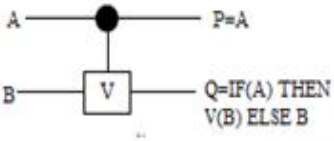

Fig:3 Quantum Representation of Control v

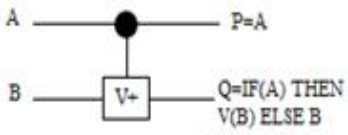

Fig:4 Quantum representation of control V+

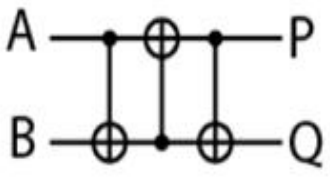

Fig: 5Quantum Representation of Swap Gate.

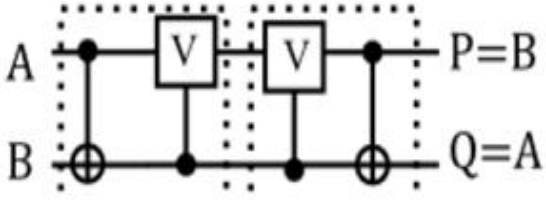

Fig:6 Quantum representation of Swap gate using INTEGRATED QUBIT GATES

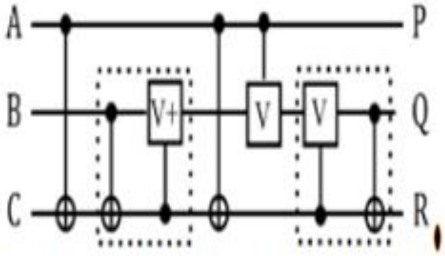

Fig:7 Quantum representation of Integrated Qubit Fredkin Gate

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 1, January 2015

III. LITERATURE SURVEY

In this work, we have proposed a new n × n (n inputs and noutputs) conservative reversible logic gate named SCRL gate. In theSCRL gate, out of n inputs there is 1 control input and n −1 datainputs. Let us define n inputs of the SCRL gate as c_0; a_0; a_1:::$a_{n-2}$where c_0 is the control input and a_0 to a_{n-2} are the data inputs. Theoutput function of the SCRL gate is defined as follows:

- The control input c0 is hardwired to the first output of the SCRLgate.
- The remaining n − 1 outputs have the output function c0ai +c0ak, where a^i is the i^{th} input and i ∈ {0 to n −2}; and a_k is the k^{th} input where k ∈ {0 to n − 2} such that k = i and a_k cannot occur as the coefficient of c_0 in any other output function.

Two examples of n × n SCRL gate are shown in Figure 8. FromFigures 8(a) and8(b) it can be observed that there can be more than one n × n SCRL gates depending on the selection of the coefficient
of c0 in the output function: c0ai + c0ak.

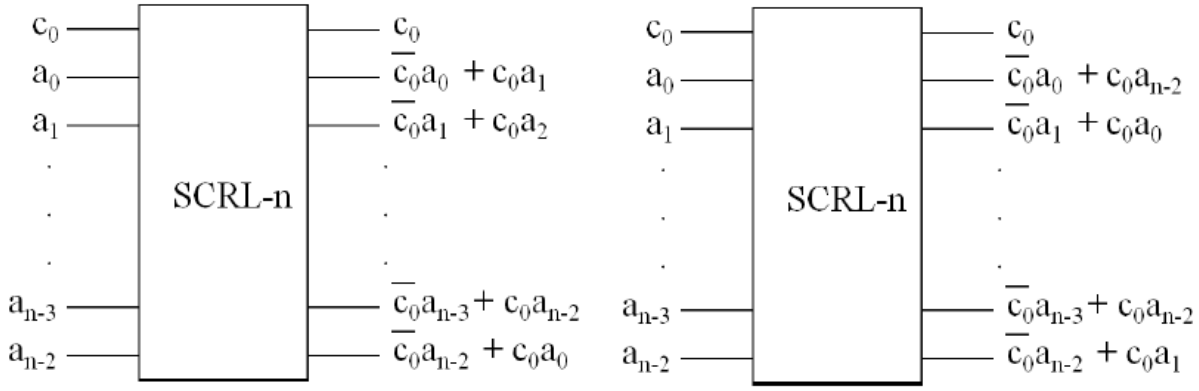

Fig:8 SCRL –n type gate representation

A)SCRL gate as a Super Set of Fredkin gate[1]:

A 3x3 SCRL gate (SCRL-3) is similar to the existing Fredkin gate. Theexisting Fredkin gate is very limited in functionality as compared to the proposed generalized SCRL gate as illustrated below

- The existing Fredkin gate is not suitable for designing SCRL gates with even inputs, It can be observed that SCRL-4 gatecannot be designed from the existing Fredkin gate.
- The odd inputs SCRL gates such as SCRL-5, SCRL-7, etc. can be defined as SCRL-(2n+1) where n is an integer such that n≥1. By cascading the Fredkin gates in series, we can design odd inputs/outputs equivalent of SCRL gates.

The Fredkin gate based logical block can do the pair wise bit swap but it is not capable of performing the swap of any two input bits. Our proposed SCRL gate has overcome this limitation as it is more generic in nature and can swap any two input bits when control input is 1.

IV. PROPOSED SCRL INTGRATED QUBIT GATE

In SCRL we can do pair wise swapping of bits but also it can swap two or more bits depending on control inputs like SCRL gate [1], InSCRL [1] uses swap gate as shown in Fig 5 with qubit gate its quantum cost is ‘3’ unit .Proposed INTEGRATED QUBIT based SCRL uses swap with which uses integrated qubit gates as shown in fig 6 .The cost reduces from ‘3’ to ‘2’ for 1 swap gate.

A)PROPOSED DESIGN OF A REVERSIBLE BARREL SHIFTERUSING SCRL GATE

For a (n,k) reversible barrel shifter the input data is represented as in-1; in-2; in-3; :::::; i2; i1; i0. The (n,k) reversible barrel shifter has log2(n) stages. The log2(n) number of stages of a(n,k) reversible logical right shifter is controlled by control signalsS_{k-1},S_{k-2},....,S_1,S_0. The S_0will work as the control signal for 1ststage, S1 will work as the control signal for

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 1, January 2015

2nd stage and so on. Thus for mth stage the control signal will be S_{m-1} where m= 1 tok-1. We can observe that each stage of the (n,k) barrel shifter can beimplemented using SCRL-(n+1) gate. It is to be noted that for the(i+1)th stage of (n,k) reversible barrel shifter where i=0 to k-1, $S_i$will be the control signal of the SCRL-(n+1) gate.The proposed design of (n,k) reversible barrel shifter using SCRL with integrated qubit gates is illustrated with an example of (4,2) reversible barrel shifter.Figure 9 shows the equations of (4,2) reversible barrel shifter generatedusing SCRL gates, the stage 1 of the reversible barrel shiftergenerates the intermediate outputs K0 to K3. In stage 2 the finaloutputs are generated as O0 to O3. Thus, the proposed SCRL-5 gate implements the stage 1 with Zero ancilla inputs and zero garbage outputs. The Stage 2 of (4,2)reversible barrel shifter generates the final outputs O0 to O3 as shownin Table1 that can be mapped to another SCRL-5 gate as illustrated in Figure 9(b).

Table 1: Representation ofequation of Shifter Stage

$K3=i_3+S_0\ i_0 O3=K_3+S_1K_1 K2=i_2+S_0\ i_3\ O2=K_2+S_1\ K_0$
$K1=i_1+S_0i_2\ O1=K_1+S_1K_2$
$K0=i_0+S_0\ i_1\ O0=K_0+S1K_3$

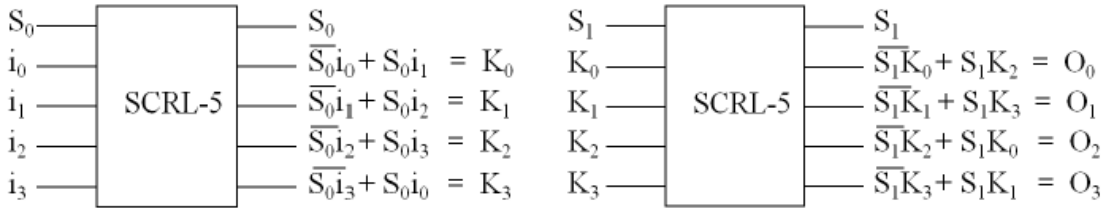

Fig:9(a) Mapping of Stage Fig:9(b) Stage 2 of reversible barrel shifter onproposed SCRL-5 gate

The complete design of the proposed (4,2) reversiblebarrel shifter cascading Stage 1 and Stage 2 with two SCRL gates isshown in Figure 10(a). Thus, using the proposed design methodologyof (4,2) reversible barrel shifter, the (n,k) reversible barrel shiftercan be designed using SCRL gates as illustrated in Figure 10(b)where each stage is implemented with proposed SCRL-(n+1) gate.

The proposed (n,k) reversible barrel shifter based on SCRL gates canbe summarized as :
Cost reduced by 1 unit for 1 swap gate
Number of SCRL Gates (NSCRL) = k
Number of Garbage Outputs (NGO) = 0
Number of Ancilla Inputs (NAI) = 0

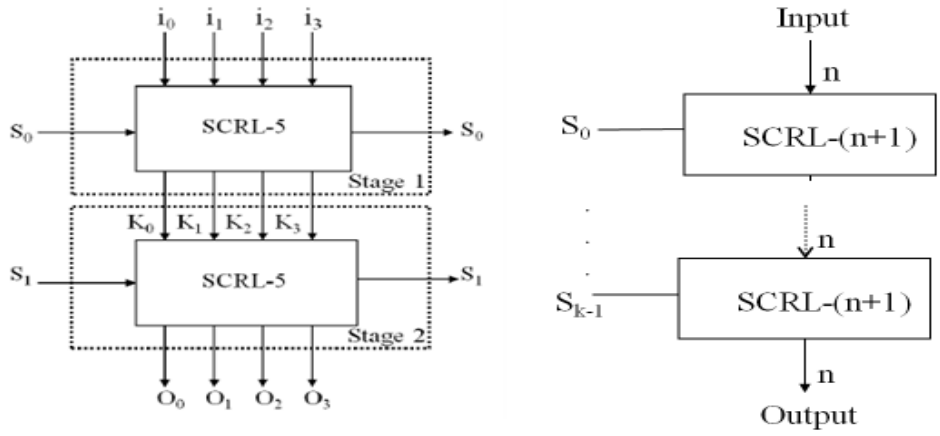

Fig: 10(a)**Proposed design of reversible (4,2) barrel shifter and(b)reversible (n,k)barrel shifter based on SCRL gate**

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 1, January 2015

B)Simulation Result for (4,2) Barrel Shifter:

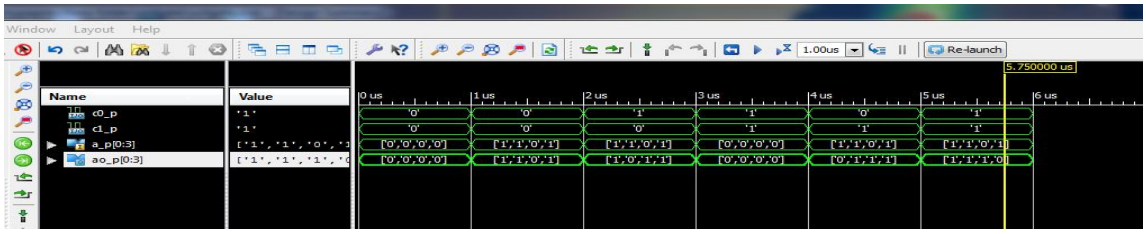

Fig:11Simulation result of (4,2) Reversible Barrel shifter using integrated qubit based SCRL

V. DISCUSSIONS AND CONCLUSIONS

We present a novel conservative reversible logic gate (SCRL gate)which is superior, and is a superclass of Fredkin gate. Further, the design of (4,2) reversible barrel shifter with zero ancilla inputs andzero garbage outputs is presented based on the proposed SCRL gate.We conclude that the use of the specific reversible gate for a particularcombinational function can be very much beneficial in minimizing thenumber of ancilla inputs and garbage outputs in reversible quantumcircuits. All the proposed reversible designs are functionally verified at the logical level by using the VHDL and the HDL simulators. In future work, we would like to illustrate the various other applications of the proposed SCRL gate in the design of reversible quantum circuits.

REFERENCES

[1]H.Thapliyal, A.Bhatt and N. Ranganathan, "A New CRL Gate as Super Class of Fredkin Gate to Design Reversible Quantum Circuits ", *Proceedings of the 56th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Columbus, Aug 2013, pp. 1067-1070.
[2]. MatthewLewandowski,Nagarajan Ranganathan, and Matthew Morrison"Behavioral Model of Integrated Qubit Gates for Quantum Reversible Logic Design"
[3] V. Vedral, A. Barenco, and A. Ekert, "Quantum networks for elementaryarithmetic operations," *Phys. Rev. A*, vol. 54, no. 1, pp. 147–153, Jul 1996.
[4] Y. Takahashi, "Quantum arithmetic circuits: a survey," *IEICE Trans.Fundamentals*, vol. E92-A, no. 5, pp. 276–1283, 2010.
[5] B.-S. Choi and R. Van Meter, "On the effect of quantum interactiondistance on quantum addition circuits," *J. Emerg. Technol. Comput. Syst.*,vol. 7, pp. 11:1–11:17, August 2011.
[6] H. Thapliyal, H. Jayashree, A. Nagamani, and H. R. Arabnia, "Progressin reversible processor design: A novel methodology for reversible carrylook-ahead adder," in *Transactions on Computational Science XVII*.Springer, 2013, pp. 73–97.
[7] H. Thapliyal and N. Ranganathan, "Design of reversible sequential circuitsoptimizing quantum cost, delay and garbage outputs," *ACM Journal ofEmerging Technologies in Computing Systems*, vol. 6, no. 4, pp. 14:1–14:35, Dec. 2010.
[8] S.Gorgin and A. Kaivani, "Reversible barrel shifters," in *Proc. 2007 Intl.Conf. on Computer Systems and Applications*, Amman, May 2007, pp.479–483.
[9] I. Hashmi and H. Babu, "An efficient design of a reversible barrel shifter,"in *VLSI Design, 2010. VLSID '10. 23rd International Conference on*, Jan2010, pp. 93 –98.
[8] E. Fredkin and T. Toffoli, "Conservative logic," *International J. Theory.Physics*, vol. 21, pp. 219–253, 1982.
[10] S. Kotiyal, H. Thapliyal, and N. Ranganathan, "Design of a reversiblebidirectional barrel shifter," in *Proc. the 11th IEEE NANO*, Portland, Aug.2011, pp. 463–468.

BIOGRAPHY

B.PRADEEP*:* He received his, B.Tech in Electronics & Communication Engineering from QIS College of Engineering Ongole affiliated to JNTU, Kakinada, AP, India and Pursuing M.Tech in VLSI&ES at QIS College of Engineering, Ongole, affiliated to JNTU, Kakinada, AP, India. His areas of interest are VLSI Design and Reversible Logic

V.VISHNUVARDHAN*:* He received the B.Tech Degree in electronics and communication engineering from Jntu Hyderabad, in 2008, and received the M.Tech. Degree in Embedded Systems from Vignan University in 2011. He is currently a Assistant professor in QIS College of Engineering & Technology, Jntuk. His current research interests include Embedded Systems, Image Processing, and Pattern Recognition.