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Design and Testing of PMSM Drive for Automotive Industry

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ABSTRACT: This paper describes the design and testing of PMSM drive for Automotive Industry. The impact of various circuits is discussed in detail. Permanent magnet synchronous motor is used here with three stator windings for the motor operation. Three supply voltage are obtained with the help of three phase MOSFET bridge inverters. MOSFET bridges are fed with fixed dc voltage which is obtained by rectifying ac voltage available from ac mains with the help of diode bridge. Shunt capacitor filter is used for filtering purpose. Operation of the MOSFET bridge is controlled by the control circuit. Gating pulses required to turn the MOSFET On are obtained from the control circuit. By controlling the frequency of the gating pulses frequency of the output from MOSFET bridge is controlled. Control circuit consists of clock generator counter and EPROM. First data required to generate gating pulses is calculated and is stored in EPROM. This data is outputted at the output of the EPROM by generating the address of the memory location with the help of 4 bit binary ripple counter. Clock input required for the operation of the counter is generated using IC 555 in astable mode. Frequency of the gating signals coming out of EPROM is dependent on the frequency with which addressing is done which is turn dependent on the clock frequency. Thus by varying the clock frequency of gating signal is varied. If frequency of gating signal is varied, then the MOSFET bridge output frequency is also varied. Thus we obtain variable frequency output.

Gating signal outputted by EPROM cannot be directly applied to MOSFET bridge as they are very weak. So isolator and driver circuit is used. Necessary isolation of low power control circuit from high power bridge circuit is obtained by using opt isolator.

The Experiment results show that by varying the inverter frequency the speed of the motor also gets varied. If the frequency increases the speed of the motor also increases and if the frequency decreases the speed of the motor also decreases. If the frequency is kept constant at particular value, the speed of the motor also remains constant, irrespective of the load.

Keywords: Permanent magnet synchronous machine. Permanent magnet material, MOEFET Inverter Circuit, clock signal generator, address generator, EPROM, Electric power Steering.

I. INTRODUCTION

Permanent magnet synchronous motors (PMSM) are widely used in high-performance drives such as industrial robots and machine tools for their advantages on high power density, high-torque, free maintenance and so on. In recent years, the magnetic and thermal capabilities of the PM have been considerably increased by employing the high-coercive PM materials [1]. In last few years, permanent magnet synchronous motor (PMSM) consequently is acquired in more and more far-ranging application, because of its properties such as small volume, light weight, high efficiency, small inertia, rotor without heat problem, etc. [2]. Space vector pulse width modulation DTC is a technique to reduce the ripples of the electromagnetic torque and flux linkage. Direct Torque Control (DTC) is a new control method after vector control. It abandons decoupling thought of vector control, and uses the stator flux linkage directly to control the flux linkage and the torque of motor. Thus, the dynamic response of the System is very fast [3]. The DTC control strategy is applied for PMSM in order to improve the torque characteristics of the motor, which currently has caused the extensive attention of people. The traditional DTC usually adopts bang-bang control strategy to implement. But this control strategy cannot meet the

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system requirements both of torque and flux linkage at the same time, which leads to large fluctuations of flux linkage and torque generated by system and leads to the problem of pulse current and switches noise caused by higher switching frequency changes. The electrical machine that converts electrical energy into mechanical energy, and vice versa, is the workhorse in a drive system. Drive systems are widely used in applications such as fibers spinning mills, rolling mills, MAGLEV - linear synchronous motor propulsion, aircraft engines, paper and textile mills, electric vehicle and subway transportation, home appliances, wind generation systems, servos and robotics, computer peripherals, steel and cement mills, ship propulsion, etc. A machine is a complex structure electrically, mechanically, and thermally. Although machines were introduced more than one hundred years ago, the research and development (R&D) in this area appears to be never-ending. However, the evolution of machines has been slow compared to that of power semiconductor devices and power electronic converters. An engineer designing a high-performance drive system must have the knowledge about machine performance, the dynamic model, and parameter variations. Industrial drive applications are generally classified into constant-speed and variable-speed drives. Traditionally, ac machines with a constant frequency sinusoidal power supply have been used in constant-speed applications, whereas dc machines were preferred for variable-speed drives. Dc machines have the disadvantages of higher cost, higher rotor inertia, and maintenance problems with commutator and brushes. Commutator and brushes, in addition, limit the machine speed and peak current, cause EMI problems, and do not permit a machine to operate in dirty and explosive environments. However, dc machine drive converters and controls are simple, and the machine torque response is very fast.

II. PMSM DRIVE DESIGN CONSIDERATIONS

The following aspects of the system design are described in this section: Diode Bridge rectifier with filter, Power Circuit, Control Circuit, Isolator and driver circuit, over current Protection Circuit, Power Supply for Control Circuit, Protection of devices and circuits.

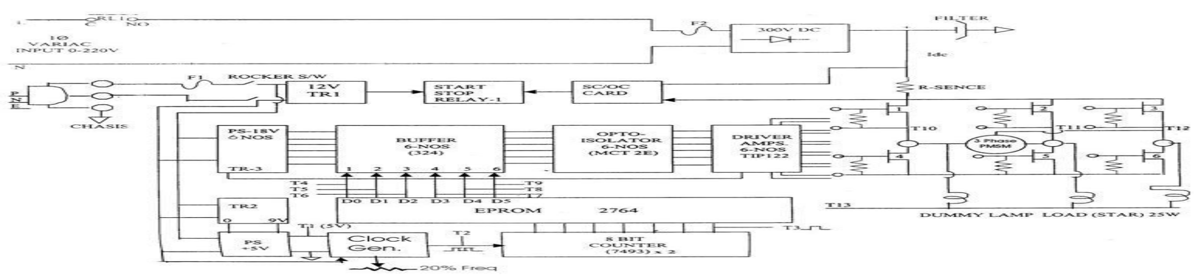

Fig 1: system Block Diagram of PMSM Drive

A. Diode Bridge rectifier with filter

This circuit converts the available ac line voltage into required dc voltage for the next circuit. i.e. main power circuit. It uses four diode D_1, D_2, D_3 and D_4 in bridge configuration as shown in fig.2. Diode bridge converts ac to dc. This dc voltage is not pure dc voltage but contains ac ripples in it. So capacitor is connected across the output of the bridge rectifier which filters out ac contained in the dc and gives almost pure dc voltage.

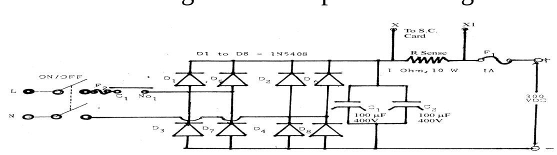

Fig 2: Circuit Diagram of Diode Bridge Rectifier with Filter

B. Power Circuit

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The power circuit is a three phase bridge inverter using MOSFETs which converts dc power into ac power at desired output voltage and frequency. The center points of the transistor connection are used to take the output. Power MOSFET device permit the highest switching frequency although their power handling capability is limited. Their on state resistance increases approximately with the power of 2.6 as the blocking voltage increases, rendering the efficiency of high voltage MOSFET device low. Their typical ratings are about 50 A, 500V and 20KHz.

A basic three phase inverter is a six step bridge inverter with six semiconductor switching device. In inverter terminology, a step is defined as a change in the firing from one switch to other in proper sequence. For one cycle of 360^0, each step would be of 60^0 interval for a six step inverter.

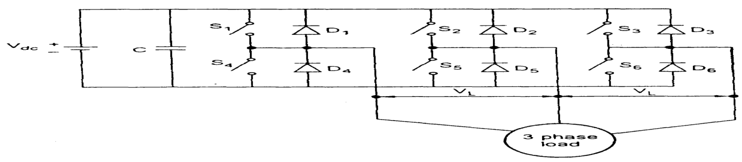

Fig 3: Three Phase Bridge Inverter

Fig.3 shows the inverter with six semiconductor switched and the diodes. For simplicity the gating circuit are omitted. Let the three phase load be connected in star. These are two possible patterns of providing pulses to these switches. In one pattern, each switch conducts for 180^0 and in the other each switch conducts for 120^0. But in both these patterns gating signals are applied and removed at 60^0 intervals of the output voltage waveform. Therefore both these modes require a six step bridge inverter.

In this drive 120^0 mode is used. The voltage waveforms and the firing sequence is shown in the fig. 3.4 (please refer fig. 3.4 on net page). It can be seen from the first row of the table that S1 conducts for 120^0 and for the next 60^0, neither S1 nor S4 conducts. Now S4 is on at 180^0 and it further conducts for 120^0 i.e. unto 300^0. This means that for 60^0 interval series connected switches do not conduct. At 300^0 S4 is turned off, then 60^0 interval elapses before S1 is turned on again at 360^0.

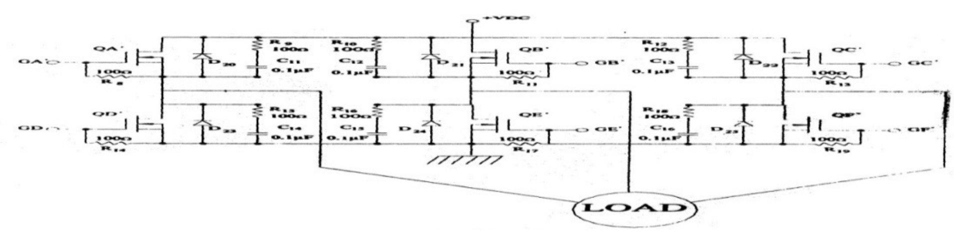

Fig 4: Main Power Circuit (MOSFET Bridge with Snubber)

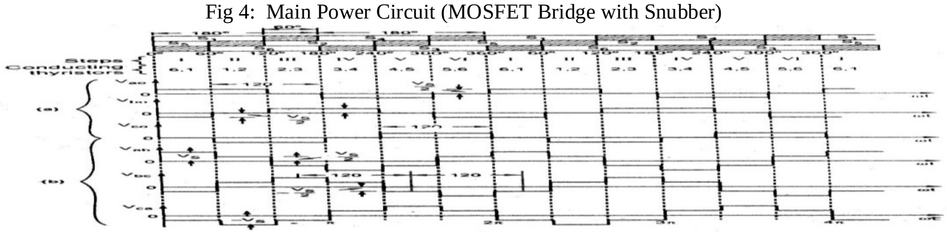

Fig 5: Voltage Waveforms for 120^0 mode six-step 3-Phase VSI

In the second row, S2 is turned on at 120^0 which conducts for 120^0, then 60^0 interval elapses during which neither S2 and S5 conducts. At 300^0, S5 is turned on and it conducts for 120^0 after which S2 is turned on again with time interval

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of 60^0, in between. The third row is also completed similarly. The sequence in which the switches are fired is 1-6-2-4-3-5 and generate two step or quasi square wave format. During each step, only two switches conduct for this inverter-one from the upper group and one from the lower group. Any one of the load terminals always remains open in this case. in first step, the line to neutral voltages are given below.

$V_{a0} = V_s / 2, \quad V_{0b} = V_s / 2$

$V_{b0} = V_s / 2$ and $V_{c0} = 0$

The line voltage are given by

$V_{ab} = V_{a0} - V_{c0}$

$V_{bc} = V_{b0} - V_{c0}$

$V_{ca} = V_{c0} - V_{a0}$

It can be seen from the waveform that phase voltage have one positive pulse and one negative pulse (each of 120^0 duration) for one cycle of output alternating voltage. The line voltage however, have six steps per cycle of output alternating voltage. The merits and demerits of 120-degree mode inverter over 180-degree mode inverter are as follows

i) In the 180^0 mode inverter, when gate signal is cut off to turn off S1 at $\omega t = 180^0$, gating signal for switch S4 is simultaneously applied to turn on S4 in the same leg. In practice a commutation interval must exist between the removal of first gating pulse and applications of the other pulse. Otherwise dc source would experience a direct short circuit through S1 and S4 in the same leg.

This difficulty is overcome considerably in 120-degree mode inverter. In this inverter, there is a 60^0 interval between the turning off of S1 and turning on of S4. The interval of 60^0 in between is sufficient for the commutation. In general, this angular interval of 60^0 exists between the turning off of one device and turning on of the complementary device in the same leg.

ii) In this mode of inverter, the potentials of only two output terminals connected to the dc source are defined at any time of the cycle. The potential of the third terminal, pertaining to the particular leg in which neither device is conducted is not well defined its potential therefore depends on nature of load circuit. Thus analysis of this type inverter circuit is complicated for a general load circuit.

The Fourier Analysis of line voltage waveform V_{ab} shown in fig.

$$V_{ab} = \sum_{n=6k+1}^{\infty} \frac{3V_{dc}}{n\pi} \sin n\left(\omega t + \frac{\pi}{3}\right) \quad \text{where} \quad k = 0,1,2,3,.....$$

similar expressions for V_{bc} and V_{ca} can also be written R.M.S. value of fundamental phase voltage is

$V_{Pt} = 2V_{dc} / \sqrt{2} . \pi \text{ x } \cos \pi/6$

$= 0.3898\ V_s$

R.M.S. value of phase voltage,

$V_P = [1/\pi \int_0^{2p/3} (V_{dc}/ 2)^2 \text{ x } d(\omega t)]^{1/2}$

$= \sqrt{2/3}\ V_{dc} / 2 = V_{dc} / \sqrt{6} = 0.4082\ V_{dc}$

R.M.S. value of fundamental line voltage is

$V_{L1} = 3V_{dc} / \sqrt{2}\pi = 0.6752\ V_{dc} = \sqrt{3}\ V_{p1}$

R.M.S. value of line voltage,

$V_L = \sqrt{3}\ V_{p1} = V_{dc} / \sqrt{2} = 0.7071\ V_{dc}$

C. Control Circuit

The control circuit consists of the clock signal generator, address generator for EPROM, data base stored in EPROM, logic circuits and optical solators.

Clock signal generator

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It consists of timer 555 operated in as table mode. The clock generator runs at a very high frequency (256 times that of the output frequency). An astable multivibrator is a rectangular wave generating circuit is also called free running multivibrator as it dose not require external trigger to change the state of the output. Fig.3.6 shows the 555 timer connected in astable mode.

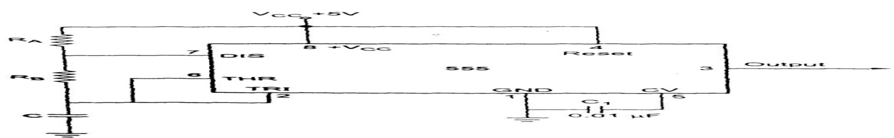

Fig 6: 555 Circuit diagram in astable mode

The output of 555 is given as clock signal to the counter IC 7493 which generates the address lines for the EPROM.

i. *Address Generator* It consists of IC 7493 which is used for generating the address for the EPROM. This IC has four J-K flip flops with outputs Q_0, Q_1, Q_2 and Q_3. Q_0 is the LSB and Q_3 is the MSB. The flip-flops are shown arranged with LSB on the left.

Each flip-flop has a CP (clock pulse) input, which is just another name for the CLK input. The clock inputs to Q_0 and Q_1labeled CP_0 and CP_1 respectively, are externally accessible. The inversion bars over these inputs indicate that they are activated by a NGT.

Each flip-flop has an asynchronous CLEAR input, C_D. These are connected together to the output of a two input NAND gate with input MR_1 and MR_2 where MR stands for Master Reset. Both MR inputs must be HIGH to clear the counter to 0000.

The logic diagram and symbol for 7493 is shown in fig (a) and (b).

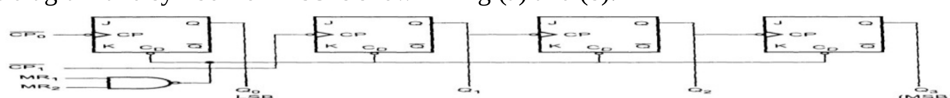

Fig 7: Logic diagram for IC 7493

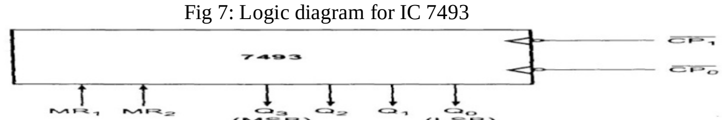

Fig 8: simplified Symbol for 7493

Flip-flops Q_1, Q_2, and Q_3 are already connected as a 3 bit ripple counter. Flip flop is not connected to anything internally. This allows the used the option of either connecting Q_0 to Q_1 to form a 4 bit counter or using Q_0 separately if desired.

In the controller here, 2 such IC's are used to generate 256 address lines as the data is stored in these locations. The output of these counter are respectively the address lines for the EPROM 2764.

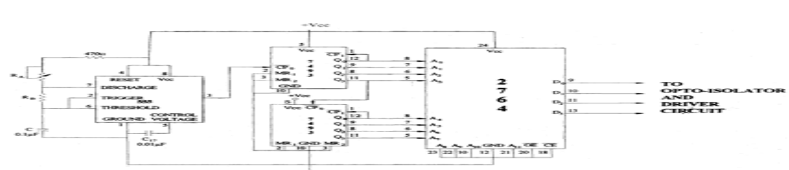

Fig 9: Circuit diagram of Control Circuit

ii. *EPROM*

The output generated by IC 7493 act as address lines for the EPROM wherein data base for the 120^0 mode of conduction for the inverter is stored. An EPROM can be programmed by the user and it can also be erased and

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reprogrammed as often as desired. Once programmed, the EPROM is a non-volatile memory that will hold its stored data indefinitely.

The process of programming an EPROM involves the application of special voltage levels (typically in the 10-25 V) to the appropriate chip inputs for a specified amount of time range (typically 50 ms per address location). The programming process is usually performed by a special programming circuit that is separate from the circuit in which the EPROM will eventually be working. The complete programming process can take upto several minutes for one EPROM chip.

The data stored in EPROM is square pulse signal for 120^0 mode. It is taken out by data line D_0 to D_5 . There are 13 address line, out of that only 8 (A_0 to A_7) address lines are used.

D. Isolator and driver circuit

Fig. shows isolator and driver circuit. Square wave pulses are available at the output of the control circuit. Which have phase relations as per the requirement. The power circuit is operating at very high voltage while control circuit is operating at very less voltage as compared to power circuit. So the control circuit ground and power circuit ground must be isolated from each other to protect control circuit from any damage due to malfunctioning in power circuit. It isolation is not used then it may be dangerous to operator. Also without isolation when gate pulses are applied the device become on and live terminal of supply is connected to ground of control circuit and power circuit. Any operation trying to control the circuit is likely to touch control ground (which is usually supposed to be the safest potential) and in fact is directly in contact with the live terminal of supply. Thus it is dangerous for the operation. This isolation is very much essential.

III.RESULTS ANALYSIS

Table No.1: Variation in the speed of the motor as a function of inverter frequency

Sr.No.	Time (m.s.)	Frequency (Hz)	Expected Speed (rpm)	Measured Speed (rpm)	Voltage (Volts)
1	30	33.3	999	1010	265
2	25	40	1200	1226	270
3	22	45.4	1362	1380	270
4	20	50	1500	1520	270
5	18	55.5	1665	1682	270
6	17	59	1770	1790	270

Table No.2: Variation of speed vs load at constant frequency of 33.3 Hz

Sr.No.	Load (gm)	Expected Speed (rpm)	Measured Speed (rpm)	Voltage (volts)
1	500	999	1010	270
2	1000	999	1010	270
3	1500	999	1010	270
4	2000	999	1010	270
5	2500	999	1010	270
6	3000	999	1010	270

Table No.3: Variation of speed vs load at constant frequency of 40 Hz

Sr.No.	Load (gm)	Expected Speed (rpm)	Measured Speed (rpm)	Voltage (Volts)
1	500	1200	1226	270
2	1000	1200	1226	270
3	1500	1200	1226	270
4	2000	1200	1226	270
5	2500	1200	1226	270
6	3000	1200	1226	270

Table No.4: Variation of speed vs load at constant frequency of 45.4 Hz

Sr.No.	Load (gm)	Expected Speed (rpm)	Measured Speed (rpm)	Voltage (Volt)
1	500	1362	1380	270
2	1000	1362	1380	270
3	1500	1362	1380	270
4	2000	1362	1380	270
5	2500	1362	1380	270
6	3000	1362	1380	270

Table No.5 Variation of speed vs load at constant frequency of 50 Hz

Sr.No.	Load (gm)	Expected Speed (rpm)	Measured Speed (rpm)	Voltage (Volt)
1	500	1500	1520	270
2	1000	1500	1520	270
3	1500	1500	1520	270
4	2000	1500	1520	270
5	2500	1500	1520	270
6	3000	1500	1520	270

Table No 6: Variation of speed vs load at constant frequency of 55.5 Hz

Sr.No.	Load (gm)	Expected Speed (rpm)	Measured Speed (rpm)	Voltage (Volt)
1	500	1665	1682	265
2	1000	1665	1682	265
3	1500	1665	1682	265
4	2000	1665	1682	265
5	2500	1665	1682	265
6	3000	1665	1682	265

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Table No.7: Variation of speed vs load at constant frequency of 59 Hz.

Sr.No.	Load (gm)	Expected Speed (rpm)	Measured Speed (rpm)	Voltage (Volt)
1	500	1770	1790	265
2	1000	1770	1790	265
3	1500	1770	1790	265
4	2000	1770	1790	265
5	2500	1770	1790	265
6	3000	1770	1790	265

RESULT TABLE:-

Table 1:

Sr. No.	Load (gm)	Frequency (Hz)	Speed (rpm)	Torque (N-m)	Output Power (W)
1	500	33.3	1010	0.14715	15.55
2	1000	33.3	1010	0.2943	31.12
3	1500	33.3	1010	0.4414	46.68
4	2000	33.3	1010	0.5886	62.19
5	2500	33.3	1010	0.7357	77.81
6	3000	33.3	1010	0.8829	93.38

Table 2:

Sr. No.	Load (gm)	Frequency (Hz)	Speed (rpm)	Torque (N-m)	Output Power (W)
1	500	40.0	1226	0.14715	18.93
2	1000	40.0	1226	0.2943	37.78
3	1500	40.0	1226	0.4414	56.66
4	2000	40.0	1226	0.5886	75.56
5	2500	40.0	1226	0.7357	94.45
6	3000	40.0	1226	0.8829	113.35

Table 3:

Sr. No.	Load (gm)	Frequency (Hz)	Speed (rpm)	Torque (N-m)	Output Power (W)
1	500	45.4	1380	0.14715	21.31
2	1000	45.4	1380	0.2943	42.53
3	1500	45.4	1380	0.4414	63.78
4	2000	45.4	1380	0.5886	85.06
5	2500	45.4	1380	0.7357	106.31
6	3000	45.4	1380	0.8829	127.59

Table 4:

Sr. No.	Load (gm)	Frequency (Hz)	Speed (rpm)	Torque (N-m)	Output Power (W)
1	500	50	1520	0.14715	23.47
2	1000	50	1520	0.2943	46.84
3	1500	50	1520	0.4414	70.25
4	2000	50	1520	0.5886	93.68
5	2500	50	1520	0.7357	117.1
6	3000	50	1520	0.8829	140.5

Table 5:

Sr. No.	Load (gm)	Frequency (Hz)	Speed (rpm)	Torque (N-m)	Output Power (W)
1	500	59	1790	0.14715	27.64
2	1000	59	1790	0.2943	55.16
3	1500	59	1790	0.4414	82.73
4	2000	59	1790	0.5886	110.33
5	2500	59	1790	0.7357	137.90
6	3000	59	1790	0.8829	165.49

Table 6:

Sr. No.	Load (gm)	Frequency (Hz)	Speed (rpm)	Torque (N-m)	Output Power (W)
1	500	55.5	1682	0.14715	25.98
2	1000	55.5	1682	0.2943	51.83
3	1500	55.5	1682	0.4414	77.74
4	2000	55.5	1682	0.5886	103.67
5	2500	55.5	1682	0.7357	129.58
6	3000	55.5	1682	0.8829	155.51

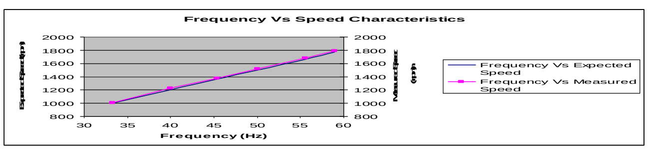

Fig 1: Frequency Vs Speed characteristics

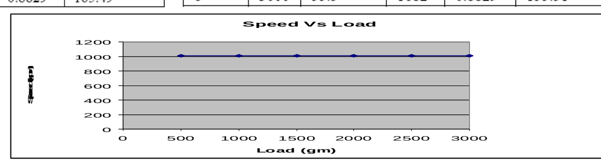

Fig 2: Speed Vs Load Characteristics at Constant Frequency = 33.3 Hz

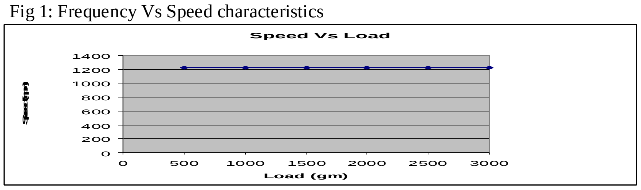

Fig. 3: Speed Vs Load Characteristics at Constant Frequency = 40 Hz

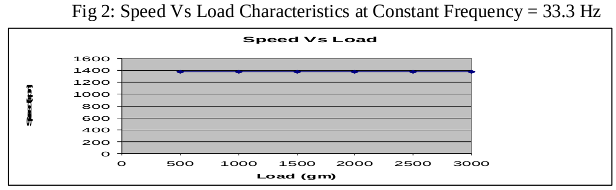

Fig 4: Speed Vs Load Characteristics at Constant Frequency = 45.4 Hz

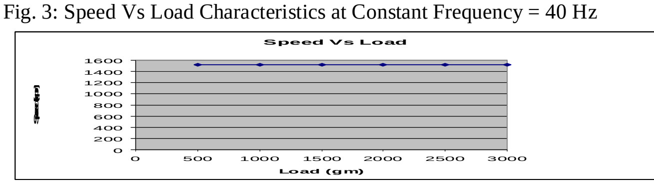

Fig 5: Speed Vs Load Characteristics at Constant Frequency = 50 Hz

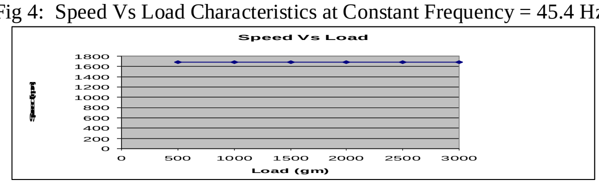

Fig. 6: Speed Vs Load Characteristics at Constant Frequency = 55.5 Hz

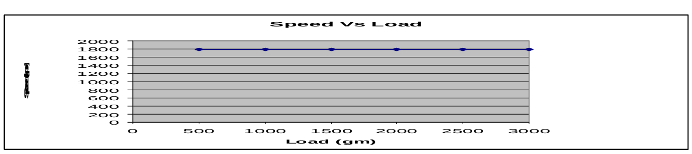

Fig 7: Speed Vs Load Characteristics at Constant Frequency = 59 Hz

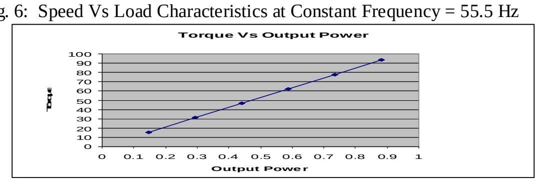

Fig 8: Torque Vs Output Power at frequency 33.3 Hz

Fig 9: Speed Vs Torque at Constant Frequency = 50 Hz

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IV. CONCLUSION

The Experiment results show that by varying the inverter frequency the speed of the motor also gets varied. If the frequency increases the speed of the motor also increases and if the frequency decreases the speed of the motor also decreases. If the frequency is kept constant at particular value, the speed of the motor also remains constant, irrespective of the load. Hence PMSM drive is suitable for Automotive Industry.

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