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Design of Energy Aware Data Processing Architecture for Wireless Sensor Nodes

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ABSTRACT— Wireless Sensor Networks (WSN) has become a very significant enabling technology in civil, military, radio communication and medical applications for collecting and processing of complex environmental data. Radio communication has highest energy consumption in wireless sensor nodes. Sensor nodes are battery driven and have lifetime on the order of months to years. Hence, energy consumption is the important factor in determining sensor nodes lifetime. To reduce the number of processing elements in sensor nodes, folded tree architecture is used. Here proposing, DVFS (Dynamic Voltage and Frequency Scaling) algorithm is used along with folded tree architecture to reduce power and to improve performance of sensor nodes. As wireless nodes are expensive to buy replace it's important to increase life time of nodes in order to increase life time of nodes we are going to use folded tree architecture.to reduce power in wireless sensor node by using reused technology of PES(processing elements).in previous works they used 2N number of PES. In our project we used half amount of PE. Software used xilinix, proposed to work –combination of energy saving algorithm and hardware decreases power and increases node life time.

KEYWORDS—Folded tree; Processing element; Wireless sensor network; Dynamic voltage frequency scaling

I. INTRODUCTION

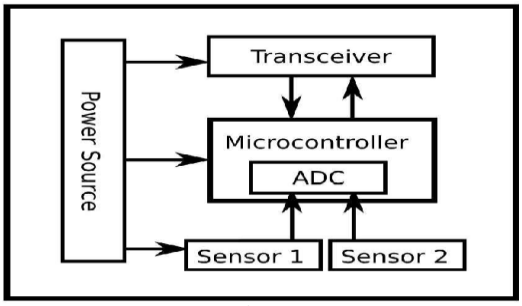
Wireless sensor network (WSN) applications range from medical monitoring to environmental sensing, industrial inspection, and military surveillance. WSN nodes essentially consist of sensors, a radio, and a microcontroller combined with a limited power supply, e.g., battery or energy scavenging. Since radio transmissions are very expensive in terms of energy, they must be kept to a minimum in order to extend node lifetime. The ratio of communication-to computation energy cost can range from 100 to 3000. So data communication must be traded for on-the-node processing which in turn can convert the many sensor readings into a few useful data values. The data-driven nature of WSN applications requires a specific data processing approach. Previously, we have shown how parallel prefix computations can be a common denominator of many WSN data processing algorithms. Hence to fill this gap this paper attempts to increase the lifetime of wireless sensor nodes to minimize the power consumed by processing the elements of WSN, in which the existing works were fail to explore. VirtexV and Xilinx are used as solution methodology for calculating the power and showing the simulated results respectively.

II. WIRELESS SENSOR NETWORK

A Wireless Sensor Network (WSN) consists of spatially distributed autonomous wireless sensor nodes. A node in a wireless network is able to collect the information from sensors, process it and communicate wirelessly with other nodes in the network to monitor physical or environmental conditions, such as temperature, sound, vibration, pressure, motion or pollutants and to cooperatively pass their data through the network to a main location.

A. Components of wireless sensor network

A typical sensor network device comprises the following components some of which are optional: power supply, microcontroller, wireless communication channel, wired communication, sensor, local storage, and real time clock systems. The principal idea is that the sensors are connected to a tiny computer that coordinates the measurement, pre-processes, stores and delivers the information.



Block diagram of a Wireless Sensor Node

The following is a list of electronic components commonly used in sensor network devices. First, Microcontrollers, radio transceivers, sensors, power/batteries

B. *Factors influcening sensor network design*

- Fault Tolerance
- Scalability
- Production cost
- Transmission Media
- Power consumption

C. *Applications*

- Area monitoring
- Health care monitoring
- Air pollution monitoring
- Forest fire detection
- Landslide detection
- Water quality monitoring
- Natural disaster prevention
- Machine health monitoring
- Data logging
- Water/waste water monitoring

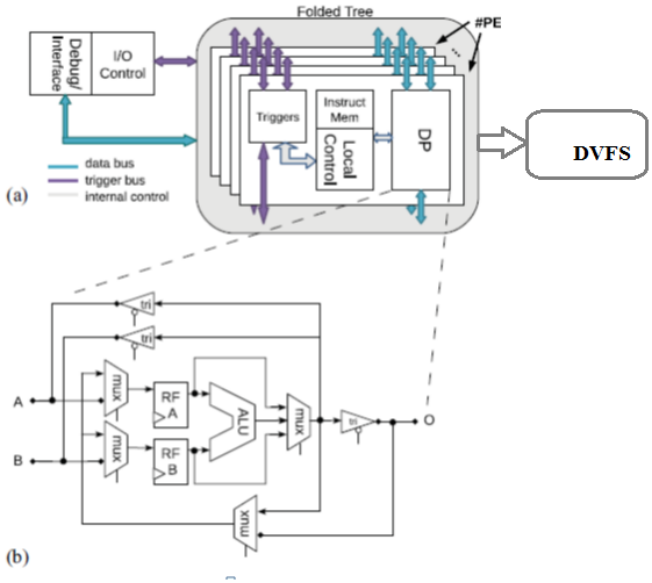
III. PROPOSED SYSTEM

Before you begin to format your paper, first write and save the content as a separate text file. Keep your text and graphic files separate until after the text has been formatted and styled. Do not use hard tabs, and limit use of hard returns to only one return at the end of a paragraph. Do not add any kind of pagination anywhere in the paper. Do not number text heads-the template will do that for you.

Finally, complete content and organizational editing before formatting. Please take note of the following items when proofreading spelling and grammar:

A. *Folded tree*

However, a straightforward binary tree implementation of Blelloch's approach as shown in Fig. costs a significant amount of area as n inputs require $p = n - 1$ PEs. To reduce area and power, pipelining can betraded for throughput. With a classic binary tree, as soon as a layer of PEs finishes processing, the results are passed on and new calculations can already recommence independently. The idea presented here is to fold the tree back onto itself to maximally reuse the PEs as shown in fig. 4.4. In doing so, p becomes proportional to $n/2$ and the area is cut in half. Note that also the interconnect is reduced. On the other hand, throughput decreases by a factor of log2 *(n) but* since the sample rate of different physical phenomena relevant for WSNs does not exceed 100 kHz, this leaves enough room for this trade-off to be made. This newly proposed folded tree topology is depicted in Fig on the right, which is functionally equivalent to the binary tree on the left.



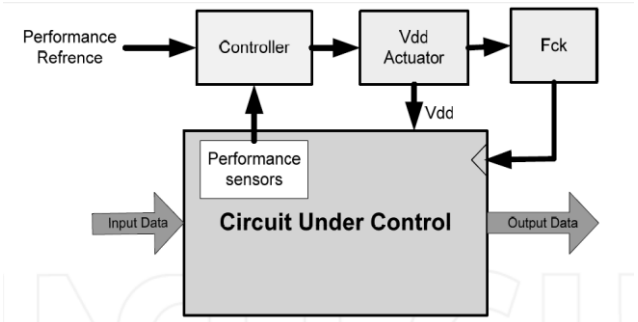
Block diagram of proposed system

They are interconnected through the request-acknowledge handshaking trigger bus and the bidirectional data bus in the folded way. Handshaking triggers activate the PEs only when new data is available and in such a way that they functionally become a binary tree in both directions of the trunk- and twig-phase. Within each data path, muxes select external data, stored data or the previous result as the next input for the data path. The data path contains an algorithmic logical unit (ALU) with four-word deep register files (RF-A and RF-B) at the inputs A and B for operand isolation. These RFs comprise the distributed data memory of the whole system, with a combined capacity of 4 KB. They are the only clocked elements within the data path. As data flows through the tree, it is constantly kept local to its designated operation. Goal is to remove bottleneck and saves power.

(*sponsors*).

IV. APPLICATION OF THE PROPOSED SYSTEM

A. Algorithm



In this block diagram, there are three main components. The first component is a performance sensor that monitors the main specification of the processor e.g. average of supply current, temperature and supply voltage variations. The second component is the controller. This controller block works based on an input data received from the sensors by comparing it with the reference performance received from the power management unit or software to decide the change in supply voltage when necessary. The third block is the supply voltage actuator that can be on-chip or off-chip, e.g. a DC-DC converter and clock frequency actuators that can be a PLL. Since reducing the supply voltage causes increasing the delay of circuits, controlling the voltage and frequency of a processor dramatically depends on the accuracy of the controller.

B. Software used

XILINX ISE:

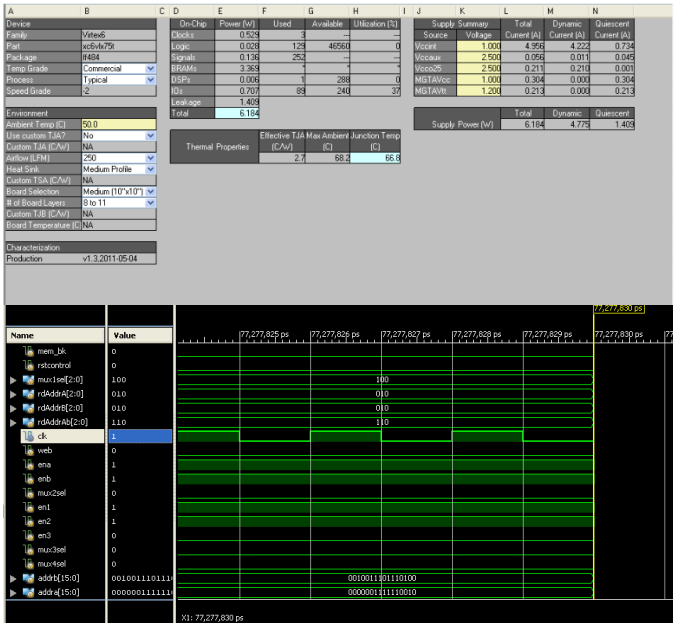
Xilinx ISE (**I**ntegrated **S**oftware **E**nvironment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.

Virtex:

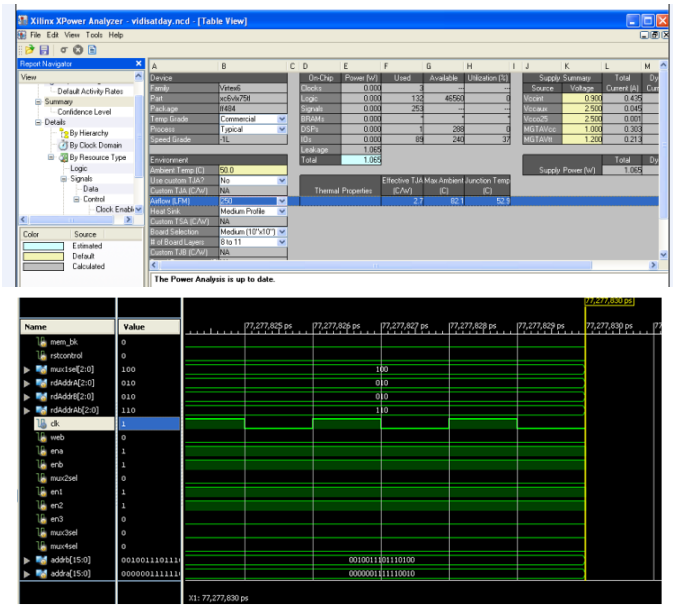
The Virtex series of FPGAs have integrated features that include FIFO and ECC logic, DSP blocks, PCI-Express controllers, Ethernet MAC blocks, and high-speed transceivers. In addition to FPGA logic, the Virtex series includes embedded fixed function hardware for commonly used functions such as multipliers, memories, serial transceivers and Microprocessor cores. These capabilities are used in applications such as wired and wireless infrastructure equipment, advanced medical equipment, test and measurement, and defense systems. Some Virtex family members are available in radiation-hardened packages, specifically to operate in space where harmful streams of high-energy particles can play havoc with semiconductors. The Virtex-5QV FPGA was designed to be 100 times more resistant to radiation than previous radiation-resistant models and offers a ten-fold increase in performance. However, characterization and test data were not yet available for the Virtex-5QX on the Xilinx Radiation Test Consortium website as of November 2011.

V. RESULTS

A. Existing results



B. Proposed system results



C. Comparison table:

MEHTOD	POWER	DELAY
Existing method	6.184	5.792
Proposed method	1.065	3.240

VI. CONCLUSION

This project presented the folded tree architecture of a digital signal processor for WSN applications. The design exploits the fact that many data processing algorithms for WSN applications can be described using parallel-prefix operations, introducing the much needed flexibility. Energy is saved by adopting following techniques:

1) Limiting the data set by pre-processing with parallel-prefix operations;

2) The reuse of the binary tree as a folded tree; and

3) The combination of data flow and control flow elements to introduce a local distributed memory, which removes the memory bottleneck while retaining sufficient flexibility. In future, low power algorithm is used along with folded tree architecture to reduce power consumption during processing of data in sensor nodes

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