ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 6, June 2014

Design of Low Power Transceiver for OFDM Based WLAN Systems

[1]Naveen L J, [2]Vinutha C B, [3]Abdul Imran Rashid, [4]Dr. M Z Kurian

[1]4th Semester, M. Tech (Digital Electronics), SSIT, Tumkur, Karnataka, India.

[2]Assistant Professor, Dept. of ECE, SSIT, Tumkur, Karnataka, India.

[3]Asst. Prof., Dept. of EEE, MSRSAS, Bangaluru, Karnataka, India.

[4]HOD, Dept. of ECE, SSIT, Tumkur, Karnataka, India.

ABSTRACT- In digital communication Orthogonal Frequency Division Multiplexing (OFDM) is regarded as a promising technology in recent years. In this paper, propose low power transceiver for OFDM based wireless local area network (WLAN) system using Application Specific Integrated Circuit (ASIC) platform. As per the IEEE standard 802.11a OFDM based transceiver are capable of providing data rates up to tens of Mbps but OFDM transceiver will dissipate huge amount of power. The objective of the work is the optimization with respect to power & area. It includes various low power libraries as well as ample amount of low power constrain.

KEYWORDS: OFDM, WLAN, ASIC, low power transceiver, IEEE 802.11a.

I. INTRODUCTION

Orthogonal frequency division multiplexing (OFDM) is a special case of multicarrier transmission, where a single data stream is transmitted over a number of lower rate subcarriers. OFDM can be seen as either a modulation technique or a multiplexing technique [1]

One of the main reasons to use OFDM is to increase the robustness against frequency selective fading or narrowband interference. In a single carrier system, a single fade or interferer can cause the entire link to fail, but in a multicarrier system, only a small percentage of the subcarriers will be affected. Error correction coding can then be used to correct for the few erroneous subcarriers [1], [2]

II. LITEARTURE SURVEY

(a). Orthogonal Frequency Division Multiplexing.(OFDM)

Orthogonal Frequency Division Multiplexing (OFDM) is one of the Multi-Carrier Modulation (MCM) techniques that transmit signals through multiple carriers. These carriers (subcarriers) have different frequencies and they are orthogonal to each other. Orthogonal frequency division multiplexing techniques have been applied in both wired and wireless communications, such as the IEEE 802.11a standard [1], [2].

(b). Orthogonality.

Orthogonality is defined for both real and complex valued functions. The functions $\phi_m(t)$ and $\phi_n(t)$ are said to be orthogonal with respect to each other over the interval $a < t < b$ if they satisfy the condition.

$$\int_a^b \phi_m(t)\phi_n^*(t)\,dt = 0, where\ n \neq m$$

OFDM splits the available bandwidth into many narrowband channels (typically 100-8000), each with its own sub-carrier. These sub-carriers are made orthogonal to one another, meaning that each one has an integer number of cycles over a symbol period. Thus the spectrum of each sub-carrier has a “null” at the centre frequency of each of the other sub-carriers in the system, as demonstrated in Figure 2.1. This results in no interference between the sub-carriers, allowing them to be spaced as close as theoretically possible. Because of this, there is no great need for users of the

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 6, June 2014

channels to be time-multiplexed, and there is no overhead associated with switching between users. This overcomes the problem of overhead carrier spacing required in FDMA [1], [2], [3].

III. LOW POWER AT DIFFERENT LEVELS OF VLSI DESIGN

Low power chip requirement in the VLSI industry is main considerable field due to the reduction of chip dimension day by day and environmental factors. [4]
Low Power Design Methodologies presents the first in-depth coverage of all the layers of the design hierarchy, ranging from the system layer, architectural levels, logic and circuit, up to the technology.[4]

(a) System Level

A system typically consists of both hardware and software components, which affect the power consumption. The system design includes the hardware/software partitioning, hardware platform selection (application-specific or general purpose processors), resource sharing (scheduling) strategy, etc. The system design usually has the largest impact on the power consumption and hence the low power techniques applied at this level have the most potential for power reduction.[4],[7].
The power-down and clock gating are two of the most used low power techniques at system level. The non-active hardware units are shut down to save the power. The clock drivers, which often consume 30-40% of the total power consumption, can be gated to reduce the switching activities as illustrated in Fig 1

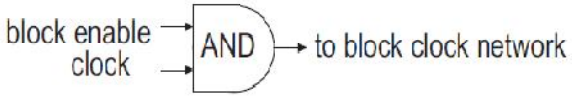

Fig 1: Clock gating.

(b) Algorithm Level

The algorithm selections have large impact on the power consumption. For example, using fast Fourier transform instead of direct computation of the DFT reduces the number of operations with a factor of 8 for an 8-point Fourier transform and the power consumption is likely to be reduced with a similar factor. The task of algorithm design is to select the most energy efficient algorithm that just satisfies the constraints. The cost of an algorithm includes the computation part and the communication/storage part. The complexity measurement for an algorithm includes the number of operations and the cost of communication/storage. Reduction of the number of operations, cost per operation, and long distance communications are key issues to algorithm selection.

One important technique for low power of the algorithmic level is algorithmic transformations. This technique exploits the complexity, concurrency, regularity, and locality of an algorithm .Reducing the complexity of an algorithm reduces the number of operations and hence the power consumption. The possibility of increasing concurrency in an algorithm allows the use of other techniques, e.g., voltage scaling, to reduce the power consumption. The regularity and locality of an algorithm affects the controls and communications in the hardware [6], [8].

(c) Architecture Level

The implementation dependent part of the power consumption of a system is strongly related to a number of properties that a given system or algorithm. The component that contributes a significant amount of the total energy consumption is the interconnect. The power consumption of the interconnect is highly dependent on algorithm and architecture-level design decisions. Two properties of algorithms are important for reducing interconnect power consumption are locality and regularity [6].
Locality relates to the degree to which a system or algorithm has natural isolated clusters of operation or storage with a few interconnections between them. Partitioning the system or algorithm into spatially local clusters ensures that the majority of the data transfers take place within the clusters and relatively few between clusters. The result is that the local buses are shorter and more frequently used than the longer highly capacitive global buses.
Regularity in an algorithm refers to the repeated occurrence of computational patterns. Common patterns enable the design of less complex architecture and therefore simpler interconnect structure (buses, multiplexers, buffers) and less control hardware.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 6, June 2014

As the algorithm is selected, the architecture can be determined for the given algorithm. As it can see from Eq. (2.16), an efficient way to reduce the dynamic power consumption is the voltage scaling. When supply voltage is reduced, the power consumption is reduced. However, this increases the gate delay. The delay of min-size inverter (0.35 mm standard CMOS technology) increases as the supply voltage is reduced. [6] [8].

(d) Logic Level

The power consumption depends on the switching activity factor, which in turn depends on the statistical characteristics of data. However, most low power techniques do not concentrate on this issue from the system level to the architecture level. The low power techniques at the logic level, however, focus mainly on the reduction of switching activity factor by using the signal correlation and, of course, the node capacitances [6], [9].

(e) Circuit Level

At the circuit level, the potentials power saving are often less than that of higher abstract levels. However, this cannot be ignored. The power savings can be significant as the basic cells are frequently used. A few percents improvement for D flip-flop can significantly reduce the power consumption in deep pipelined systems [9].

In CMOS circuits, the dynamic power consumption is caused by the transitions. Spurious transitions typically consume between 10% and 40% of the switching activity power in the typical combinational logic. In some cases, like array multipliers, the amount of spurious transitions is large. To reduce the spurious transitions, the delays of signals from registers that converge at a gate should be roughly equal. This can be done by insertions of buffers and device sizing. The insertions of buffer increase the total load capacitance but can still reduce the spurious transitions. This technique is called path balancing [6], [9]

IV. SYSTEM DESIGN

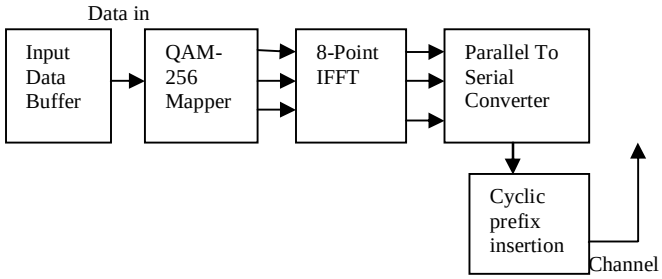

Fig 2: Block diagram of OFDM transmitter

Fig 2 shows the simplified block diagram of OFDM transmitter. The generation of OFDM signal started from amplitude modulation mapping bank. The serial input data is mapped to appropriate symbol to represent the data bits. These symbols are in serial and need to convert into parallel format since IFFT module requires parallel input to process data. The serial to parallel module does the conversion. These parallel symbols are transformed from frequency domain into time domain using IFFT module. These signals are converted into serial format and add a cyclic prefix to data frame before being transmitted.

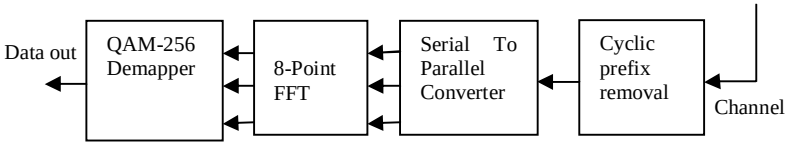

Fig 3: Block diagram of OFDM receiver

Fig 3 shows the basic block diagram for receiver module. There are five modules in the receiver block and initially the cyclic prefix has to be removed from the received signals. As the received data is in serial format, and since FFT requires input in parallel format, a module which converts serial data to parallel data is required. Output from FFT is converted back to serial format through parallel to serial converter. The conversion is required since the serial data need to be transmitted. Finally the serial output is demodulated using de-mapping module to get the transmitted data.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 6, June 2014

All these modules are designed using the verilog coding, once the code is ready and simulated using the Xilinx software or using synopsys verilog compiler simulator in ASIC. OFDM system results are synthesized and simulated using ASIC platform.Table1 shows the complete operation at every modules of transmitter and receiver of the OFDM system.

Modulating data	Mapper		IFFT		FFT		Demodulated data
	I-phase	Q-phase	Real (Re)	Imaginary (Im)	Re	Im	
00000000	-15	-15	-8	-15	-15	-15	00000000
00000001	-13	-15	-1	-357	-13	-15	00000001
00000010	-11	-15	-1	-1	-11	-15	00000010
00000011	-9	-15	-1	-355	-9	-15	00000011
00000100	-7	-15	-1	0	-7	-15	00000100
00000101	-5	-15	-1	355	-5	-15	00000101
00000110	-3	-15	-1	1	-3	-15	00000110
00000111	-1	-15	-1	357	-1	-15	00000111

Table 1: Simulated results of OFDM transceiver system results

LOW POWER TRANSCEIVER FOR OFDM

Now the all the OFDM module is synthesized and simulated and now we are applying various low power constraints to these codes we get area and power report. In our work we apply two low power constraints as worst case and best case. After that we apply clock gating low power technique to this design to reduce the power.
On applying “tcbn65lphvtbc_140” as technology library to OFDM module, properly synthesized and mapped to get the area and power report as given in below Table 2.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 6, June 2014

```
================================================
  Generated by:                 Encounter(R
  Generated on:                 May 12 2014
  Module:                       ofdm
  Technology library:           tcbn65lphvt
  Operating conditions:         BCCOM (bala
  Wireload mode:                segmented
  Area mode:                    timing libr
================================================

    Instance       Cells   Cell Area   Net
------------------------------------------------
ofdm                12528       70361
  m1                 7717       44978
    re4               249        1056
      mul_40_7        194         805
    re3               249        1056
      mul_40_7        194         805
    re2               247        1050
      mul_38_7        192         795
    re1               247        1050
      mul_38_7        192         795
    m45               171         818
      mul_38_7        142         566
    m42               171         818
      mul_38_7        142         566
    img4              206         814
      mul_40_7        151         563
    img3              206         814
      mul_40_7        151         563
    img2              198         802
      mul_38_7        142         550
    img1              198         802
      mul_38_7        142         550
    as2r              125         751
      sub_45_7         37         166
      add_41_7         19         151
    as2i              125         751
```

Table 2**:** Area report for applying 'tcbn65lphvtbc_140' technology library

Table 2 shows the area report of OFDM when applying "tcbn65lphvtbc_140" as technology library. It gives the cell area of OFDM as 70361 microns and consumes 12528 cells. Similarly on the same library we get power report as shown in table 3.

```
=======================================================
  Generated by:           Encounter(R) RTL Compiler RC1
  Generated on:           May 12 2014  06:12:22 pm
  Module:                 ofdm
  Technology library:     tcbn65lphvtbc 140
  Operating conditions:   BCCOM (balanced_tree)
  Wireload mode:          segmented
  Area mode:              timing library
=======================================================

                        Leakage    Dynamic      Total
  Instance    Cells Power(nW)  Power(nW)   Power(nW)
-------------------------------------------------------
ofdm          12528  1974.353 2725088.610 2727062.963
  m1           7717  1279.646 1815972.328 1817251.973
    re4         249    28.205   53519.135   53547.339
      mul_40_7  194    21.146   43556.928   43578.074
    re3         249    28.125   55220.247   55248.372
      mul_40_7  194    21.108   44667.080   44688.188
    re1         247    27.448   51476.534   51503.982
      mul_38_7  192    20.870   42653.638   42674.507
    re2         247    27.394   60604.730   60632.124
      mul_38_7  192    20.835   51249.538   51270.373
    m45         171    22.001    5822.455    5844.456
      mul_38_7  142    15.359       0.484      15.843
    m42         171    21.979    5207.566    5229.546
      mul_38_7  142    15.359       0.484      15.843
    img2        198    21.715   34173.226   34194.941
      mul_38_7  142    14.635   24711.974   24726.609
    img1        198    21.631   28975.968   28997.600
      mul_38_7  142    14.544   19960.272   19974.816
    img4        206    21.352   32119.269   32140.622
      mul_40_7  151    14.309   20532.058   20546.368
    img3        206    21.235   29974.207   29995.442
```

Table 3: Power report for applying 'tcbn65lphvtbc_140' technology library

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 6, June 2014

This report yields the total power consumption of OFDM module as 2727062.9(nw) of power with the loss of 1974.3(nw) of leakage power and 2725058(nw) of dynamic power. This is the worst case scenario where the above area and power reports show that the design consumes larger area and maximum power respectively. Therefore we apply one more low power constraint to OFDM module, the results of which are shown in Table 4 and Table 5.

```
=======================================
  Generated by:                Encounter(
  Generated on:                May 12 201
  Module:                      ofdm
  Technology library:          tcbn65lphv
  Operating conditions:        WCLCOM (ba
  Wireload mode:               segmented
  Area mode:                   timing lib
=======================================

    Instance       Cells   Cell Area   Ne
---------------------------------------
ofdm                12498       70254
  m1                 7689       44869
    re4               248        1056
      mul_40_7        193         805
    re3               248        1056
      mul_40_7        193         805
    re2               246        1049
      mul_38_7        191         794
    re1               246        1049
      mul_38_7        191         794
    m45               173         804
      mul_38_7        144         553
    m42               173         804
      mul_38_7        144         553
    img4              191         792
      mul_40_7        136         541
    img3              191         792
      mul_40_7        136         541
    img2              194         783
      mul_38_7        138         531
    img1              194         783
      mul_38_7        138         531
    as2r              125         751
      sub_45_7         37         166
      add_41_7         19         151
    as2i              125         751
```

Table 4: Area report for applying‘tcbn65lphvtwcl_140’ technology library

Here “tcbn65lpvtwcl_140” technology library were applied the area report is shown in table 4. In this case OFDM module consumes 70254 microns cell area and consumes 12498 cells.

```
=============================================================
  Generated by:            Encounter(R) RTL Compiler RC10
  Generated on:            May 12 2014  06:20:42 pm
  Module:                  ofdm
  Technology library:      tcbn65lphvtwcl 140
  Operating conditions:    WCLCOM (balanced_tree)
  Wireload mode:           segmented
  Area mode:               timing library
=============================================================

                      Leakage     Dynamic       Total
   Instance    Cells Power(nW)   Power(nW)    Power(nW)
-------------------------------------------------------------
ofdm           12498   231.611 1973677.895 1973909.506
  m1            7689   150.733 1231466.506 1231617.239
    re4          248     3.508   35357.800   35361.307
      mul_40_7   193     2.720   28757.483   28760.203
    re3          248     3.507   33760.380   33763.887
      mul_40_7   193     2.719   27608.188   27610.907
    re1          246     3.450   40190.280   40193.730
      mul_38_7   191     2.681   33558.116   33560.797
    re2          246     3.448   38191.215   38194.663
      mul_38_7   191     2.680   31449.521   31452.202
    img4         191     2.685   23846.947   23849.632
      mul_40_7   136     1.895   17225.509   17227.404
    img3         191     2.683   22831.568   22834.251
      mul_40_7   136     1.896   15659.528   15661.424
    m42          173     2.674    3605.642    3608.316
      mul_38_7   144     1.898       0.493       2.391
    m45          173     2.673    3578.901    3581.574
      mul_38_7   144     1.898       0.493       2.391
    img2         194     2.597   23471.535   23474.132
      mul_38_7   138     1.809   16568.550   16570.359
    img1         194     2.595   25083.245   25085.839
      mul_38_7   138     1.806   17673.150   17674.955
    as2r         125     2.543   38437.796   38440.339
      sub_45_7    37     0.622   12518.982   12519.604
      add_41_7    19     0.619   11548.932   11549.552
    as2i         125     2.543   23362.856   23365.399
      add_41_7    19     0.627    5429.640    5430.267
```

Table 5: Power report for applying ‘tcbn65lphvtwc_140’ technology library

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 6, June 2014

Table 5 shows the power report for applying 'tcbn65lphvtwc_140' technology library and it consumes 1973909.5(nw) total power with the loss of 19733677.8(nw) dynamic power and 231.6(nw) leakage power. By comparing the above constraints with results, "tcbn65lpvtwcl_140" is best case scenario because it consumes less power and less area as compared to "tcbn65lphvtbc_140" technology library.

From the above experiment, the following inference is obtained that "tcbn65lpvtwcl_140" is best case technology library but the power can still be reduced to higher extent by applying clock gating technique to this library then the following results in Table 6 and Table 7 will be obtained.

```
  Generated by:            Encounter(R) RTL Compi
  Generated on:            May 12 2014  06:28:48
  Module:                  ofdm
  Technology library:      tcbn65lphvtwcl 140
  Operating conditions:    WCLCOM (balanced_tree)
  Wireload mode:           segmented
  Area mode:               timing library
```

Instance	Cells	Cell Area	Net
ofdm	14972	75856	
m1	9352	48827	
re4	489	1966	
mul_40_7	194	805	
mul_38_7	194	805	
RC_OI_HIER_INST	19	41	
RC_OI_CTRL_INST	1	3	
RC_OI_HIER_INST12	19	41	
RC_OI_CTRL_INST	1	2	
RC_CG_HIER_INST98	1	6	
RC_CG_HIER_INST5	1	6	
re3	489	1966	
mul_40_7	194	805	
mul_38_7	194	805	
RC_OI_HIER_INST	19	41	
RC_OI_CTRL_INST	1	3	
RC_OI_HIER_INST12	19	41	
RC_OI_CTRL_INST	1	2	
RC_CG_HIER_INST97	1	6	
RC_CG_HIER_INST4	1	6	

Table 6: Area report after applying clock gating

After applying the clock gating to the best case library it yields the area report as shown in table 6 here it consume 75856 cell area in terms of microns, and consumes 14972 cells.

```
  Generated by:            Encounter(R) RTL Compiler RC10.1.304 -
  Generated on:            May 12 2014  06:29:19 pm
  Module:                  ofdm
  Technology library:      tcbn65lphvtwcl 140
  Operating conditions:    WCLCOM (balanced_tree)
  Wireload mode:           segmented
  Area mode:               timing library
```

Instance	Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
ofdm	14972	254.772	1600515.694	1600770.467
m1	9352	167.927	1043320.431	1043488.359
re3	489	6.505	16727.097	16733.601
mul_38_7	194	2.729	6194.458	6197.187
mul_40_7	194	2.729	6194.458	6197.187
RC_OI_HIER_INST12	19	0.095	0.518	0.613
RC_OI_CTRL_INST	1	0.005	0.020	0.025
RC_OI_HIER_INST	19	0.073	337.089	337.163
RC_OI_CTRL_INST	1	0.004	0.022	0.026
RC_CG_HIER_INST97	1	0.018	154.720	154.738
RC_CG_HIER_INST4	1	0.018	403.328	403.346
re4	489	6.503	16855.056	16861.559
mul_38_7	194	2.729	6194.458	6197.187
mul_40_7	194	2.729	6194.458	6197.187
RC_OI_HIER_INST12	19	0.095	0.518	0.613
RC_OI_CTRL_INST	1	0.005	0.020	0.025
RC_OI_HIER_INST	19	0.073	337.089	337.162
RC_OI_CTRL_INST	1	0.004	0.022	0.026
RC_CG_HIER_INST98	1	0.018	154.720	154.738
RC_CG_HIER_INST5	1	0.018	403.328	403.346
re1	293	5.321	4180.515	4185.836

Table 7: Power report after applying clock gating

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 6, June 2014

After applying the clock gating to the best case library it yields the power as 1600770.4(nw) of total power consumption and dynamic power as 1600515.6(nw). By comparing the best case scenario with the clock gating technique, it is seen that less power is utilized. However, it consumes more cell area and cells because in this technology extra AND gates are inserted into the OFDM modules to reduce the switching power consumption. Therefore, obliviously area will be relatively increased.

V. CONCLUSION

In this paper, the Low power transceiver for OFDM based WLAN system on ASIC platform is presented by using ample number of various low power libraries. It can be observed that comparing each library, the best case for implementation in real time can be selected. From the above experiment and results we conclude that clock gating reduces power consumption further. So power and area is always the traded-off between one another, depending on the requirement any one case can be selected for real time implementations.
Further, many more low power libraries are there to reduce the power, area, as well as timing to yields the better performance.

REFERENCES

[1] Shruti M. kallurwar, Assistant Prof. Rahila Patel, *"Reduction of ICI in OFDM Based WLAN System using Neural Network"*, International Journal of Advanced Research in Computer Science and Software Engineering (IJARCSSE), Volume 2, Issue 7, July 2012, pg no 356-360
[2] Preeti Mankar, L. P. Thakare, A. Y. Deshmukh, *" Design of Reconfigurable FFT for Wireless Communication Application"*, International Journal of Advanced Research in Computer Science and Software Engineering (IJARCSSE), Volume 4, Issue 4, April 2014, pg no 319-323.
[3] Aníbal luis intini, "Santa Barbara", Graduate Student Electrical and Computer Engineering Department, university of California aintini@engineering.ucsb.edu.
[4] Tipler P., Physics for Scientists and Engineers, 3rd Edition, Worth Publishers, pp.464-468, 1991.
[5] Rappaport, T.S *" Wireless Communications Principles and Practice"*, IEEE Press, New York, Prentice Hall, pp. 169-177, 1996
[6] Chethan Sharma *"Low power at different levels of VLSI design and clock distribution schemes"*,
[7] Michael B.Henry , *"Emerging power gating techniques for low power digital circuits"*
[8] Alfonso Troya and Koushik Maharatan, *"Low-Power VLSI Implementation of the Inner Receiver for OFDM-Based WLAN Systems"*,
[9] Massoud Pedram *"Digital Technologies for low power VLSI"* , Department of EE-Systems University of Southern California.