



# **Design of Positive Edge Triggered D Flip-Flop Using 32nm CMOS Technology**

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**ABSTRACT:** The usage of the low power consumptions devices in today's global village has become pervasive and indispensable in almost every walk of life. The thrust is towards reducing the high power energy consumption, required to reduce cost of the circuitry, while increasing the speed of performances in any operations. A high speed low power consumption positive edge triggered Delayed (D) flip-flop can be design for increasing the speed of counter in Phase locked loop, using 32 nm CMOS technology. Here we design D flip-flop for Phase locked loop (PLL). Phase locked loop is an important analog circuit used in various communication applications such as frequency synthesizer, radio computer, clock generation microprocessors etc. The design counter can be used in the divider chip of the phase locked loop. A divide counter is required in the feedback loop to increase the VCO frequency above the input reference frequency. The propose circuit will faster than conventional circuit as it will have fast reset operation. The circuit will consumes less power as it prevents short circuit power consumption. The circuit operates at low voltage power supply. The CMOS based fast D flip-flop circuit can be design and simulated by using Microwind 3.1 tool.

**KEYWORDS:** Phase Locked Loop (PLL), D flip-flop, Phase Frequency Detector (PFD) and Voltage Control Oscillator (VCO).

## **I. INTRODUCTION**

Phase locked loop (PLL) is an important analog circuit used in various communication applications such as frequency synthesizer, radio computer, clock generation microprocessors etc. Phase locked loop is a control system that generates an output signal whose phase is related to the phase of an input reference signal. For maintaining a well-defined phase and hence frequency relation between two independent signal sources, phase-locked loop can be used.

D flip-flop is an important part of the modern digital circuits. Phase locked loop with an excellent performance is widely studied in recent years. Frequency divider and PFD are indispensable modules of PLL, which uses D flip-flop as an integral part. Edge Triggered D flip flops are often implemented in integrated high speed operations using dynamic logic. This means that the digital output is stored on parasitic device capacitance while the device is not transitioning. This design of dynamic flip flops also enables simple resetting since the reset operation can be performed by simply discharging one or more internal nodes. The conventional D flip-flop has higher operating frequencies but it features static power dissipation. However this causes small increase in power dissipation, since at the frequencies of interest dynamic power consumption is dominant. In the proposed circuit dynamic power consumption was reduced by lowering internal switching and speeds is increased by shortening input to output path.

## **II. PHASE LOCKED LOOP (PLL)**

Phase locked loop is generally used in wireless communication and data recovery circuits. At present, for the above mentioned application a low voltage, low area and high performance integrated circuits are used which complicates the execution of such type of integrated circuit.

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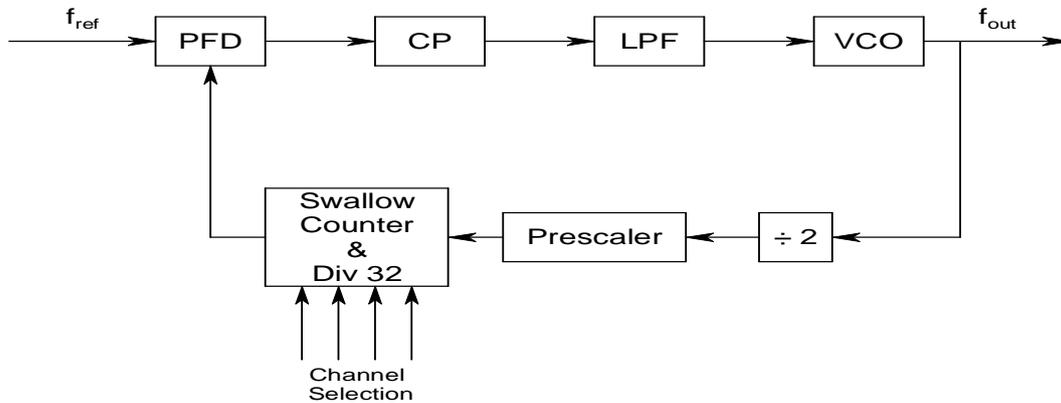


Fig.1 Block diagram of PLL

A PLL is a control system that generates a signal that has a fixed relation to the stage of a "reference" signal. A phase-locked loop circuit responds to both the frequency and the phase of the input signals, automatically raising or lowering the frequency of a controlled oscillator until it is coupled to the character in both frequency and phase. Phase locked loops are built of a detector, charge pump, low pass filter, voltage-controlled oscillator (VCO) and frequency divider placed in a negative feedback closed-loop configuration. A phase detector compares two input signals and produces an error signal which is proportional to their phase difference. The error signal is then low-pass filtered and used to drive a voltage-controlled oscillator (VCO) which creates an output frequency. The output frequency is fed through a frequency divider back to the input of the system, creating a negative feedback loop. If the output frequency drifts, the error signal will increase, driving the VCO frequency in the opposite direction so as to reduce the error. Thus the output is locked to the frequency of the other input.

## A. Phase Frequency Detector

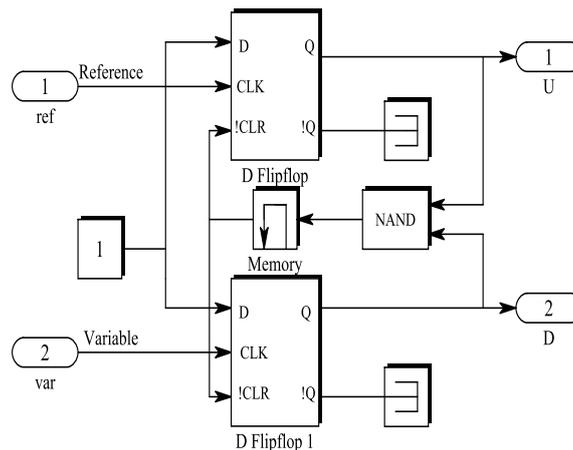


Fig. 2 Block diagram of PFD

A phase frequency detector (PFD), is a device which compares the phase of two input signals and provides a signal in the form of phase error. It accepts two inputs which correspond to two different input signals, usually one from a voltage-controlled oscillator (VCO) and the other is a reference source. It has two outputs which instruct subsequent circuitry on how to adjust to lock onto the phase. A charge pump circuit is used to convert the digital signal from the phase frequency detector to an analog signal, the output of which is used to control the frequency of the voltage control oscillator. To form a phase-locked loop (PLL), the phase error output of PFD is fed to a charge pump



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(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 4, April 2015

and then to loop filter which integrates the signal to get a sharper and smoother signal so that the disturbances at the input of VCO get minimized. As can be ascertained from the following diagram, the D flip-flop is an integral part of pfd. Hence, to make the operation of PFD faster, a fast D flip-flop is required.

## B. Frequency Divider

Frequency divider divides the VCO frequency to generate a frequency which is compared with reference frequency. In the block diagram PLL, the prescaler and swallow counter together acts as a frequency divider. D flip flop is an integral part of both of them.

## C. Voltage Controlled Oscillator

A voltage-controlled oscillator or VCO is an electronic oscillator whose oscillation frequency is controlled by a voltage input. The applied input voltage determines the instantaneous oscillation frequency. Consequently, modulating signals applied to control input may cause frequency modulation (FM) or phase modulation (PM). A VCO may also be part of a phase-locked loop.

## D. Low Pass Filter

A low-pass filter is a filter that passes low-frequency signal. Attenuates signals with frequencies higher than the cutoff frequency. The actual amount of attenuation for each frequency varies depending on specific filter design. It is sometimes called a high-cut filter, or treble cut filter in audio applications. A low-pass filter is the opposite of a high-pass filter. A band-pass filter is a combination of a low-pass and a high-pass.

Low-pass filters exist in many different forms, including electronic circuits, anti-aliasing filters for conditioning signals prior to the analog-to-digital conversion, digital filters for smoothing sets of data. Also for acoustic barriers, blurring of images, and so forth. The moving average operation used in areas such as finance is a particular kind of low-pass filter, and can be analyzed with the same signal processing techniques as are used for other low-pass filters. Low-pass filters provide a smoother form of a signal, removing the short-term fluctuations, and leaving the long-term trend. An optical filter can correctly be called a low-pass filter, but is conventionally called a long pass filter (low frequency is long wavelength), to avoid confusion.

### III. RELATED WORK

A high speed low power consumption positive edge triggered Delayed (D) flip-flop was designed for increasing the speed of counter in Phase locked loop, using 180 nm CMOS technology. This circuit operates at 1.8v power supply in CADENCE spectra, it uses 12 transistors. The designed counter has been used in the divider chip of the phase locked loop [1]. A high-speed low-power CMOS D-type master-slave flip-flop is proposed and adopted in the PFD. Higher speed and lower power operation are attributed to the reduced node capacitance. Charge-sharing phenomena are circumvented in the proposed PFD. The proposed PFD shows improvement in frequency sensitivity at high operating frequency. The proposed PFD is suitable for high-speed low-power operation. This circuit is designed using 0.5 $\mu$ m CMOS technology at 5V supply voltage [2]. In this paper S. H. Yang design a new dynamic D flip-flop for high speed operation and low power consumption is presented aiming at glitch free operation. The flip-flop consists of only nine transistors based on the transistor merging technique, which is smaller than other alternatives. The fewer transistors in the flip-flop can achieve faster operation and lower power consumption. To evaluate the proposed flip-flop circuit, a dual-modulus divide by 128/129 prescaler has been designed and fabricated using 0.25 $\mu$ m CMOS technology. At the 2.5V supply voltage, the prescaler using the proposed dynamic D flip-flop can operate up to the frequency of 2.9GHz consuming 3.621mW and shows half the power delay product of Huang's circuits [3]. Won Hyo Lee and Jun Dong Cho introduce a high-speed and low power Phase-Frequency Detector (PFD) that is designed using modified TSPC (True Single-phase Clock) positive edge triggered D flip-flop. This PFD has a simpler structure with using only 19 transistors. The operation range of this PFD is over 1.2GHz without additional prescaler circuits. Furthermore, the PFD has a dead zone less than 0.0lns in the phase characteristics and has low phase sensitivity errors [4]. Design and performance analysis of D flip-flop using 32nm technology for high speed and low power application. The newly designed high speed and low-power flip-flop can be used for any digital application. They compare the two different flip flop circuits contain 10 transistors and 12 transistors [5]. Low-power high-speed programmable dual modulus divider architecture is presented by Mohd S. Sulaiman and Nasserullah khan. The circuit's three building blocks: prescaler, 2- and 5-bit programmable dividers; were designed using high-performance single-phase clocking latch up

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(An ISO 3297: 2007 Certified Organization)

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circuits rather than the conventional latch up circuits widely used in digital systems. They have presented a dual-modulus divider with extremely low power consumption, designed in a 0.18 $\mu$ m CMOS process. The maximum operating frequency is 2.4 GHz with a 1.8-V supply and a power of only 2.26 mW [6].

## IV. DESIGN METHODOLOGY

Designing steps of D Flip-Flop using CMOS technology are

**Step 1:-** Design a conventional D Flip-Flop using 32 nm CMOS technologies.

**Step 2:-** Design a proposed D Flip-Flop using 32 nm CMOS technologies.

**Step 3:-** Simulation & Analysis of proposed design.

Every step of design follows the design flow of Microwind 3.1 software as mentioned in fig 4.1. The design methodology will be according to VLSI backend design flow. The main target is to design and analyze the D Flip Flop. To achieve the proposed target following steps are included in the design and analysis of proposed D Flip Flop for Phase Locked Loop (PLL).

- Schematic design of proposed D Flip Flop using CMOS transistors (BSIM4).
- Performance verification of the above for different parameters.
- CMOS layout for the proposed different D Flip Flop using VLSI backend.
- Verification of CMOS layout and parameter testing.
- If the goal is achieved for all proposed parameter including detail verification, sign off for the design analysis and design will be ready for IC making.
- If detail verification of parameters would not completed then again follow the first step with different methodology.

For performing this project the different methodology and techniques can be used for research. The MICROWIND3.1 programs allow to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. MICROWIND 3.1 includes all the commands for a mask editor as well as original tools never gathered before in a single module (2D and 3D process view, VERILOG compiler, tutorial on MOS devices). We can gain access to circuit simulation by pressing one single key. The electric extraction of circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

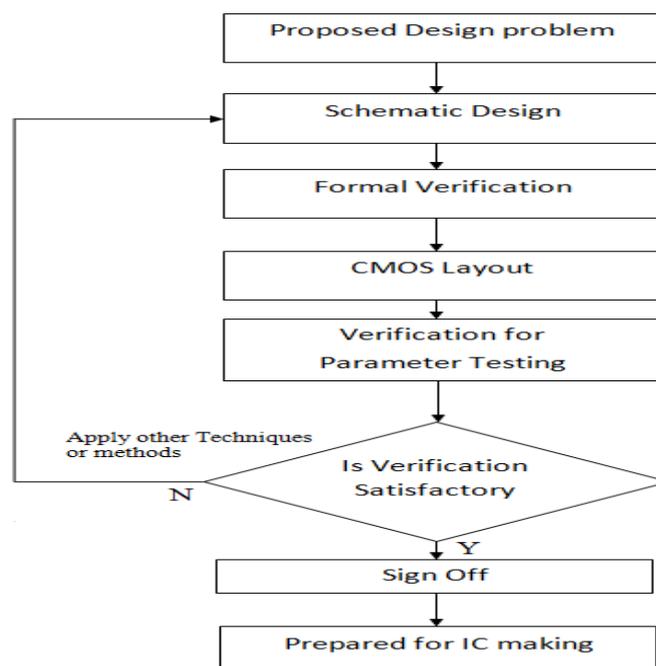


Fig. 4 Design Flow Chart

# International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 4, April 2015

## V. DESIGN IMPLEMENTATION

Here we design D flip-flop in which first we design conventional D flip-flop and then proposed D flip-flop. The proposed research is aimed to achieve the reduced area; low power consumption and high stability for D flip flop which is used in phase locked loop (PLL). All this design D flip-flop is implemented by using 32nm CMOS technology.

### 5.1: DESIGN OF CONVENTIONAL D FLIP-FLOP USING 32nm CMOS TECHNOLOGY

D flip-flop is an important part of modern digital circuits. The conventional D flip-flop is design here by using 32nm CMOS technology in microwind 3.1 software. This design D flip-flop is used in phase locked loop. Circuit schematic of conventional D flip-flop is as shown in figure 5.1.

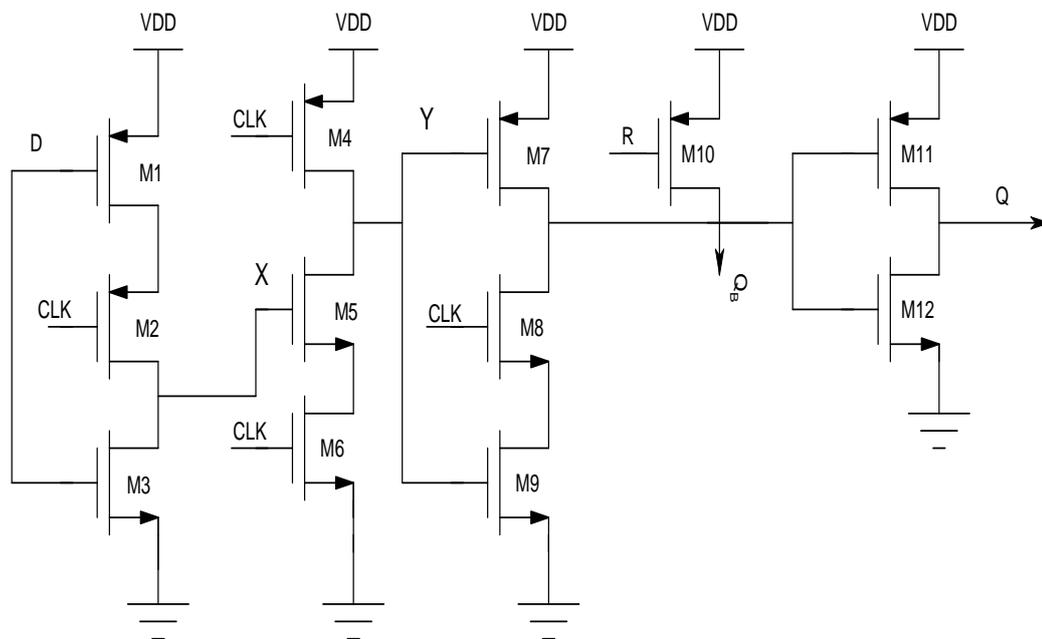


Fig. 5.1 Structure of conventional D flip-flop

Fig. 5.1 shows the design of a specialized single  $\phi$ -phase edge triggered register. When  $clk=0$ , the input inverter is sampling the inverted D input on node X. The second (dynamic) inverter is in precharge mode, with M4 charging up node Y to VDD. The third inverter is in the hold mode, since M7 and M8 are off. Therefore during the low phase of the clock, the input of the final inverter holding its previous value and the output Q is stable. On the rising edge of the  $clk$ , the dynamic inverter M4-M6 evaluates. If X is high on the rising edge, node Y discharges. The third inverter M8-M9 is on during the high phase and the node value of Y is passed to the output Q. On the positive phase of clock, note that node X transitions to a low if the D input transition to a high level. Therefore the input must kept stable till the value on node X before the rising edge of the clock propagates to Y. This represents the hold time of register. transistor sizing is critical for achieving correct functionalities. The glitch problem can be corrected by resizing the pull down paths through M5-M6 and M8-M9. This design of dynamic flip flop also enable simple resetting M10 since the reset operation can be performed by simple discharging one or two internal nodes.

Figure 5.2 shows the layout design of conventional D flip-flop using 32nm CMOS technology. This layout uses a power supply less than 1.20 volt dc. This layout is done using professional software Microwind. The layout has area  $7.5\mu m^2$ , which is small enough. Parasitic extraction and post simulation is performed successfully. This conventional D flip-flop contains 12 transistors.

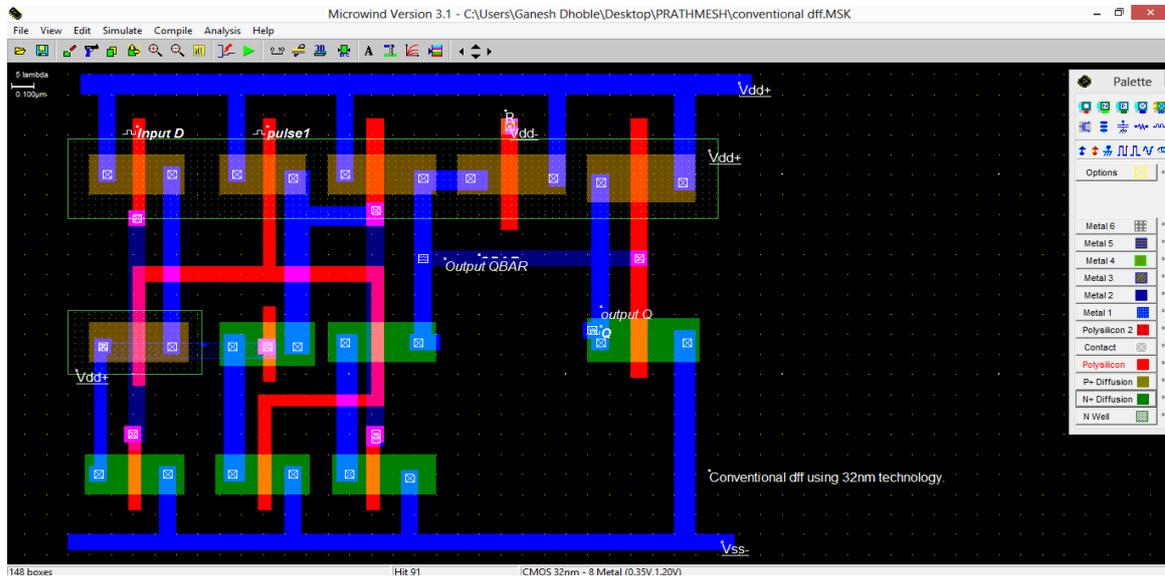


Fig. 5.2 Layout of Conventional D flip-flop

## 5.2: DESIGN OF PROPOSED D FLIP-FLOP USING 32nm CMOS TECHNOLOGY

The positive edge triggered proposed D flip-flop is to be design here. D flip-flop is an important part of modern digital circuits. The proposed D flip-flop is design here by using 32nm CMOS technology in microwind 3.1 software. This design D flip-flop is used in phase locked loop. Circuit schematic of conventional D flip-flop is as shown in figure 5.3.

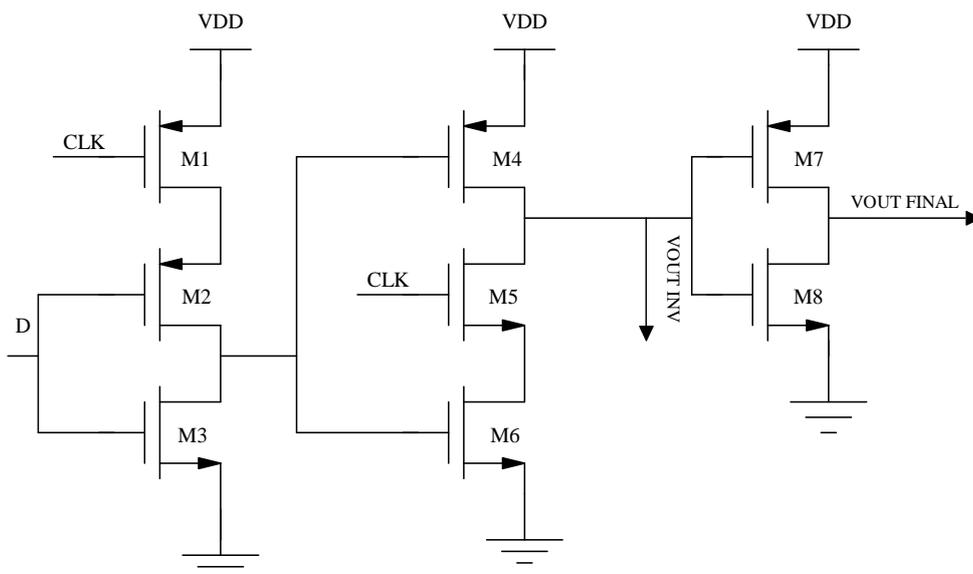


Fig. 5.3 Structure of proposed D flip-flop

The layout of proposed D flip-flop circuit shown in Figure 5.4 is done using professional software Microwind 3.1. The layout has area  $3.0\mu\text{m}^2$ , which is fairly small as compared to other power amplifiers. Parasitic extraction and Post simulation is performed successfully. Here only 8 transistors are used to proposed D flip-flop.

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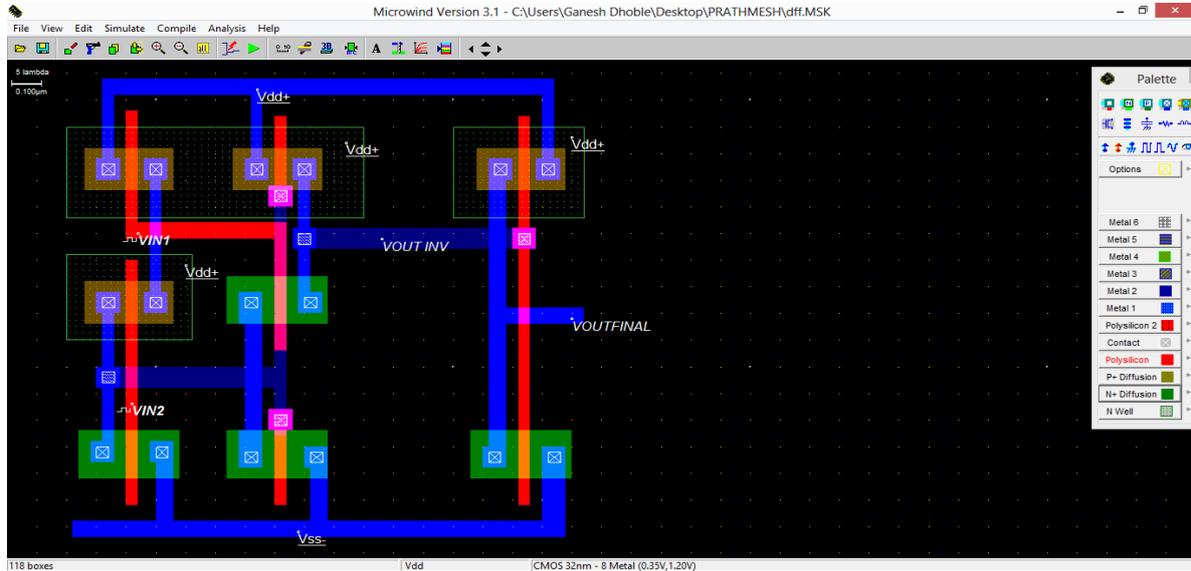


Fig. 5.4 Layout of Proposed D flip-flop

## VI. RESULT

### 6.1: SIMULATED RESULT OF CONVENTIONAL D FLIP-FLOP USING 32nm CMOS TECHNOLOGY

The simulated output waveform of conventional D flip-flop for voltage vs. time is shown in Fig.6.1. Simulations at the schematic level were performed using Microwind tool. Power consumption can be calculated from DC simulations. Simulated output voltage wave forms of differential time scale shown in figure 6.1. Here in the given output result pulse1 is to be a clock signal. The time scale should be a 500p and it can be vary. Q & QBAR output are always inverse to each other. When D is 1 also pulse is at high the output Q is also 1 and QBAR is reverse.

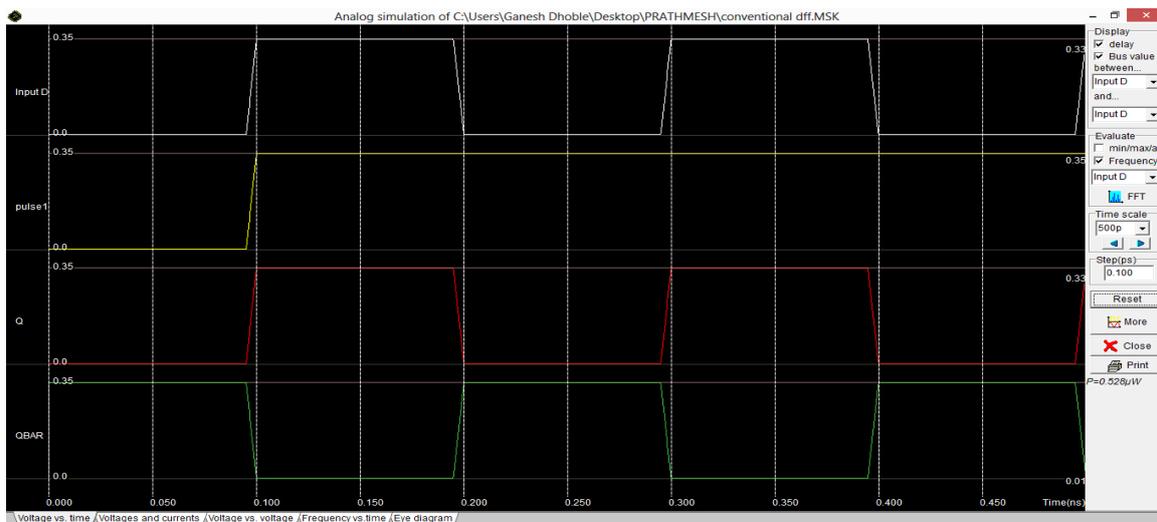


Fig 6.1 Simulated output waveform of voltage verses time

Stimulated output waveform of conventional D flip-flop for voltage and current with differential output voltage as shown in Fig 6.2. Result obtain from simulation was  $I_{ddmax} = 0.007mA$  and current for N1 was  $0.004mA$  with Vdd supply of 1.20V. It is evidence that current depends on the input clock of D flip-flop.

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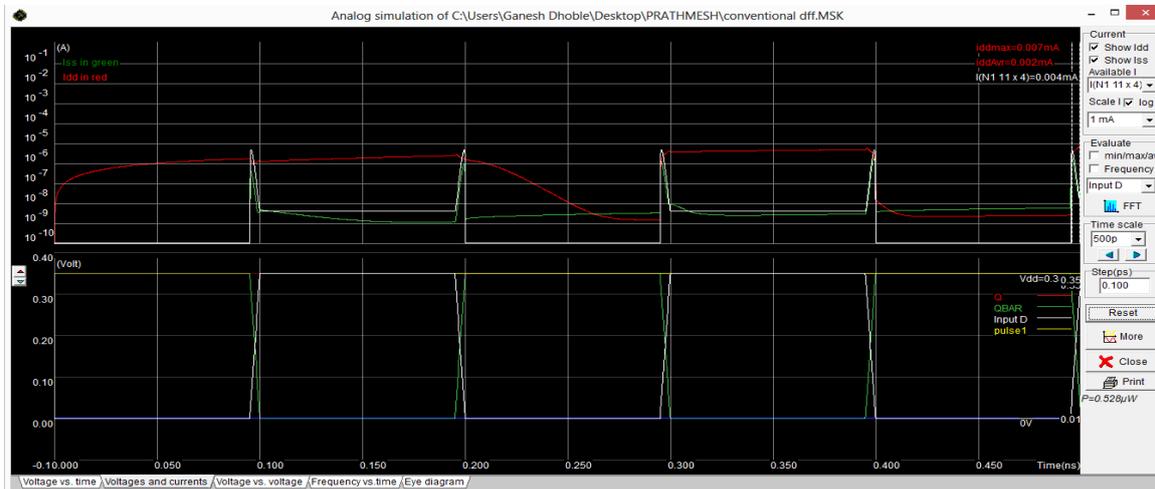


Fig 6.2 Simulated output waveform of voltage and current

## 6.2: SIMULATED RESULT OF PROPOSED D FLIP-FLOP USING 32nm CMOS TECHNOLOGY

The simulated output waveform of proposed D flip-flop for voltage vs. time is shown in Fig. 6.3. Simulations at the schematic level were performed using Microwind 3.1 tool. Power consumption can be calculated from DC simulations. Simulated output voltage wave forms of differential time scale shown in figure 6.3. Here time scale is to be 2n and it can be vary. VOUT INV & VOUTFINAL are always inverses to each other. VOUTFINAL gives time delay it is to be 20ps-21ps. VIN2 is to be a clocked signal.

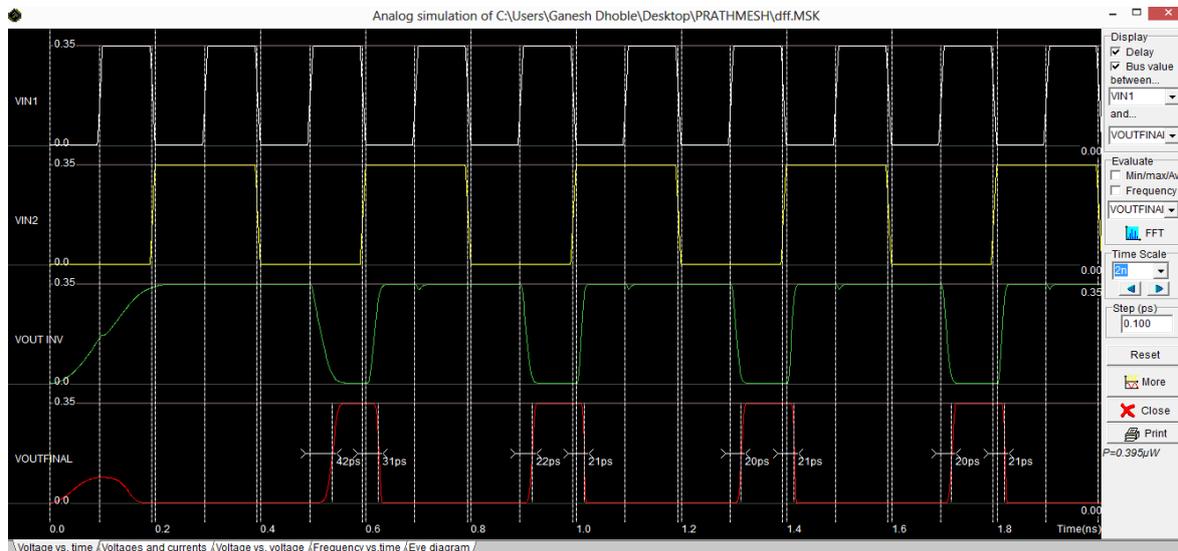


Fig 6.3 Simulated output waveform of voltage verses time

Stimulated output waveform of proposed D flip-flop for voltage and current verses time with differential output voltage as shown in Fig 6.4. Result obtain from simulation was Iddmax =0.010mA and current for N1 was 0.0016mA with Vdd supply of 1.20V. It is evidence that current depends on the input clock of D flip-flop.

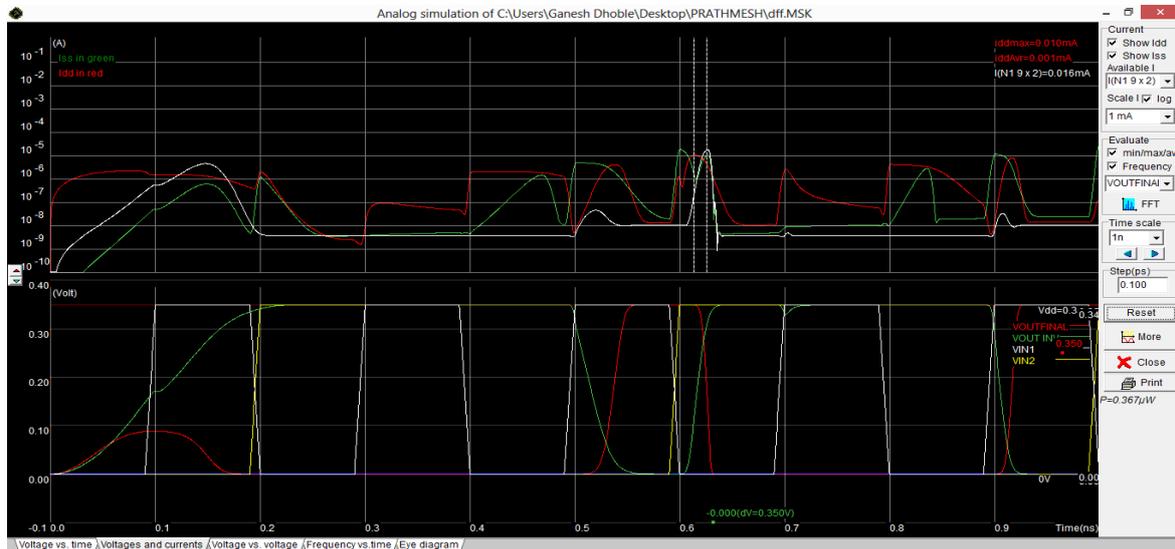


Fig 6.4 Simulated output waveform of voltage and current

## VII. CONCLUSION AND FUTURE WORK

Many researchers have designed D flip-flop for phase locked loop (PLL) by applying different techniques. In the world today VLSI/CMOS is in very much in demand, from the careful study of reported work it is observed that very few researchers have taken a work for designing PLL with CMOS/VLSI technology.

Researchers have undertaken different designs processes or phenomena with regard to optimize the performance of D flip-flop. Following table shows the parameters of proposed D flip-flop.

| Sr. No. | Parameter                   | 2012                 | 2014               |
|---------|-----------------------------|----------------------|--------------------|
| 1       | Technology used             | 180nm                | 32nm               |
| 2       | VDD/Vout (V)                | 1.80V                | 1.20V              |
| 3       | No. of NMOS transistor used | 6                    | 4                  |
| 6       | No. of PMOS transistor used | 6                    | 4                  |
| 7       | Power consumption           | 16.49µW              | 0.367µW            |
| 8       | Temperature                 | Not specified        | 27°C               |
| 9       | Surface area                | 55.22µm <sup>2</sup> | 3.0µm <sup>2</sup> |

Table 7.1: Parametric summary of D flip-flop design

From the optimized parameters of the Table 7.1, it is concluded; all the output of proposed D flip-flop is found stable which proved the high stability of the D flip-flop. Also from the parametric analysis of design tool, the power dissipation measured by  $V_{DD}$  at 1.20Volt is found only 0.367µW, which shows that power consumption is very low. Also the optimum, high efficient chip design of D flip-flop using 32nm CMOS technology. In this way very high efficient, low power, optimum area chip is designed for low power D flip-flop.

The number of applications of integrated circuits in telecommunications and consumer electronics has been rising steadily. For future work, phase locked loop is the most important part of integrated circuit used in electronics and for the building of the important part of electronic circuit D flip-flop is the most useful part. Here conventional D flip-flop is used in phase locked loop which can be replaced by proposed D flip-flop. Then there is a reduction in power



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consumption. This is most beneficial in Bluetooth application for transceiver. As the new technology comes (i.e.4G, 5G...), the frequency range of proposed D flip-flop in phase locked loop will be subjected to change as per the requirement. As the process technology has rapidly shrunk from 180nm to 45nm and attempt to reduce further i.e.32nm. So the proposed D flip-flop in phase locked loop can also be implemented as per the requirement of new process technology for getting low power.

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