



Design of Two Stage Ultra Low Power CMOS Operational Transconductance Amplifier (OTA) Using 180 nm Technology

Soumen Pal¹, Puspak Pain²

Assistant Professor, Dept. of ECE, Narula Institute of Technology, MAKAUT WB, Kolkata, India¹

Assistant Professor, Dept. of ECE, Narula Institute of Technology, MAKAUT WB, Kolkata, India²

ABSTRACT: This paper deals with well-defined design criteria for ultra low power two stage CMOS operational transconductance amplifiers (OTAs) with simple yet robust implementation in nm dimension. A simple design approach which allows electrical parameters to be univocally related to each circuit element and biasing values for low frequency applications is presented. The operational transconductance amplifier with $\pm 1.8\text{V}$ power supply has been simulated using TANNER Tools ver.13 with $0.18\mu\text{m}$ CMOS technology which provide expected characteristics with convenient performance for given specification.

KEYWORDS: CMOS, OTA, ultra low power, 180 nm design.

I. INTRODUCTION

Operational Transconductance Amplifier (OTA) is a fundamental building block of analog circuits and systems being used in a vast array of consumer, industrial, and scientific portable monitoring systems such as data converters, four-quadrant multipliers, mixers, modulators and continuous-time filters. Unbuffered operational amplifiers (voltage controlled current sources) are direct couple high differential gain amplifier with typically very high output resistance (65.68k for externally connected 100k load resistance). Designing high performance analog integrated circuits in low power applications with reduced channel length devices is becoming increasingly exigent with the relentless trend toward reduced supply voltages. A large part of the success of the MOS transistor is due to the fact that it can be scaled to increasingly smaller dimensions, which results in higher performance. On the other hand for different aspect ratio, there is a trade-off among speed, power, gain and other performance parameters. Thus realization of a CMOS OTA that combines a high linearity, considerable dc gain with high unity gain frequency tends to be a constraint in circuits and systems design task. There have been several circuit approaches to evade this quandary. In designing a low power OTA, several electrical characteristics, such as supply voltages, dc gain, load capacitance, unity gain frequency, phase margin, slew rate, input common mode range, output swing all have to be taken into consideration [1,2,5].

The implementation of high performance signal processing and conditioning block is one of the most significant tasks in real-time system designing. Operational amplifiers are essential components for simple amplification of weak signals in addition to complex audio and video processing applications in mixed-signal domain. In the basic differential amplifier section, p-mos and n-mos transistors in μm range worked as driver and load respectively. The performance CMOS OTA has been optimized with 10pF capacitive load which can provide gain 47.86dB and power dissipation 1.3mw [3].

The main aim of this work is to design two stage CMOS OTA using 180nm technology able to be operated with negative feedback connection for that phase and frequency compensation is necessary to achieve closed loop stability. The proposed OTA satisfy all the required electrical specifications that combines good compensation strategy and design technique which is able to achieve high open loop gain 54.03 dB with low power consumption $9\mu\text{W}$, high CMRR up to 46.55 dB and PSRR up to 56.47 dB at 1.8 V supply.



International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 2, February 2016

II. THEORY OF TWO STAGE OP-AMP

The CMOS OTA can be designed by using either two stage or folded cascade topology with modifying any section of the basic op-amp configuration. The selection of the topology is based on the required non functional parameters and features of op-amp. The basic CMOS two stage OTA is divided into four subsection of circuit: Differential gain stage, second gain stage, compensation circuitry and bias string [2,3,5].

Differential gain stage:

The first subsection concern is the differential gain stage which consists of transistors M1, M2, M3 and M4. The gate of M1 is the inverting input and the gate of M2 is the non-inverting input jointly forms the basic driver stage of the amplifier. The transconductance of this stage is simply the transconductance of M1 or M2. M3 and M4 are the active load transistors of the differential amplifier. The current mirror active load used in this circuit has distinct advantage; the use of active load devices creates a large output resistance in relatively small amount of die area [2].

Second gain stage:

The second stage is a current sink load inverter. The purpose of the second gain stage (M6 and M7) is to provide additional gain in the amplifier. This stage takes the output from the drain of M4 and amplifies through M6 which is in the standard common source configuration with a current sink load M7 [1,2].

Compensation circuitry:

The high gain CMOS op-amp is generally used in negative feedback configuration to obtain a very accurate transfer function where the closed loop gain is almost independent of open loop gain and depends on feedback elements only. In negative feedback amplifier frequency and phase compensation is necessary which is achieved by a miller compensation capacitance connected in between first and second stage. The compensation of the two stage CMOS amplifier has been carried out internally using a pole splitting capacitor (C_c) to achieve a desirable phase margin[4,5].

Bias string:

The biasing of the operation amplifier is achieved with a current mirror circuit consisting of M5 and M8 along with a current source I_{ref} . MOS Transistor M5 and M7 sink a certain amount of current based on their gate voltage which is driven by the drain voltage of M8[3].

III. DESIGN APPROACH OF TWO STAGE CMOS OTA

A design technique for two stage CMOS OTA (Fig.1) can be constructed as follows [4,5,6]. The currents through the transistors M3 and M4 are equal as they form a current mirror so I_3 and I_4 are equal. Again the transistors M1 and M3 are in series, hence, they carry same current i.e. $I_1 = I_3$. Again for identical biasing of two differential input transistors we can write

$$I_1 = I_2 = I_3 / 2 \quad (1)$$

$$\text{Now } C_c \text{ can be calculated as, } C_c = 0.2 \times C_L \quad (2)$$

$$\text{And } I_5 = SR \times C_c \quad (3)$$

Transconductance of transistor M1 and M2 are equal and can be calculated as

$$g_{m1} = GBW \times C_c \quad (4)$$

$$\text{And } g_{m1} = \sqrt{2\mu_n C_{ox} (W/L)_1 I_1} \quad (5)$$

So $(W/L)_1$ and $(W/L)_2$ can be calculated from the equation (4) and (5).

The transistor M3 is always saturated as its drain and gate are connected together. The transistor M3 and M4 have the same source voltage, gate voltage and drain current. As M3 and M4 constitute a current mirror configuration so M4 will also saturated and $(W/L)_3$ is equal to $(W/L)_4$. $(W/L)_3$ can be calculated as

$$(W/L)_3 = \frac{I_5}{\mu_n C_{ox} \left[V_{DD} - V_{in(max)} - |V_{th,p}(max) + V_{th,n}(min)| \right]^2} \quad (6)$$

Transistor M5 and M8 are used for biasing which form a current mirror circuit. So aspect ratio of NMOS M5 and M8 are equal. They can be calculated as follows

$$V_{DS5(sat)} = V_{in(min)} - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{th,n} \quad (7)$$

$$(W/L)_5 = \frac{2I_5}{\mu_n C_{ox} [V_{DS5(sat)}]^2} \quad (8)$$

Assume that,



International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 2, February 2016

$$g_{m6} \geq 10g_{m1} \quad (9)$$

Aspect ratio of Transistor M6 and M7 are

$$(W/L)_6 = \frac{(W/L)_4 g_{m6}}{g_{m4}} \quad (10)$$

$$(W/L)_7 = \frac{(W/L)_5 I_6}{I_5} \quad (11)$$

Where,

C_c = Compensation capacitor.

SR = Slew rate of the op-amp.

C_L = Load capacitance of the op-amp.

I_i = Drain current of i-th transistor in Fig.1.

μ_p = Mobility of PMOS.

μ_n = Mobility of NMOS.

GBW = Unity Gain Bandwidth product

g_{mi} = Transconductance of i-th transistor

C_{ox} = Oxide capacitance per unit area.

V_{SS} = Negative supply voltage.

V_{DD} = Positive supply voltage.

$V_{in(max)}$ = Maximum common mode input.

$V_{in(min)}$ = Minimum common mode input.

$(W/L)_i$ = Aspect ratio of i-th transistor.

$$\beta_1 = \mu_n C_{ox} (W/L)_1$$

IV. DESIGN SPECIFICATIONS OF TWO STAGE CMOS OTA

The following Table 1 represents specifications and Table 2 represents process parameters for the CMOS OTA which has been designed as shown in Fig.1 and the design parameters can be determined as given in Table 3.using the design procedure as described in section 3.

Table 1. Electrical Specifications of CMOS OTA

Electrical Parameters	Values
Supply voltage (V)	± 1.8
Load Capacitance (pF)	1
Output Resistance(k Ω)	65.68
Bias current (μ A)	1.3
Open Loop Gain (dB)	54.03
Open loop Unity gain frequency (MHz)	7.93
Closed loop Unity gain bandwidth(MHz)	15
Phase Margin (degree)	-150.03
Slew rate (volt/ μ sec)	6.5
Input Common mode range (volt)	-0.27 to +1.5
Output swing (volt)	-0.25 to +1.78
CMRR (dB)	46.55
PSRR (dB)	56.47
Power Dissipation (μ Watt)	9

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 2, February 2016

Table 2.Process Parameters

Parameters	NMOS	PMOS
Gate Oxide thickness	2.5 nm	2.6nm
Threshold voltage	237mV	-320mV
Mobility	0.113 m ² /Volt-Sec	0.012 m ² /Volt-Sec

Table 3.Design parameters of CMOS OTA as shown in Fig.1

Parameters (Unit)	Values
C _c (fF)	200
(W/L) _{1,2} (nm/ nm)	1800/180
(W/L) _{3,4} (nm/ nm)	180/180
(W/L) _{5,8} (nm/ nm)	180/540
(W/L) ₆ (nm/ nm)	2232/540
(W/L) ₇ (nm/ nm)	540/180

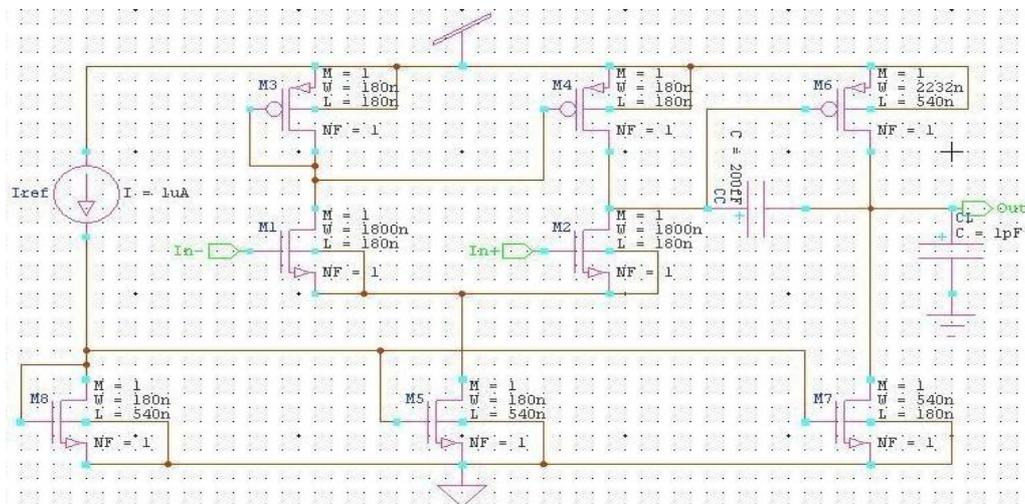


Fig. 1 Schematic diagram of designed operational transconductance amplifier (OTA) using 0.18μm CMOS technology.

V. SIMULATION RESULTS

For the electrical specifications (Table.1), the process parameters (Table.2) and with the help of the design techniques as mentioned in Section.3, the design parameters of CMOS OTA (Table.3) has been calculated and a two stage CMOS OTA (Fig.1) has been designed and simulated using TANNER TOOL version-13. The T-SPICE simulation results are discussed as follows

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 2, February 2016

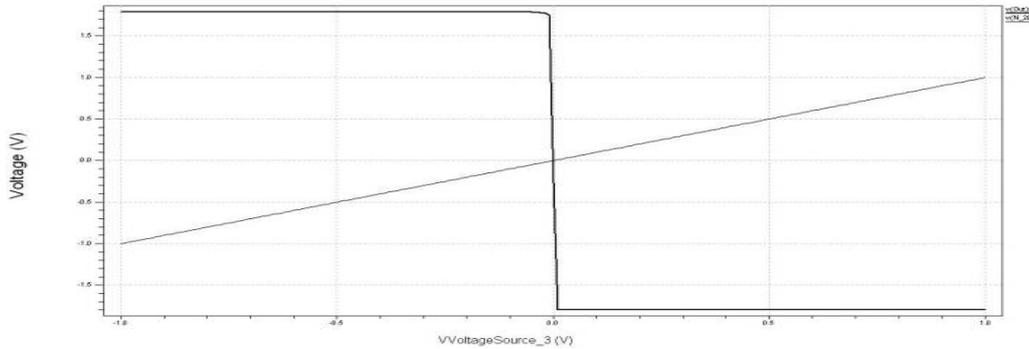


Fig. 2 Voltage transfer characteristic of designed OTA in inverting mode.

In Fig.2 it has been shown that output will change from $+V_{sat}(+1.8V)$ to $-V_{sat}(-1.8V)$ when a variable DC voltage (-1v to +1v) is applied in inverting terminal and non- inverting terminal is connected to ground.

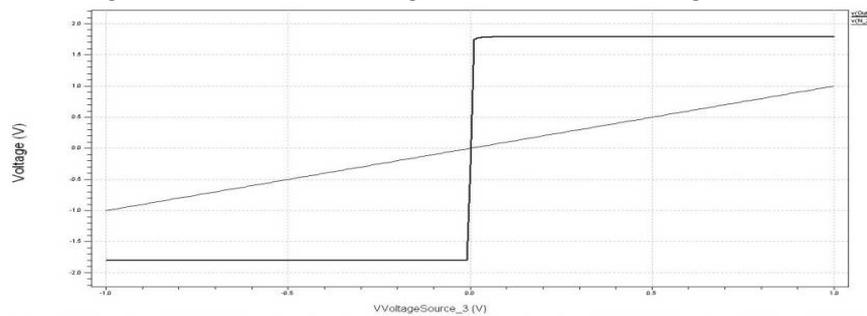


Fig. 3 Voltage transfer characteristic of designed OTA in non-inverting mode.

In Fig.3 it has been shown that output will change from $-V_{sat}(-1.8V)$ to $+V_{sat}(+1.8V)$ when a variable DC voltage (-1v to +1v) is applied in non- inverting terminal and inverting terminal is connected to ground.

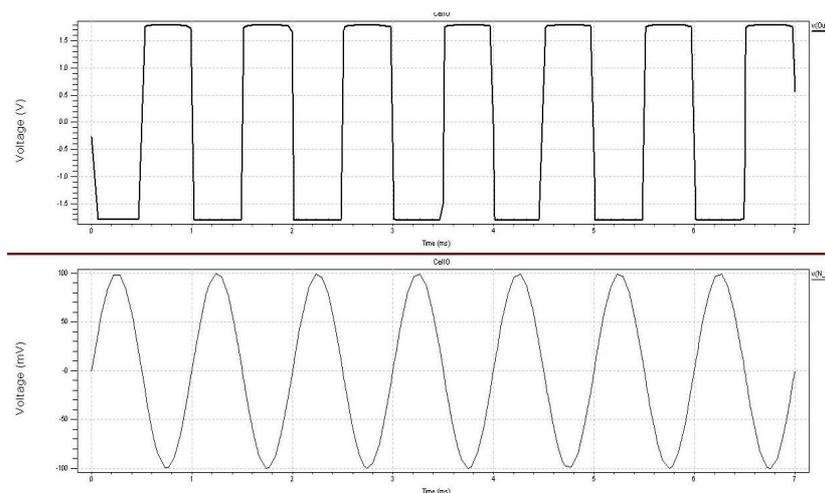


Fig. 4 Transient response of designed OTA in inverting mode.

Fig. 4 shows the transient analysis when a sinusoidal voltage of 100mV amplitude is applied in inverting input terminal for open loop configuration. The simulated result shows the output is switching in between $-V_{sat}(-1.8V)$ and $+V_{sat}(+1.8V)$ in opposite phase with input.

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 2, February 2016

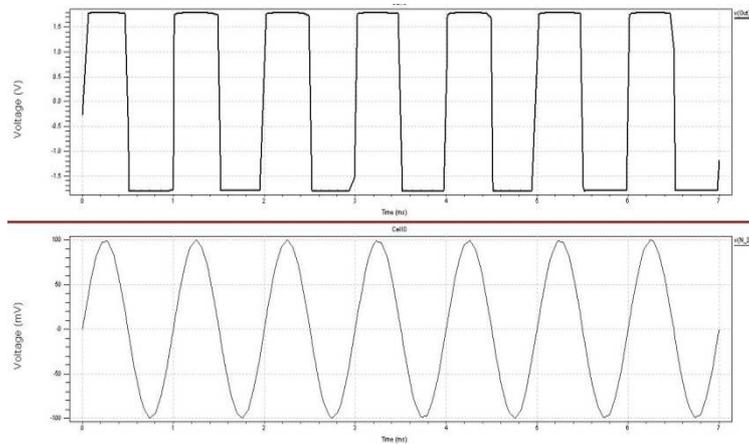


Fig. 5 Transient response of designed OTA in non-inverting mode.

Fig. 5 shows the transient analysis when a sinusoidal voltage of 100mV amplitude is applied in non-inverting input terminal for open loop configuration. The simulated result shows the output is switching in between +Vsat(+1.8V) and -Vsat(-1.8V) in same phase with input.

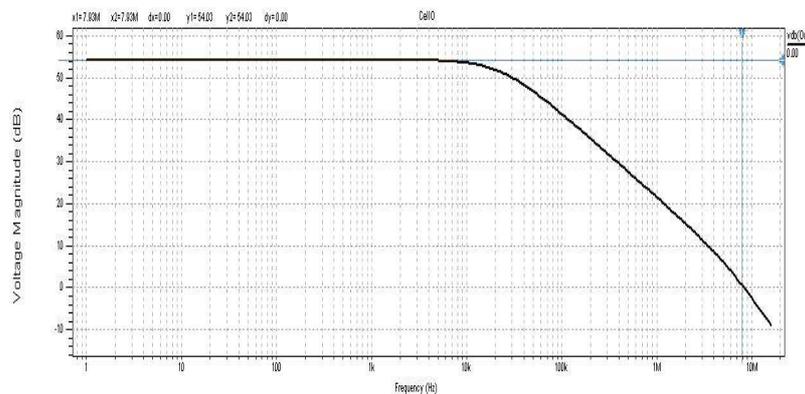


Fig. 6 Magnitude response in open loop configuration

Fig. 6 shows the Magnitude Vs frequency plot for open loop configuration. It shows open loop gain is 54.03dB and unity gain frequency is 7.93MHz.

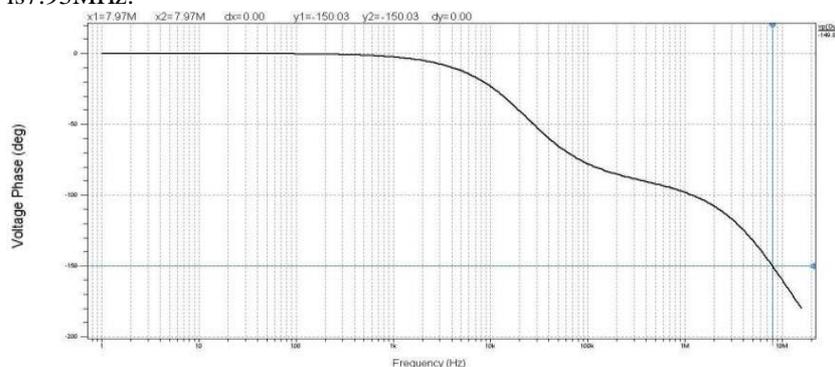


Fig.7 Phase response in open loop configuration.

Fig. 7 shows phase vs. frequency plot for open loop configuration with phase Margin -150.03 degrees.

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 2, February 2016

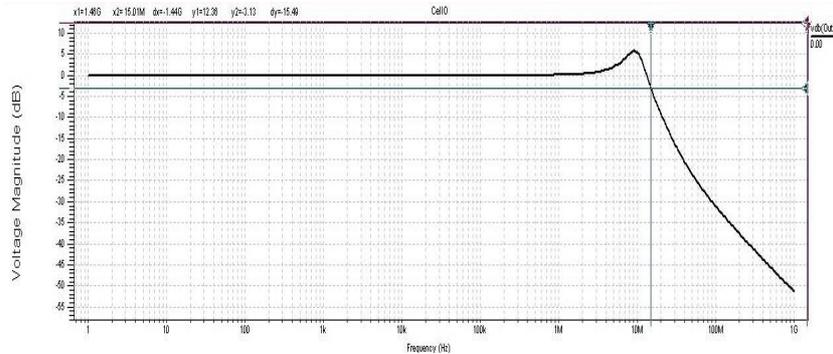


Fig. 8 Closed loop frequency response.

Fig. 8 shows the closed loop frequency response for voltage follower configuration which represent the closed loop unity gain bandwidth (-3dB bandwidth) is 15MHz.

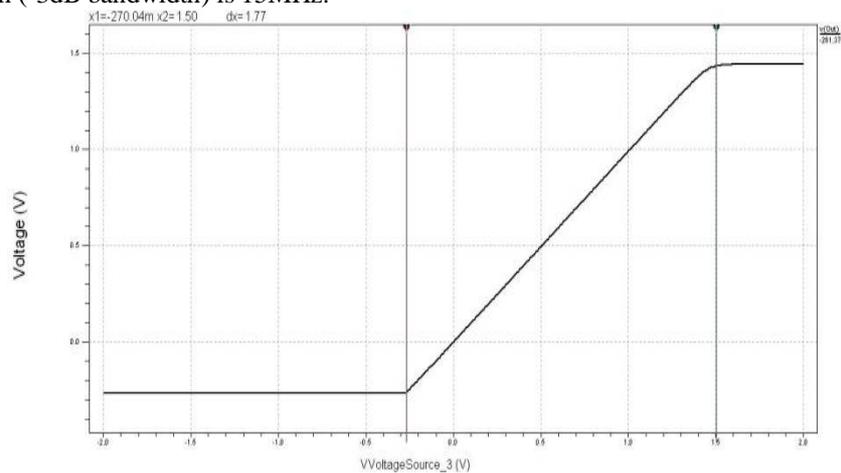


Fig. 9 Input common mode range (ICMR) of designed CMOS OTA.

Fig. 9 shows the measured input common mode range of designed CMOS OTA from simulated curve is -0.27 Volt to +1.5 Volts.

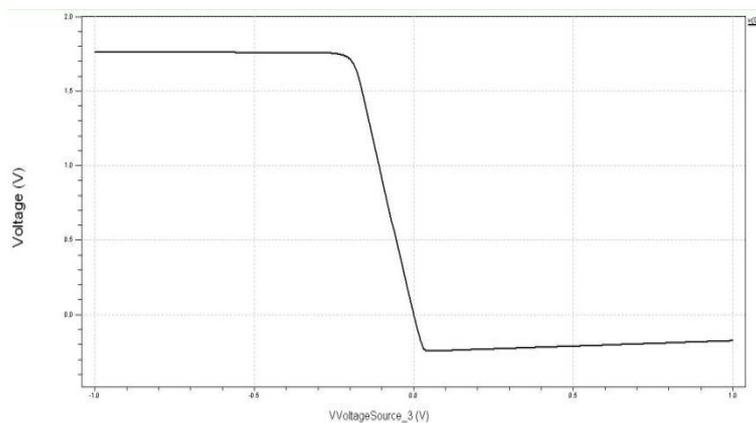


Fig. 10 Output swing of designed CMOS OTA.

Fig. 10 shows the output swing of designed CMOS OTA from simulated curve is -0.25 Volt to +1.78 Volts.

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 2, February 2016

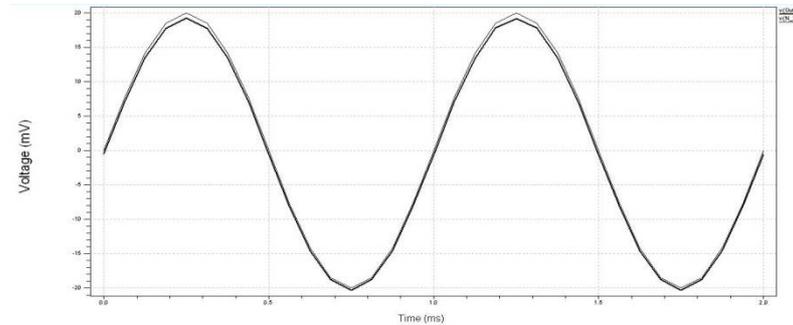


Fig. 11 Simulated Slew characteristics of designed CMOS OTA.

Fig. 11 illustrates the slew characteristics of designed CMOS OTA which provide expected result.

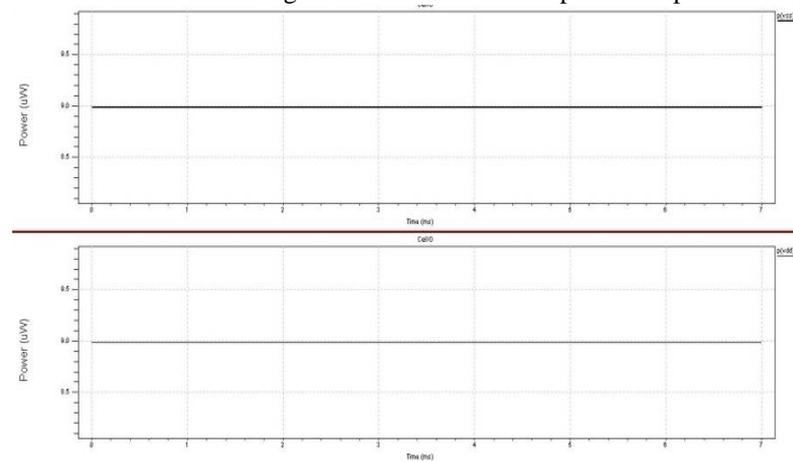


Fig. 12 Power consumption of designed CMOS OTA.

Fig. 12 represents power consumption of simulated CMOS OTA which has been found very low as 9 μ Watt.

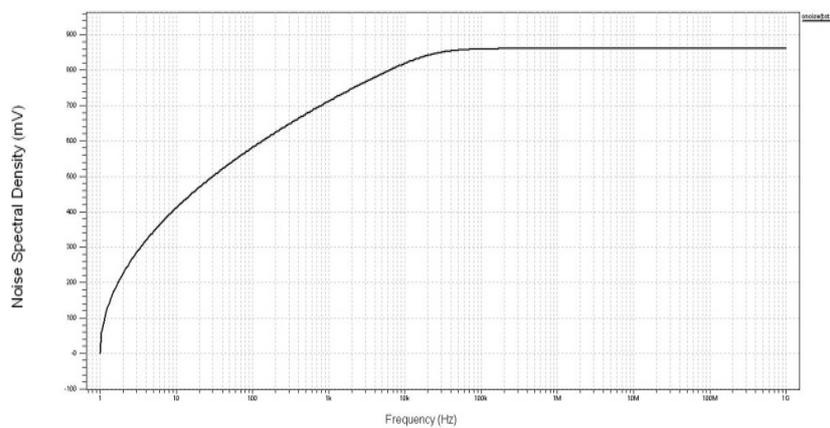


Fig.13 Noise spectral density of designed CMOS OTA.

Fig. 13 depicts variation of noise spectral density with frequency of designed CMOS OTA



International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 2, February 2016

VI. CONCLUSION

In this work two stage operational transconductance amplifiers has been designed and simulated using TANNER tools ver.13 with 0.18 μ m CMOS technology at 1.8V supply voltage.The simulation result agree with theoretical prediction which confirms that the design aspect is suitable for low power, high differential gain, high CMRR and PSRR CMOS OTA .The simulated characteristics shows open loop gain of CMOS OTA is 54.03db with phase margin of -150.03 degree and 9 μ Watt power dissipation.

REFERENCES

- [1] Bhumika B.Thakkar, Kehul A. Shah “Design of low power cmos two stage op-amp”,International Journal of Electrical and Electronics Engineers Vol. 07, Issue 01, pp.334-339, Jan- June 2015.
- [2] Sayan Bandyopadhyay, Deep Mukherjee, Rajdeep Chatterjee,“ Design of two stage CMOS op-amp in 180nm technology with low power & high CMRR”, Int. J. of Recent Trends in Engineering & Technology,ACEEE, vol. 11, pp. 239-247, June 2014.
- [3] Hitesh Modi, Nilesh D. Patel “Design and Simulation of Two Stage OTA Using 0.18 μ m and 0.35 μ m Technology”, International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Vol.02, Issue-3, pp. 445-448, February 2013.
- [4] B. Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw-Hill, p.p. 291-335, edition 2002.
- [5] P.E. Allen and D.R. Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 2002.
- [6] Debaprasad Das,“VLSI Design”, Oxford University Press, 2010.

BIOGRAPHY



SOUMEN PAL is at present Assistant Professor in department of Electronics and Communication Engineering at Narula Institute of Technology, Kolkata,West Bengal, India. He received B.TECH degree in Electronics and Communication Engineering from W.B.U.T, Kolkata and M.Tech degree in VLSI design and Microelectronics Technology from Jadavpur University, Kolkata.His teaching and research areas include VLSI circuits and nano devices.



PUSPAK PAIN is at present Assistant Professor in department of Electronics and Communication Engineering at Narula Institute of Technology, Kolkata,West Bengal, India. He received the B.E. and the M.Tech degrees in Electronics and Communication Engineering from the University of Burdwan and W.B.U.T,Kolkata respectively. His teaching and research areas include analog circuits and solid state devices.