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Design of Ultra Low Power CMOS Temperature Sensor for Space Applications

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Abstract*:* In this paper we are introducing novel Ultra Low Power CMOS temperature sensors for space applications. Nowadays for each & every application new standard circuits are required. This proposed CMOS temperature sensor is able to measure the temperature range from -150^{o}C [-238 ^{o}F] to 260^{o}C [500 ^{o}F]. This low power CMOS temperature sensor is able to work in harsh environment. It is gainsay to design wide range, linear response from -150^{o}C to 260^{o}C temperature sensor for different space applications such as environment cooling systems, oil in hydraulic and lubricating system and fluid in coolant and heating systems. This circuit is designed in concept of SoC and operates with a single rail power supply of 1V. This circuit power consumption is 0.752µW [-238 ^{o}F] and 46.7 µW [500^{o}F] . The sensitivity of this circuit is about 0.18 µW/ ^{o}C. This paper based on Proportional to Absolute Temperature (PTAT) and Negative Temperature Coefficient (NTC). This circuit is designed & simulated using Cadence Analog & Digital system design tools UMC 90nm technology.

Keywords: CMOS: Complementary Metal Oxide Semiconductor; VLSI: Very Large Scale Integration Circuit; SOI: System on Insulator; SoC: Silicon on Chip.

I. INTRODUCTION

Temperature is one of the most important fundamental physical quantities and is almost common in our daily life and which is independent of the amount of material i.e. temperature is having intensive property. As we know hundreds or thousands of devices are formed on thin silicon wafers. Before the wafer is scribed and cut into individual chips, they are usually laser trimmed. Process compensated CMOS temperature sensor [1] has designed for microprocessor application. The beauty of this circuit is no need of any BJT component. This CMOS temperature sensor is able to sense range -40^{o}C to 85^{o}C. The ultra low power CMOS cell temperature sensor [2] designed with PTAT (Proportional to Absolute Temperature) with NTC (Negative temperature Coefficient). This temperature sensor able to sense ranges 32^{o}C to 127^{o}C.

0.6-2.0V CMOS temperature sensor [3] defined only bulk driven technology. This temperature sensor is designed to sense from 0 ^{o}C to 120 ^{o}C using UMC 0.13um technology. A single chip PTAT sensor [4] designed using CMOS technology. This temperature sensor having wider temperature range with excellent linearity. Its range is -100 ^{o}C to 200 ^{o}C and sensitivity is about 0.05mV/ ^{o}C. The chip is designed with a single voltage source 1.6V. It can be used in various applications.

Temperature is a physical quantity that is a measure of hotness and coldness on a numerical scale [5]. In a body in its own internal thermal equilibrium, the temperature is spatially uniform. Temperature is important in all fields of natural science. Temperature sensors are not only useful for space applications, but it has many more use in different areas such as physics, chemistry, geology, and biology etc.

As we know ICs designed chips from BJT are good in some operational conditions but there are problems of power dissipation and package density. Due to requirement of simplicity, reduced parasitic/latch-up and high package density we move in the direction on new technology CMOS SOI [6]. In CMOS circuit NMOS transistor are used as the best

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driver and PMOS as a load. Decreasing feature size and increasing package density cause self-heating of chips to become an important factor. Since by decreasing the gate length the latch-up/parasitic effect increases. Hence to reduce the latch-up/parasitic effect we intend to utilize CMOS SOI technology for the same purpose. This mentioned paper work aims at developing a low power micro system (MST) for continuous temperature monitoring with a longer life power harsh environmental condition.

In early days the diode and transistor their base-emitter voltage V_{BE} related to temperature. The best performance of BJT (Bipolar Junction Transistor) is -50°C to 150°C for good linearity. Over 200°C the BJT junction is destroyed [7]. We are approaching CMOS PTAT (Proportional to Absolute Temperature) temperature sensor. In CMOS the threshold voltage and mobility are two main factors which are temperature dependent parameter. In the MOSFET the best thing is that we can scaling the parameter i.e. we can change doping, threshold voltage, mobility etc. As we know that in modern VLSI technology if we changes in channel length of transistor, then doping concentration, mobility, threshold voltage is also changes. If the threshold voltage or mobility is varies then temperature is also varies.

A 405nW CMOS Temperature sensor is based on linear MOS operation [8]. This CMOS temperature sensor is suitable for ultra low power application with a MOS transistor operation in linear region, a linear relationship between delay and temperature can be obtained.

SOI CMOS technology is feasible for extreme temperature applications up to 225 °C [9]. This SOI CMOS temperature sensor is developed for radiation environments in aerospace applications.

We proposed an ultra low power CMOS temperature sensor with excellent linearity. This CMOS temperature sensor expresses best linearity between -150°C [-238 °F] to 260°C [500 °F]. These circuits are many more feasible in space applications such as environment cooling systems, oil in hydraulic and lubricating system and fluid in coolant and heating systems. These circuits are designed on the concept of PTAT (Proportional to Absolute Temperature) with NTC (Negative temperature Coefficient). It is designed and simulated using Cadence analog and digital system design tools UMC 90nm technology. It is operational on very low single power supply 1V and its power consumption is 0.755µW [-238 °F] and 46.7 µW [500°F].

II. METHODOLOGY

Simple current mirror based circuit is shown in Fig.1. We know that when we connect the gate to the drain of MOSFET then it operates in saturation region [10]-[12]. Connecting the gate to the drain means that the V_{DS} control I_D and therefore the channel transconductance become a channel conductance. When NMOS transistor comes in saturation region then

When $0 \le V_{GS} - V_T \le V_{DS}$

$$I_D = \frac{\mu_n c_{ox} w}{2l}\left[V_{GS} - V_T\right]^2 \tag{1}$$

After simplification of Equation (1) we get

$$V_{GS} = V_T + \sqrt{\frac{2I_D l}{\mu_n c_{ox} w}} \tag{2}$$

Where $V_T = V_{TO} + \gamma\left(\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|}\right)$ (3)

Where $V_{TO} = V_T(V_{SB} = 0) = V_{FB} + 2|\phi_F| + \frac{\sqrt{2q\varepsilon_{si} N_{SUB} 2|\phi_F|}}{c_{ox}}$ (4)

γ = Bulk Threshold Voltage

$$= \frac{\sqrt{2\varepsilon_{si} q N_{SUB}}}{c_{ox}} \tag{5}$$

ϕ_F = Strong Inversion Surface Potential

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$$= \frac{kT}{q} \ln\left(\frac{N_{SUB}}{n_i}\right) \quad (6)$$

V_{FB} = Flat Band Voltage

$$= \phi_{MS} - \frac{Q_{SS}}{c_{ox}} \quad (7)$$

Where $\phi_{MS} = \phi_F(substrate) - \phi_F(gate)$ (8)

Where $\phi_F(substrate) = -\frac{kT}{q} \ln\left(\frac{N_{SUB}}{n_i}\right)$ (9)

And $\phi_F(gate) = -\frac{kT}{q} \ln\left(\frac{N_{gate}}{n_i}\right)$ (10)

Q_{SS} = Oxide-charge= qN_{SS}

k = Boltzmann's Constant

T = Temperature (K)

n_i = Intrinsic carrier concentration [9].

Now V_T is directly proportional to temperature, hence V_{GS} will be varied with variable of temperature.

I_D depends upon V_{GS} hence current will change with change in V_{GS}. When we short gate to drain the V_{GS} change in V_{DS}.

That is $V_{GS} = V_{DS}$.

Hence we can write the current equation

$$I_D = \frac{\mu_n c_{ox} w}{2l}[V_{DS} - V_T]^2 \quad (11)$$

Differentiating equation (1) with respect to V_{GS} we get

$$\frac{\partial I_D}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}}\left[\frac{\mu_n c_{ox} w}{2l}(V_{GS} - V_T)^2\right]$$

And we know that transconductance (g_m)

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \left[\frac{\mu_n c_{ox} w}{2l} 2(V_{GS} - V_T)\right]$$

$$g_m = \left[\frac{\mu_n c_{ox} w}{l}(V_{GS} - V_T)\right] \quad (12)$$

Since $r_d = \frac{1}{g_m} = \frac{l}{\mu_n c_{ox} w(V_{GS} - V_T)}$ (13)

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From equation (13) it is clear that r_d is inversely proportional to aspect ratio (w/l). Hence if we are increasing the value of aspect ration the value of resistance will be decreases.

III. SIMULATION RESULT & DISCUSSION

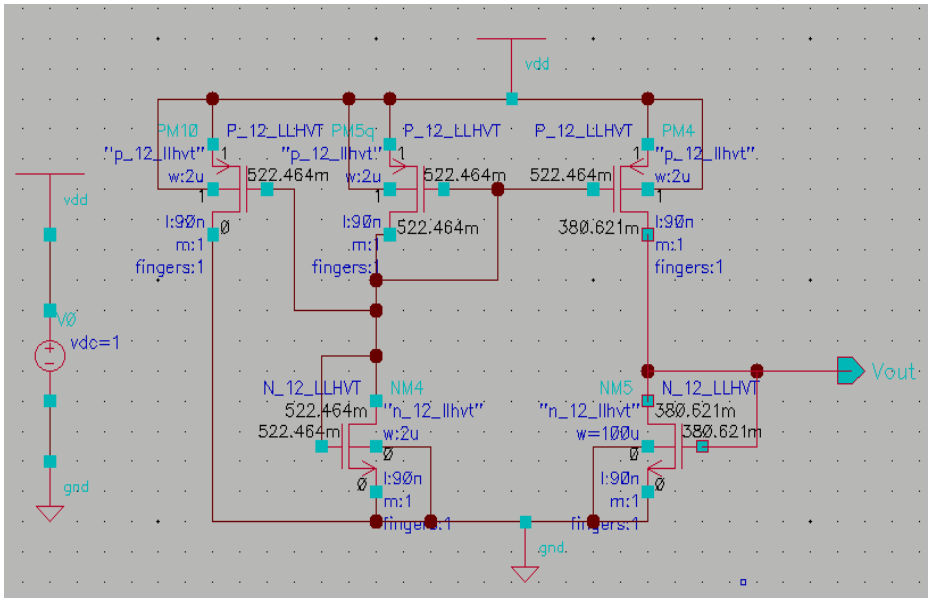

Fig. 1. Circuit diagram of ultra low power CMOS temperature sensor

A. At different w/l ratio

In the Fig (1) transistor M4 and M5 work as load. We plotted the graph between Voltage and Temperature on different aspect ratio of M5 is shown in Fig (2). In simulation we increase the value of aspect ratio range 25u to 100u with constant increment of 25u. We achieved wider excellent linearity between the ranges -150°C to 260°C at the aspect 100u and the voltage difference between this two temperature ranges is also good. Aspect Ratio of all transistor are given below S1=S2=S3=2u/90n. S4=2u/90n, S5=Variable; and Power Supply Voltage V_{DD}=1V. The temperature range at different aspect ratios is shown in table1.

TABLE -1
Temperature Range at different W/L ratio

W (M5)	Excellent Linearity Between Temperature Range	
25u(Plus)	-115°C (At 480mV)	260°C (At 345mV)
50u(Box)	-140°C (At 479mV)	260°C (At 301mV)
75u(Square)	-140°C (At 476mV)	260°C (At 276mV)
100u(Circle)	-150°C (At 474mV)	260°C (At 258mV)

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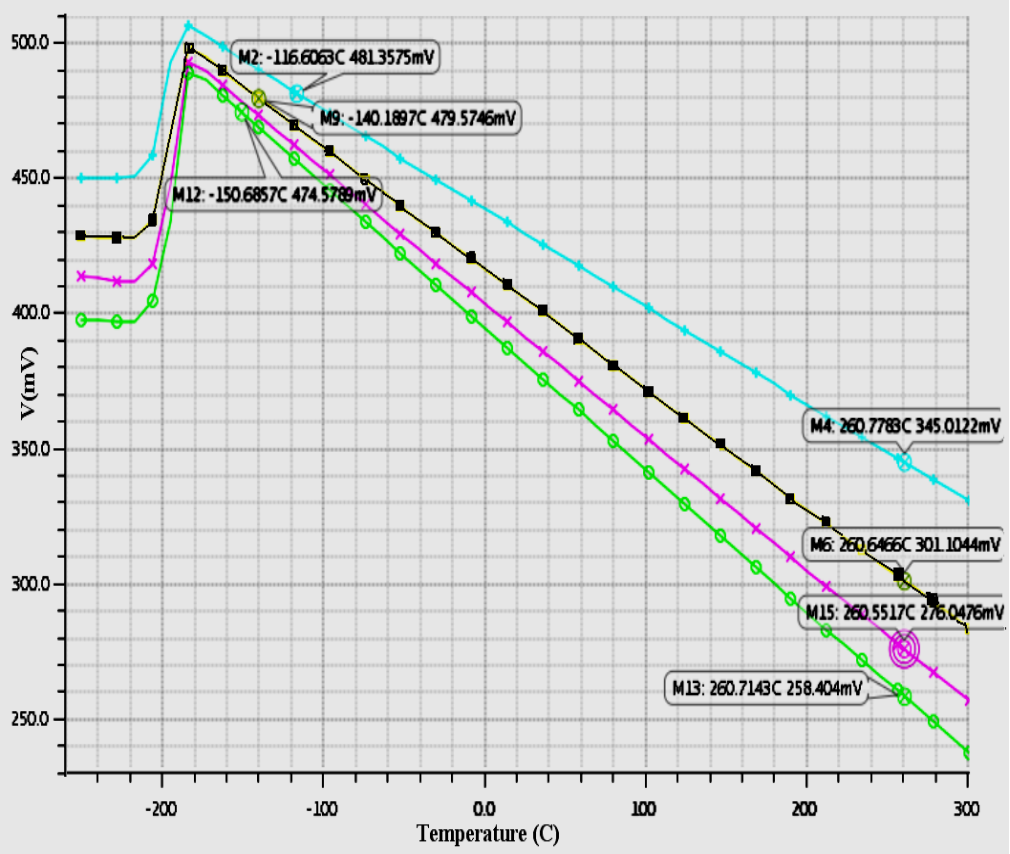

Fig. 2. Temperature vs Voltage graph at different W/L ratio at 90nm Technology.

B. At different power supply(V_{DD})

Fig.3 shows the range of temperature sensor at different power supply (V_{DD}). Hence we are changing the voltage from 0.750V to 2.000 V with increment of 0.250V. We achieved better result at 1V fixed aspect ratio of all transistors. S1=S2=S3=2u/90n, S4= 2u/90n, S5=100u/90n. Temperature range at different supply voltage is shown in table-2.

TABLE -2
Temperature Range at different supply voltages

Voltage	Excellent Linearity Between Temperature Range	
0.750V (Cross)	-100^{o}**C** (At 335mV)	216^{o}**C** (At 187mV)
1.000V (Circle)	-150^{o}**C** (At 474mV)	260^{o}**C** (At 258mV)
1.250V (Square)	-100^{o}**C** (At 536 mV)	202^{o}**C** (At 363 mV)
1.500V (Plus)	Nonlinear	
1.750V(Down Arrow)	Nonlinear	
2.000V(Up Arrow)	Nonlinear	

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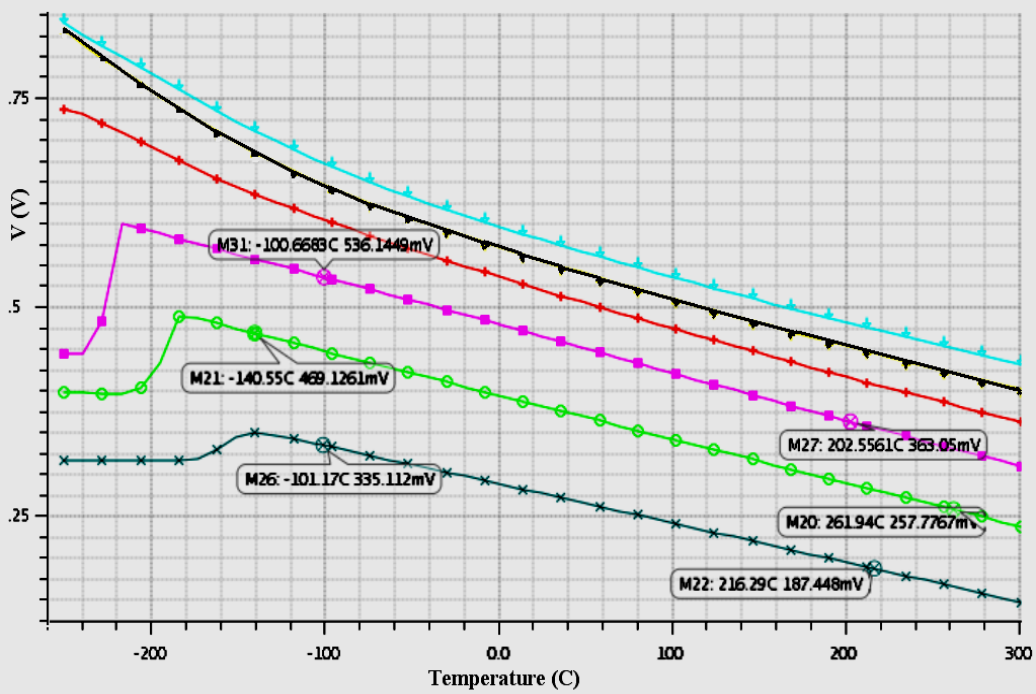

Fig. 3. Temperature vs Voltage graph at different power supply.

C. At fixed w/l ratio and fixed powers supply

Fig.4 shows the fixed supply 1V and fixed aspect ratio of all Transistors. S1=S2=S3=2u/90nm, S4= 2u/90nm, S5=100u/90n.

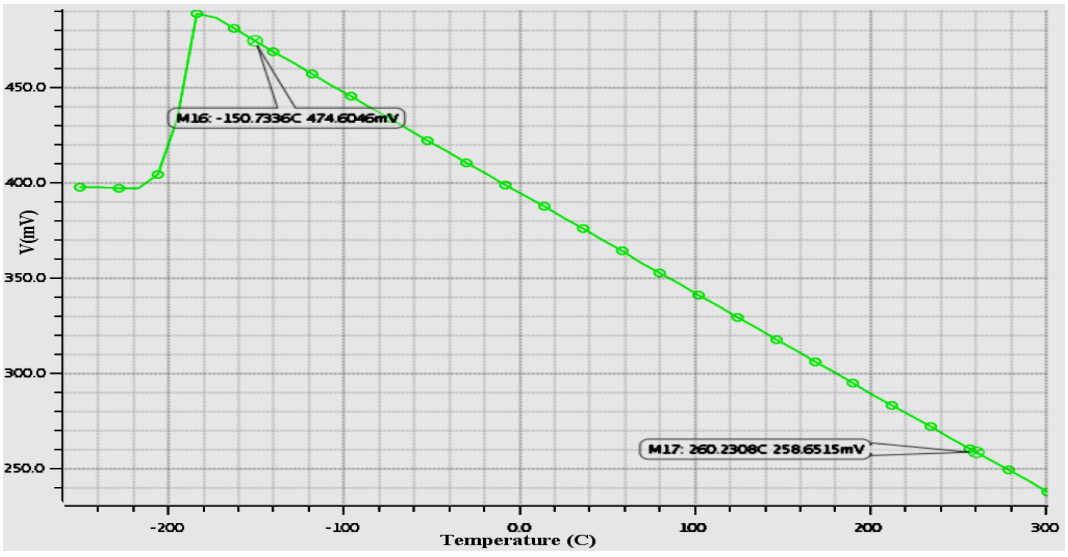

Fig. 4. Temperature vs Voltage graph at fixed W/L ratio and fixed power supply.

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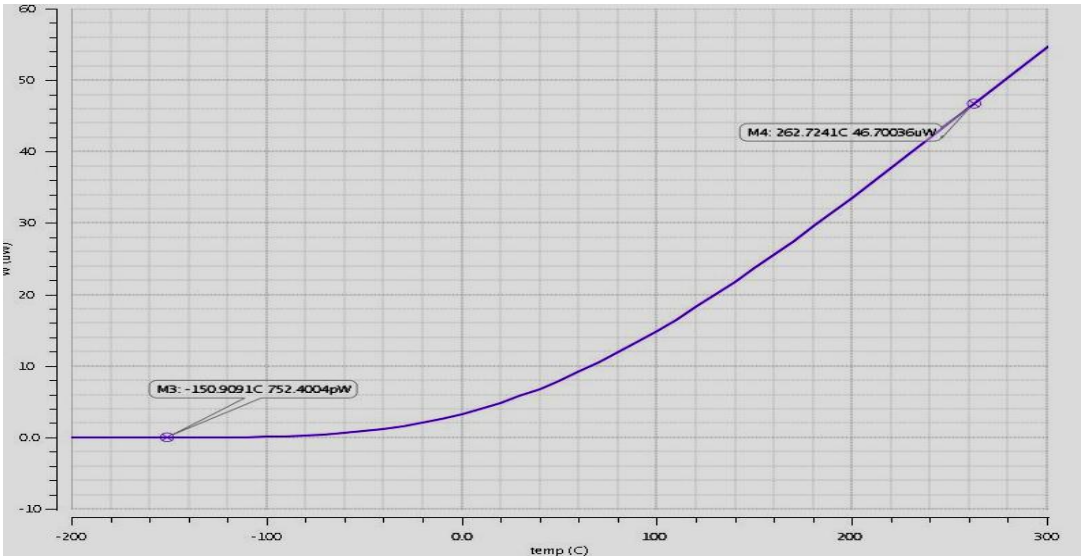

Fig. 5. Temperature vs power consumption graph at fixed W/L ratio and fixed power supply.

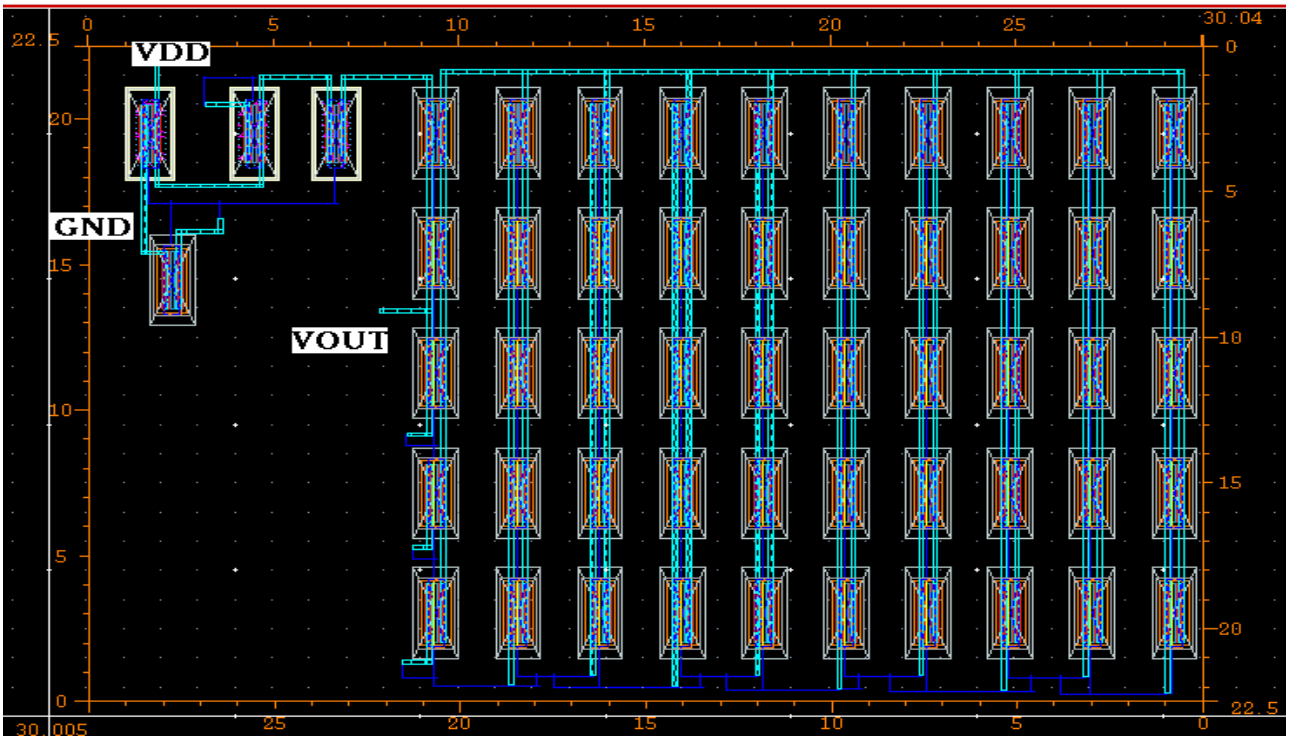

Fig. 6. Layout of ultra low power CMOS temperature sensor circuit.

Temperature vs power consumption graph at fixed W/L ratio and fixed power supply is shown in Fig.5. The layout of ultra low power CMOS temperature sensor is shown in Fig.6. Its layout area is 30 μm X 20.5 μm.

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IV. CONCLUSION

A ultra low power CMOS temperature sensor is designed with excellent linear range of -150 ^{o}C to 260 ^{o}C. The layout area of this circuit is 30 μm X 20.5 μm. The Circuit designed for fabrication in UMC Belgium with Cadence analog and digital system design tools with UMC 90nm technology. It is operational on very low single power supply 1V and its power consumption is 0.755µW [-238 ^{o}F] and 46.7 µW [500^{o}F]. The sensitivity of this circuit is about 0.18 µW/ ^{o}C.

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BIBILOGRAPHY

Abhishek Pandey was born in Maharajgunj, Uttar Pradesh, India in 1988. He received his Bachelor degree in Physics and Master degree in Electronics from DDU Gorakhpur University Gorakhpur in 2007 and 2009. He was selected as JRF in 2011 in Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra, Ranchi in a project, funded by DST New Delhi & DRDL Hyderabad, India. Project title was "Design of Ultra Low Power CMOS Cell for Temperature Sensor in VLSI". In later 2012 he was selected for Ph.D. degree in VLSI Design, Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra, Ranchi-835215. He has three publications in National & International Journal and Conferences repute. His area of research interest is VLSI Design, Technology and Embedded System.

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Vijay Nath was born in Gorakhpur (U.P.) India in 1976. He received his Bachelor degree in Physics and Master degree in Electronics from DDU Gorakhpur University, Gorakhpur in 1998 and 2001. He received PGDCN from MMM Engineering College Gorakhpur (Gold Medallist) in 1999. He received Ph.D. degree in VLSI Design & Technology from Dr. RML Avadh University, Faizabad in association with CEERI- Pilani in 2008. He was faculty in Department of Electronics, DDU Gorakhpur University, Gorakhpur (2002-2006). In 2006, he joined as a faculty in Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra, Ranchi, India.
Presently, he is Professor In-charge of VLSI Design Lab & Embedded System Design Lab, Dept. of ECE, BIT Mesra, Ranchi. He is guiding four Ph.D. students in VLSI and embedded system design areas. His research area includes analog, digital, mixed CMOS VLSI circuits, low power VLSI circuits, ADC, DAC, PTAT, CMOS bandgap voltage reference, piezoresistive pressure sensors, double ring capacitive pressure sensors, MEMS sensors, signal-processing circuits, ASICs, embedded systems designs, smart cardiac pacemaker, early stage cancer detection etc. He recipient of Viveka Nanda Techno Fiesta Best Award for outstanding conference paper, VNTF-2002. He also recipient of Young Scientist Award for outstanding conference paper, IAPS-2004. He has around 40 publications in national & international journals and conferences. He is member of VSI, USI, The Institutions of Engineers, ISTE, IETE and IEEE etc. Presently, he is advisor of the Electronics and Telecommunication, The Institution of Engineers(India), Jharkhand State Centre, Doranda, Ranchi. He is principal developer of course "VLSI Design" in National Mission Project on Education through ICT, MHRD, India & coordinated by IIT Kharagpur (He is also developing suitable pedagogical methods for various classes, intellectual calibers and research in e-learning for the course of **VLSI Design)**. He conducted Summer School on VLSI Design (SSVD_2011, 12 in three phases; 5days each), Winter School on VLSI Design (WSVD_2011 in three phases; 5 days each), Industrial Training on Embedded System Design(ITESD_2012, one phase,15 days), TEQIP funded Workshop/Refresher Course on Advanced VLSI Design(TWAVD_2012, one phase (15 days)) for faculty /scientist and industry persons. Including all the workshop more than 200 students, faculty & industry persons participated from reputed institutions. He establishes the industry level VLSI Design Lab of Cadence (45nm) in BIT Mesra and tie-up with IMEC/UMC Belgium(USA) for fabrication of designed IC in his lab. He is author two books 1- Fundamental of Embedded System Design and Applications, 2- CMOS Digital Logic Design with VHDL and Verilog. He has several R&D ongoing projects of DST, DRDL, and WSU London. He is editorial board member of international journal of systemic, cybernetics and informatics, IJ-CA-ETS and IJ-ETA-ETS. He was invited to chair different IEEE international conference programs and sessions. He has been serving in the program committees & advisory committees of over a dozen international conferences. Dr. Nath was invited to offer keynote lectures in different IEEE and others international conferences.