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Effect of High-K Oxide Layer on Carrier Mobility

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ABSTRACT: Over the past three decades CMOS has emerged as the basis of design in nanotechnology. MOSFETS provide an easier way of fabrication due to their ease of manufacturing and lower power consumption than the BJTs. However the use of high k materials to follow Moore's Law, has created certain problems in the working of these devices. In this review we have dealt with the mobility related issue, which has been a major cause of concern. The degradation of mobility due to Coulomb scattering, Phonon scattering and other methods have been focused upon. The remedies of mobility improvement have also been highlighted. This review entails about the basic details of mobility in these devices with SiO_2 and also with other high k materials. There are certain mechanisms which wrongly measure the count of charge carriers and give an overestimation or underestimation of the mobility, causing serious concern. The errors in mobility calculation and the overestimation of carrier count is a part of this review.

KEYWORDS: Coulomb scattering, Phonon scattering, Carrier trapping, mobility.

I. INTRODUCTION

Over the past three decades, CMOS technology scaling has been a primary driver of the electronics industry and has provided a path towards both denser and faster integration. The transistors manufactured today are 20 times faster and occupy less than 1% of the area of those built 20 years ago. The number of devices per chip and the system performance has been improving exponentially over the last two decades according to Moore's law. As the channel length is reduced, the performance improves, the power per switching event decreases, and the density improves. But the power density, total circuits per chip, and the total chip power consumption has been increasing.

The need for more performance and integration has accelerated the scaling trends in almost every device parameter, such as effective channel length, gate dielectric thickness, supply voltage, device leakage, etc. SiO_2 has been used as a gate oxide material for decades. As the thickness scales below 2nm, leakage currents due to tunneling increase drastically, leading to high power consumption and reduced device reliability. Replacing the silicon dioxide gate dielectric with a high-K material allows increased gate capacitance without the associated leakage effects. Since it becomes necessary to replace the SiO_2 with a physically thicker layer of oxides of higher dielectric constant (K), there are various oxides under consideration for this purpose such as HfO_2, hafnium silicate, ZrO_2 and various lanthanides and it was found that in many respects they have inferior electronic properties than SiO_2, such as a tendency to crystallize and a high concentration of electronic defects. The objective of using high-k oxides in place of silicon dioxide is to create smaller and faster devices. The speed of the device follows source to drain current, which in turn depends on the carrier mobility. The effective mobility μ_{eff} is defined in terms of the measurement of drain current I_d, in the linear region as:

$$I_d = \mu_{eff} C_{ox} \frac{W}{L} [(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}] \quad (1)$$

where,

C_{ox} is capacitance of oxide,

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W is width of oxide,
L is the channel length,
V_{GN} is gate voltage,
V_{TH} is threshold voltage,
V_{DS} is drain voltage.

One of the serious issues in high-k/metal gate stacks is degradation of effective mobility. CMOS devices with SiO_2 gate oxide have mobility close to 300 cm/V-s for the electric field and doping concentration used. The mobility offered by high K oxides is below this value. It can be easily expected that effective mobility is reduced with high-k directly in contact of Si as shown in figure 1. The mobility is limited mainly by interface roughness over the range.

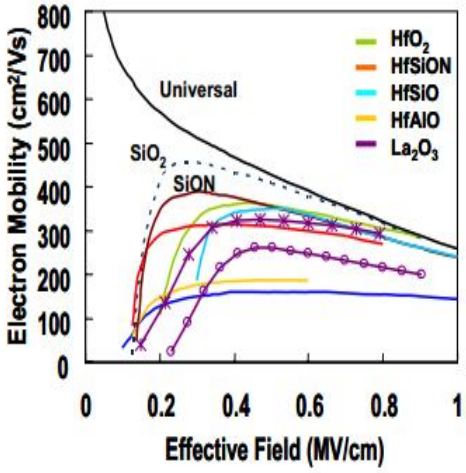

Figure 1: Degradation in Effective Mobility Using High-K Gate Oxides As Compared To SiO_2.

II. MOBILITY DEGRADATION

Mobility degradation is one of the crucial drawbacks of using high–K materials as a gate oxide as an alternative to SiO_2 in Metal Oxide semiconductor field effect transistors (MOSFET). There are certain mechanisms of decline in mobility of the charge carriers. This entails to the internal mechanisms of the device which has to be studied carefully and can be observed only after careful scrutiny. There are certain remedies which can make up to the drawback of decrease in mobility, which are discussed at the end of this review.

The observations made by Takegi et al. [3] suggested that the mobility of electrons and holes depends only on the effective gate field and Si surface [5]. The individual components of mobility add according to Matthiessen's rule,

$$\frac{1}{\mu} - \frac{1}{\mu_c} + \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR}} \qquad (2)$$

where,

μ_c is the mobility of Columbic scattering,
μ_{PH} is the mobility of phonon scattering,
μ_{SR} is the mobility of surface roughness.

The mobility is limited by different mechanisms at different fields, as each obeys a different power law with field. At low fields, mobility is limited by Columbic scattering(*C*) by trapped charges in the oxide, channels and gate electron interface; at moderate field it is limited by phonon scattering (*PH*), and at high fields by scattering by surface

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roughness (*SR*) as shown in figure 2. [4] The main focus is on Coulomb scattering due to interface traps and Phonon scattering due to soft optical phonons.

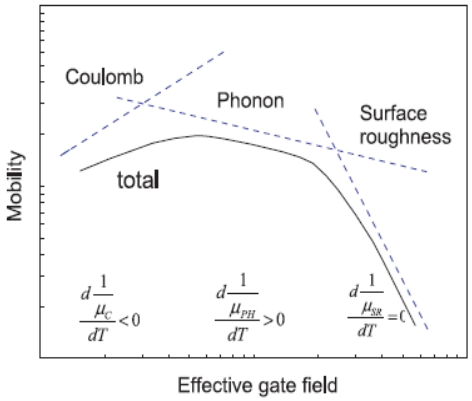

Figure 2: Schematic carrier mobility vs. vertical field in FETs in the universal mobility model.

A. Coulomb scattering

The coulomb scattering due to interface trapped charge is the dominant mechanism of mobility degradation of high-k gated MOSFETS at low fields. This is due to the fact that the energy distribution of the interface traps is found to be asymmetric as shown in figure 4.

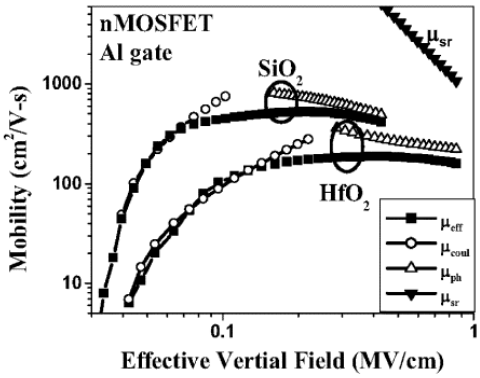

Figure 3: Effective mobility for the two samples, HfO_2 and SiO_2 samples due to Coulomb scattering and Phonon scattering

The interface trap density near the conduction band edge is higher than that near the valence edge as revealed by the larger sub-threshold swing of the n-MOSFET as compared to that of the p-MOSFET. Hence, the degradation of hole mobility in p-MOSFET is generally less severe than that for electron mobility in n-MOSFET as shown in fig. Coulomb scattering is mainly due to the electrostatic forces on the electrons when present in electric field.

B. Phonon scattering

In addition to Coulomb scattering caused by high densities of interface traps and oxide charge, the scattering due to soft optical phonons is a fascinating possibility that can't be denied and the possibility is captured in figure. As shown in figure the mobility limited by phonon scattering in HfO_2 gated MOSFETS is lower than SiO_2 gate oxides. MOSFETS with several high-k oxides such as HfO_2 has an additional source of phonon scattering.

III. Methods to Improve Mobility

The problem of mobility degradation can be overcome by substituting the poly-silicon gate electrode with metal gate as shown in figure 4. The conductivity of the poly-silicon layer is very low and because of this low conductivity, the charge accumulation is low, leading to a delay in channel formation and thus unwanted delays in circuits. The poly layer is doped with N-type or P-type impurity to make it behave like a perfect conductor and reduce the delay. Doped

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poly-silicon is a semiconductor, and thus will form a "depletion" region when voltage is applied. This "depletion" region acts very much like a thicker oxide, in that it reduces inversion charge (thus reducing inversion capacitance) with resulting degradation in drive current.

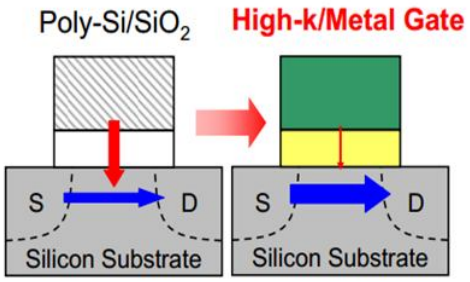

Figure 4: Replacement of Poly-Si/SiO2 with high-k/metal Gate

The metal gate have free carrier density more than $1\times10^{20}/cm^3$, which makes it possible to dynamically screen the longitudinal soft optical phonon modes arising from high-K dielectric materials. The metal gate electrodes help to screen the dipole coupling of remote phonon scattering. Thus are able to decrease phonon scattering and reduce the mobility degradation problem. The influence of dipole vibrations on the channel electrons can be reduced significantly by increasing the density of electrons in the gate electrode. Figure 5 shows how mobility is increased by replacing poly-Si with metal gate. Thus high-K oxides with metal gate have higher mobility than with poly-Si gate. In figure 6 it can be seen that HfO_2 with metal gate have improved mobility

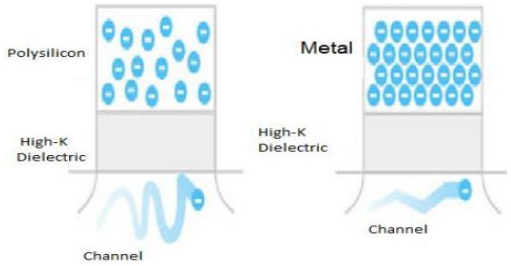

Figure 5: Increase in channel mobility by replacing poly-silicon gate with a metal gate [2]

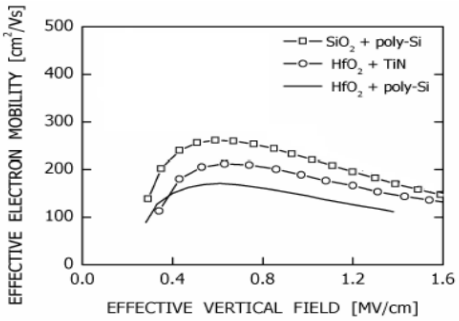

Figure 6: Effective electron mobility for a) HFO_2 with poly-Si b) HFO_2 with TiN c) SiO_2 with Poly-Si.[3]

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IV. MOBILITY MEASUREMENT AND CORRECTIONS

The effective mobility, μ_{eff}, can be obtained by measuring the drain current in the linear region.

$$\mu_{eff} = \frac{L}{W} \cdot \frac{I_{dV_g}}{V_d Q_{inv}} \qquad (3)$$

In the past, many people used the following relationship to obtain Q_{inv} for a MOSFET with a relatively thick gate dielectric in strong inversion: $Q_{inv} = C_{ox}$ (V_g-V_T) .The fact that this is a poor approximation for MOSFETs with thin gate oxides began to be recognized in the early 1980s, and the split capacitance–voltage (*C–V*) technique was introduced [3] to extract Q_{inv} more accurately by measuring the gate-channel capacitance as a function of gate voltage.

$$Q_{inv} = \int_{-\infty}^{V_g} C_{gc} V_g dV_g \qquad (4)$$

However we will show that this split *C–V* method to evaluate Q_{inv} is still very inadequate for high-k samples with high densities of interface traps and high leakage current. The error introduced by the interface traps may arise from two sources: First, the interface traps can respond to the ac modulation signal in the capacitance measurement, which results in an additional parallel capacitance C_{it} [3] that can result in an over count of Q_{inv}. This error can be minimized by using a higher frequency such that the interface traps cannot follow the ac signal or corrected by subtracting out the effect of the interface traps if one can accurately measure the interface-trap density. This aspect has been effectively dealt with by others [3], and therefore is not the focus of this paper. Second, the interface traps can follow the dc voltage sweep, so that a change of in gate voltage not only results in a change of dV_g the inversion charge dQ_{inv}, but also a change of dQ_{trap} in the charge trapped in interface traps [3], which can be expressed as,

$$dV_g = -\frac{(dQ_{inv} + dQ_{trap})}{C_{ox}} \qquad (5)$$

Where, C_{ox} is the oxide capacitance per unit area. This *C–V* stretch out effect would result in an over estimated inversion charge [3]. In this thesis, we propose a simple method to correct this error without having to measure the interface-trap density. The effects of channel resistance in weak inversion, gate leakage current, and contact resistance on the mobility extraction are also presented in this thesis, as they are distinctly different from the effects of interface traps.

V. ACCURATE MEASUREMENT OF MOSFET WITH ULTRA-THIN HIGH-K DIELECTRICS

In this section, we will discuss the following factors that could result in significant errors in mobility extraction carrier trapping, channel resistance in weak inversion and contact resistance. C_D, C_{ox}, C_{inv}.

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A. Carrier Trapping

Figure 6.4 serves to illustrate this correction method. Fig. 6.4(a) shows the experimental high-frequency gate-channel capacitance C_{gc} (i.e., part of the split C_{gc}~V_{gc} data) of a HfO_2 gated n MOSFET with interface traps (including border traps, along with the simulated ideal gate-channel capacitance without interface traps. Assuming that traps in inversion for this sample cannot follow the high frequency ac signal, or the interface-trap capacitance C_{it}, can be neglected for high-frequency measurement, then the gate-channel capacitance for metal gate samples is equal to

$$C_{gc} = (C_{ox}^{-1} + C_{inv}^{-1} + \frac{C_D}{C_{ox} C_{inv}})^{-1} \qquad (6)$$

Where,

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C_{ox} is the oxide capacitance,
C_{inv} is the inversion capacitance and,
C_D is the depletion capacitance.

Here the inversion capacitance is defined as,

$$C_{inv} = \frac{dQ_{inv}}{d\psi_s} \qquad (7)$$

Where, Q_{inv} is the inversion charge density, and ψ_s is the surface band bending in Si. Since the inversion capacitance is C_{inv} unchanged with or without traps, the gate-channel capacitance as a function of inversion charge, $C_{gc}(Q_{inv})$, should be the same with or without interface traps.

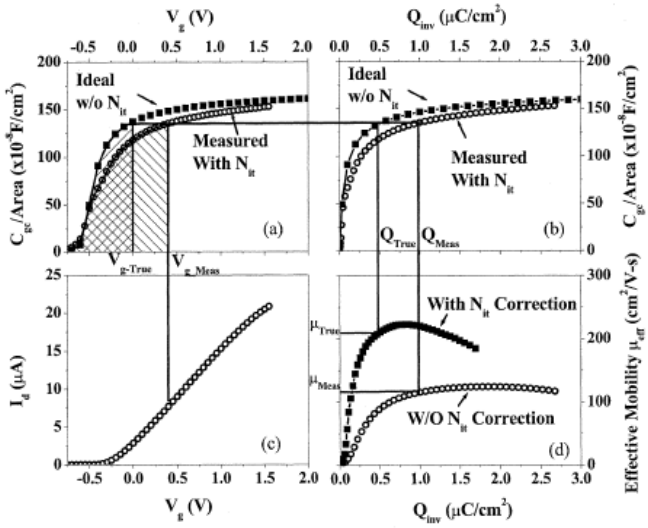

Figure 7: Illustration of interface trap correction for extracting effective mobility. (a) Measured C_{gc} for MOSFETs with interface traps (open symbols) and ideal C_{gc} without interface traps (solid symbols); shadow areas result from the integration of the measured and ideal C_{gc}~V_{gc}. (b) Surface charge in the inversion channel extracted from measured C versus V curve (open symbols) and the one from ideal C_{gc}~V_{gc} curve (solid symbols). (c) I_{gc}~V_{gc} measured from the MOSFET with interface traps. (d) Uncorrected mobility calculated from the surface charge extracted from measured C_{gc}~V_{gc} (open symbol), and the corrected one obtained from the inversion charge extracted from ideal C_{gc}~V_{gc} (solid symbol).

However, the inversion charge density Q_{Meas} in Figure 7(b), which we extracted by integrating the measured $C_{gc\ measured}$~V_g with interface traps, always exceeds Q_{True}, which is obtained by integrating the ideal curve for the same. This is because contains both the inversion carrier charge and the interface trapped charge, while Q_{True} contains only the inversion carrier charge. Since only the mobile inversion channel charge Q_{True} contributes to the drain current, we should use Q_{True} rather Q_{Meas} than to calculate the mobility. Figure 7(d), shows the mobility μ_{True} and μ_{Meas} calculated from Q_{True} and Q_{Meas} respectively. As we can see, the corrected mobility μ_{True} is much higher than the uncorrected mobility μ_{Meas}. Note that this correction is not affected by the existence of the oxide charge in the film, since the inversion charge-density Q_{True} , shown as the shaded area in Fig. 6.4(a), does not change when the curve is

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shifted along the V_g axis. The validity of this correction method has been confirmed by Hall mobility measurement. It should be worth pointing out that Q_{Meas} is not simply equal to the sum of inversion charge Q_{inv} and the interface trapped charge Q_{it}. In fact, it is less than that

$$Q_{Meas} = Q_{inv} + \int_0^{Q_{it}} \frac{C_{gc}}{C_{ox}} dQ_{it} < Q_{inv} + Q_{it} \quad (8)$$

Therefore, there is an error if one simply subtracts the interface trapped charge Q_{it} from the measured surface charge Q_{Meas} to get the mobile inversion charge Q_{inv}.

On the other hand, since

$$Q_{True} = \int_{-\infty}^{V_{g1}} C_{gc-ideal} dV_g = \int_{-\infty}^{V_{g1}} \left(\frac{dQ_{inv}}{dV_g}\right) dV_g = Q_{inv'} \quad (9)$$

one may reliably use Q_{True} to represent Q_{inv} in extracting the mobility. To estimate the errors incurred by the trapping effect, we note that the error in the inversion charge extracted from split *C-V* without correction is

$$\Delta Q = Q_{Meas} - Q_{True} = \int_0^{Q_{it}} \frac{C_{gc}}{C_{ox}} dQ_{it} \quad (10)$$

Correspondingly, the error in the mobility extracted from split *C–V* without correction is

$$\Delta\mu = \mu_{Meas} - \mu_{True} = \mu_{True} \frac{-\Delta Q}{Q_{inv}+\Delta Q} \quad (11)$$

B. Channel Resistance in Weak Inversion

As we mentioned in Section I, in order to avoid the interference of the interface-trap capacitance C_{it}, the frequency used in the split *C–V* measurement must be as high as practical. In addition, for high-leakage films, in order to reduce the dissipation factor ($D=\frac{G}{\omega C}$) and get an accurate inversion capacitance, one also needs to use the highest measurement frequency possible. However, this may cause a problem arising from channel resistance in weak inversion. Fig. 6.5(a) shows the apparent effective mobility of HfO_2-gated transistors with various gate lengths from 50 to 5 measured at 1 MHz.

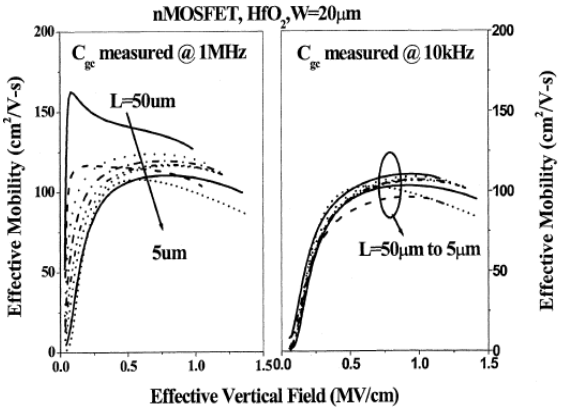

Figure 8: Mobility values of HfO_2 -gated n-MOSFET with various channel lengths extracted from split *C–V* measured at (a) 1 MHz and (b) 10 KHz.

As one can see, there is significant channel length dependence of the extracted mobility, especially in the weak inversion region. Thus, the effects of interface traps and channel resistance determine the lower and higher limits of the measurement frequency respectively.

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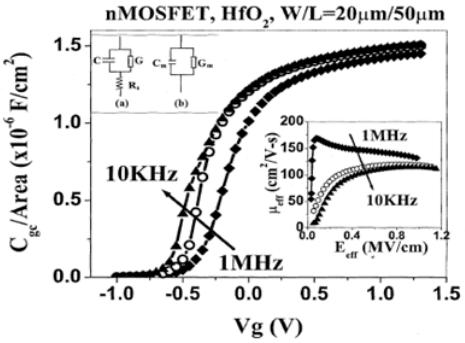

Figure 9: Gate-to-channel capacitances of HfO_2 -gated n-MOSFET with L =50μm measured at three different frequencies. The upper inset shows (a) the equivalent circuit model of the MIS capacitor and (b) the model for parallel capacitance measurement. The lower inset shows the apparent mobility values of this device as extracted from this set of split-*C*–*V* curves.

C. Contact Resistance

The effect of contact resistance on mobility extraction is well known, and gets more important as the channel gets shorter. In the case when the contact resistance is not negligible compared to the channel resistance, the voltage across the channel becomes $V_d - V_c$, where V_c is the voltage across the contact. This can be corrected by measuring the contact resistance from appropriate test structures. The mobility with contact resistance correction is much higher than the uncorrected one, especially at high electric fields.

VI. Conclusion

This review also discusses the effect of High-K oxides on the mobility of charge carriers, accurate measurements and degradation mechanisms of charge carriers with HfO_2 as dielectric. The commonly encountered sources of error, like, trapping by high densities of interface traps leads to over counting of inversion charge carriers, high gate leakage current through ultra-thin high-K film could result in underestimation of mobility at high fields, the large channel resistance in weak inversion could result in high artificial mobility at low fields, error due to contact resistance for short channel MOSFETS. Certain mechanisms of mobility degradation have also been focussed. Coulomb scattering due to interface traps is a major cause of mobility degradation. Soft optical phonons also contribute to mobility degradation. Remedies for the escalation in mobility values have also been discussed.

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