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Efficient Multiplier-less Design for 1-D DWT Using 9/7 Filter Based on NEDA Scheme

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Abstract: In this paper, we present a new efficient distributed arithmetic (NEDA) formulation of the computation of 1-D discrete wavelet transform (DWT) using 9/7 filters, and mapped that into bit parallel for high-speed and low hardware implementations, respectively. We demonstrate that NEDA is a very efficient architecture with adders as the main component and free of ROM, multiplication, and subtraction. The bit-parallel structure has 100% hardware utilization efficiency. Compared with the existing multiplier-less structures, the proposed structures offer significantly higher throughput rate and involve less area-delay product.

Keywords: -Discrete Wavelet Transform (DWT), NEDA, Xilinx Simulation.

I. INTRODUCTION

The discrete wavelet transform (DWT) has been widely used in many areas of science and engineering, e.g., signal and image processing, bio-informatics, geophysics, and meteorology etc. for the applications involving compression and analysis of various forms of data. The well-known image coding standards, namely, MPEG-4 and JPEG2000 have adopted DWT as the transform coder due to its remarkable advantages over the other transforms. For loss compression, Daubechies 9/7 orthogonal filter is used as the default wavelet filter in JPEG 2000. Efficient implementation of DWT using 9/7 filters in resource-constrained hand-held devices with capability for real-time processing of the computation-intensive multimedia applications is, therefore, a necessary challenge. Multiplier-less hardware implementation approach provides a kind of solution to this problem due to its scope for lower hardware-complexity and higher throughput of computation.

Several designs have been proposed for the multiplier-less implementation of DWT based on the principle of distributed arithmetic (DA) [1]–[5]. The structure of [1] and [2] distributes the bits of the fixed coefficients instead of the bits of input samples. Consequently, the adder-complexity of the structure of [1] and [2] depends on the DA-matrix of the fixed coefficients.

Martina *et al* [4] have approximated the 9/7 filter coefficients and expressed the 9/7 filter outputs in terms of 5/3 filter outputs. By that approach, they have significantly reduced the adder-complexity of the 9/7 DWT. Longa *et al* [5] have suggested an LUT-less DA-based design for the implementation of 1-D DWT. They have eliminated the ROM cells required by the DA-based structures at the cost of additional adders and multiplexors. The adder-complexity of this structure is significantly higher than the other multiplier-less structures.

In this paper, we have proposed an efficient scheme to derive NEDA-based bit-parallel structures, for low-hardware and high-speed computation DWT using 9/7 filters. The remainder of the paper is organized as follows: mathematical formulation of NEDA-based computation of DWT using 9/7 filter is presented in Section II. The proposed structures are presented in Section III. Hardware and time complexity of the proposed structures are discussed and compared with the existing structures in Section IV. Conclusion is presented in Section V.

II. MATHEMATICAL DERIVATION OF NEDA

Let us consider the following sum of products:

$$D = \sum_{k=1}^{L} B_k \times C_k \qquad (1)$$

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Where B_k are fixed coefficients and they C_k are the input data words. Equation (1) can also be written in the form of a matrix product as:

$$D = [B_1 \quad B_2 \quad \dots \quad B_L] \begin{bmatrix} C_1 \\ C_2 \\ . \\ C_L \end{bmatrix} \qquad (2)$$

Both B_k and C_k are in two's complement format. The two's complement representation of B_k may be expressed as

$$B_k = -B_k^M 2^M + \sum_{i=N}^{M-1} B_k^i 2^i \qquad (3)$$

Where $B_k^i = 0$ or 1, and i = N, N+1… M and B_k^M is the sign bit and B_k^N is the least significant bit (LSB).

Equation (3) can be expressed in matrix form as:

$$B_k = \begin{bmatrix} 2^N & 2^{N+1} & \dots & 2^M \end{bmatrix} \begin{bmatrix} B_k^N \\ B_k^{N+1} \\ . \\ -B_k^M \end{bmatrix} \qquad (4)$$

Similarly C_k can be represented in two's complemented format as:

$$C_k = -C_k^X 2^X + \sum_{i=W}^{X-1} C_k^i 2^i \qquad (5)$$

Where $C_k^i = 0$ or 1, and i = W, W+1, …,X and C_k^M is the sign bit and C_k^N is the least significant bit (LSB).

Now on combining equations (1) and (3), we get-

$$D = -(D^M .2^M) + \sum_{i=N}^{M-1} (D^i .2^i) \qquad (6)$$

Where $D^i = \sum_{k=1}^{L} B_k^i C_k$, i = N, N+1… M

III. PROPOSED ARCHITECTURE

In this paper, we have proposed a multiplier-less architecture for 9/7 wavelet Filter by using NEDA. The filter coefficients of 9/7 wavelet filter are given in table1. We multiply the filter coefficients by 100 for simplification. The mathematical calculation for high pass output is explained by an example.
IN Table I, where h(0), h(1),… h(4) are the Low pass filter coefficients and g(0),g(1)…g(3) are the High pass filter coefficients.
If we take the high pass coefficients g(0),g(1),g(2) and g(3), and multiply by r(1),r(2),r(3) and r(4) then we get the High pass output Y_H of the 9/7 filter as:

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$$Y_H = \begin{bmatrix} g(0) & g(1) & g(2) & g(3) \end{bmatrix} \begin{bmatrix} r(1) \\ r(2) \\ r(3) \\ r(4) \end{bmatrix}$$

Where r(1)=x(1)+x(n-6), r(2)=x(n-1)+x(n-5), r(3)=x(n-2)+x(n-4),r(4)=x(n-3).
Let r(1)=1, r(2)=2,r(3)=3,r(4)=4 then

$$Y_H = \begin{bmatrix} 55 & -29 & -2 & 4 \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} = 7$$

Now if we implement this with NEDA then $Y_H = \begin{bmatrix} 55 & -29 & -2 & 4 \end{bmatrix} \begin{bmatrix} r(1) \\ r(2) \\ r(3) \\ r(4) \end{bmatrix}$

$$Y_H = \begin{bmatrix} 110111 & 100011 & 000110 & 000100 \end{bmatrix} \begin{bmatrix} r(1) \\ r(2) \\ r(3) \\ r(4) \end{bmatrix}$$

Now we can make the DA matrix by the filter coefficients as

$$[B_k] = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 0 \\ 1 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 \end{bmatrix}$$

And thus

$$Y_H = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 0 \\ 1 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} r(1) \\ r(2) \\ r(3) \\ r(4) \end{bmatrix} = \begin{bmatrix} r(1)+r(2) \\ r(1)+r(2)+r(3) \\ r(1)+r(3)+r(4) \\ 0 \\ r(1) \\ r(1)+r(2) \end{bmatrix}$$

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Table 1: Filter Coefficients of 9/7 Wavelet Filter.

	Coefficients	Multiplied by 100	6 bit binary representation with 2's complement of negative no.
h(0)	0.60294901823636	60	111100
h(1)	0.26686441184287	26	011010
h(2)	-0.07822326652899	-7	001001
h(3)	-0.01686411844287	-1	000011
h(4)	0.02674875741081	2	000010
g(0)	0.5575435262285	55	110111
g(1)	-0.29563588155713	-29	100011
g(2)	-0.02877176311425	-2	000110
g(3)	0.04563588155713	4	000100

Following the NEDA architecture in Fig. 1, the configuration for computing Y_H is illustrated in Fig. 2. As can be observed from this example, NEDA eliminates totally the encoder logic required in Booth Multiplier for two's complement manipulation. Furthermore, only one type of operations-addition, take place during the intermediate stages of computation, greatly simplifying hardware design. What needs special care is the sign output from the adder array, which is simply taking two's complement. In the above example, invert-and-add-1 is all one needs to convert "0011" to "1101=Y_{P4}

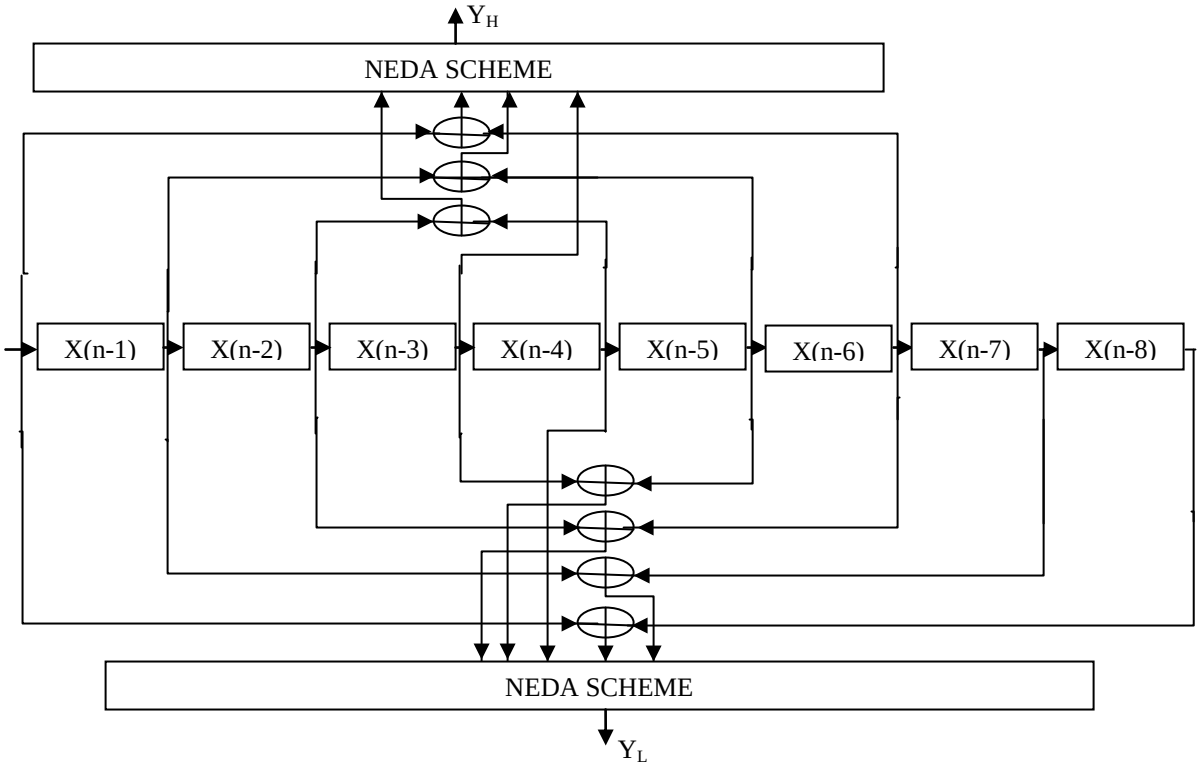

Figure 1: proposed Multiplier-less 9/7 Wavelet filter using NEDA Scheme

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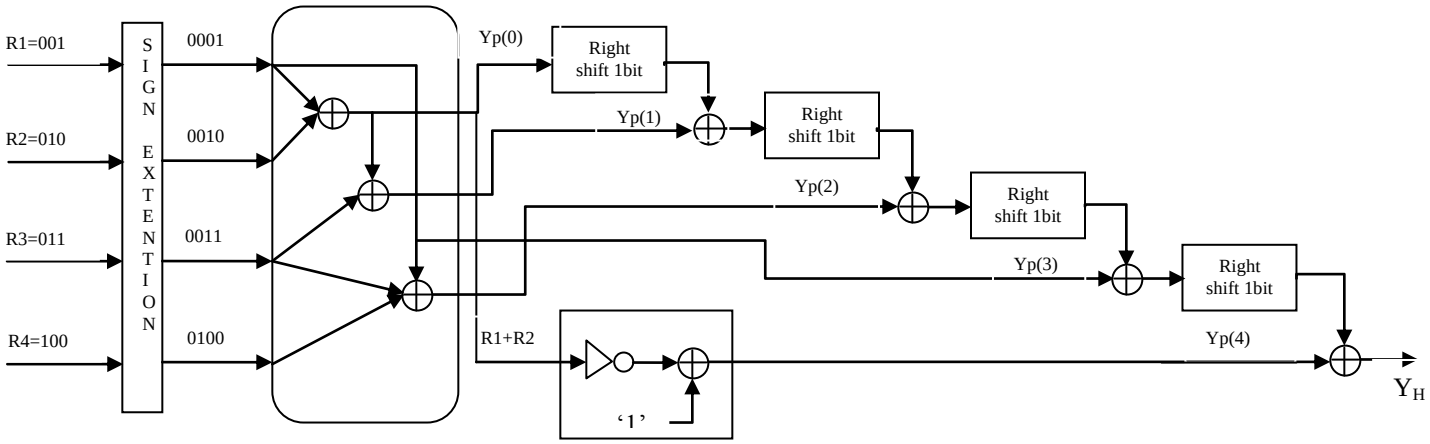

Figure 2 (a): Mathematical calculation of the NEDA Scheme of the High-pass Wavelet Filter Output

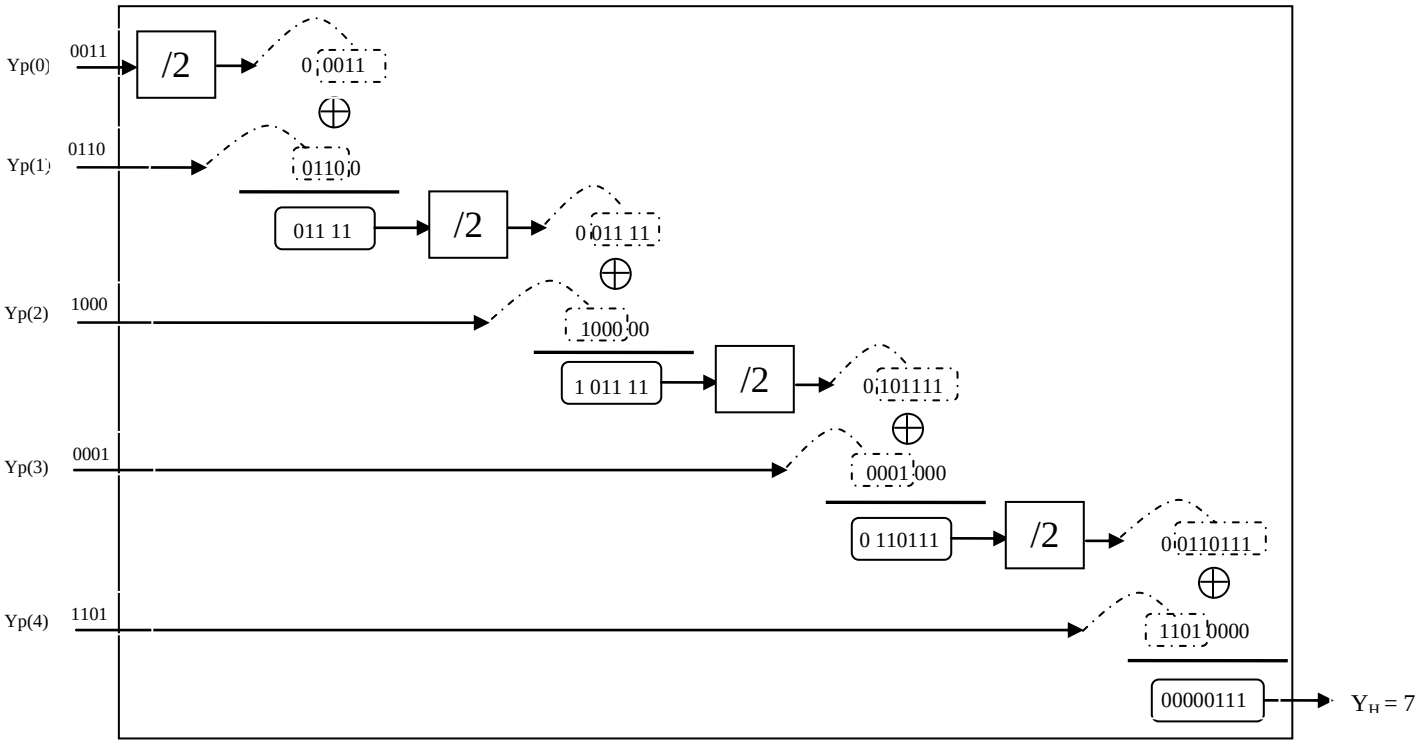

Figure 2 (b): Mathematical calculation of the NEDA Scheme of the High-pass Wavelet Filter Output

Figure 1: proposed Multiplier-less 9/7 Wavelet filter using NEDA Scheme

The proposed architecture has very low hardware complexity compared to DA based structures, because DA requires ROM. In the proposed architecture, calculate the high-pass and low-pass wavelet filter output using NEDA scheme. NEDA does not require ROM. Proposed structure consists only 29 adders, zero mux and 27 registers. In the proposed architecture is better than other architecture in shown the table 2. Implementation the Longa et al. [5] and proposed architecture has

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been captured by VHDL and the functionality is verified by RTL and gate level simulation. To estimate the timing, area and power information for ASIC design, we have used Synopsys Design Compiler to synthesize the design into gate Level. Comparison of Synopsys result in the DA based architecture and NEHA based architecture is given in Table 3.

Table 2: comparison of proposed with existing architectures

Structure	Adder	MUX	REG	CP
Alam *et al.* [1]	43	0	9	$6T_A$
Cao *et al* [2]	27	0	9	$6T_A$
Martina *et al* [4]	19	8	9	$6T_A$
Longa *et al* [5]	35	40	9	$6T_A$
Proposed	29	0	27	$6T_A$

Table 3: Comparison of DA based architecture and NEDA based architecture for 9/7 wavelet filter.

	Required time (n sec)	Power (µW)	Area (μm^2)	ADP (μm^2-sec)
Longa et al [5]	20.50	78.471	10572.45	216735.23
Proposed	19.80	43.314	9553.80	189165.24

V. CONCLUSION

We propose a novel distributed arithmetic paradigm named NEDA for VLSI implementation of DSP algorithms involving inner product of vectors. Mathematical proof is given for the validity of the NEDA scheme. We demonstrate that NEDA is a very efficient architecture with adders as the main component and free of ROM, multiplication, and subtraction. For the adder array, a systematic approach is introduced to remove the potential redundancy so that minimum additions are necessary. NEDA is an accuracy preserving scheme and capable of maintaining a satisfactory performance even at low DA precision.

In this paper, architecture suitable for high speed on-line applications. With this architecture the speed of the 9/7 wavelet filter transform is increased, occupied area of the circuit is reduced about 20-25% in the previous DA based architecture and reduced the power about 15-20% in the previous DA based architecture. It has 100% hardware utilization efficiency.

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