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Electrical Parameter Extraction Of High-K/Metal Gate N-Channel UTBB FDSOI MOSFET

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***Abstract*—**This Paper proposed a novel approach for obtaining and interpreting the better performance of NMOS with Ultra thin Body and BOX (UTBB) Fully Depleted Silicon on Insulator (FDSOI) technology. As the performance of FDSOI logic has already been reported, this paper highlights the extraction of electrical parameters by altering the dimensions and doping concentration of the device as per latest International Technology Roadmap for Semiconductors (ITRS) to obtain better results. Various technology options such as buried oxide thickness (BOX), Channel length and doping concentration were investigated in order to achieve a technology platform that offers controlling short channel effect to reduce the off-state leakage currents and to increase the on-state currents. The breakthrough technology brings a significant improvement in terms of performance and power management for VLSI Design.

***Keywords*—**UTBB FDSOI, BOX, Subthreshold Swing, Threshold Voltage

I. INTRODUCTION

Main challenges before us are scalability and variability. On continuous decreasing the channel length, short channel effects come into picture. Researcher tried strain engineering to boost mobility and explored channel doping. At high doping, although leakage reduces but variability increases. Everywhere there comes a point where these techniques become useless in order to scale down the device. In the continuation of technology SiO_2 as gate dielectric is replaced by high-k dielectric and poly-silicon as a gate material is replaced by metal gate [1].

After so many intellectual changing in the materials we end up with the solution to change in geometrical structure of transistor. UTBB FDSOI technology is a successful example of it. We have exhaustively presented its NMOS and analyzed on the basis of simulation. UTBB FDSOI with high-k/metal gate is a promising technology. The high-k dielectric reduces the gate leakage currents and good channel control allows reducing the drain leakage currents [2]. In conventional BULK technology V_T is depends on channel doping while in UTBB FDSOI technology V_T is adjusted by gate material and in this channel is kept un-doped. This V_T adjustment is done by either complex gate material or changing the doping of substrate with thin BOX.

II. SIMULATION CONDITION

The electrical characteristics of NMOS have been extracted from technology computer-aided design (TCAD) simulations based on an improved low-field mobility model including surface roughness and remote Coulomb scattering effects calibrated on experimental data [3].

The device presented in **fig. 1,** has 28nm gate length while Equivalent Oxide Thickness (EOT) is 2nm. They are composed of a High-K Metal-Gate stack (Cu) on a 7nm (t_{si}) thin SOI film with a 10nm (t_{BOX}) thin oxide (BOX). In general Source/Drain (S/D) doping is kept $1x10^{15}$ cm^{-3} while substrate doping level is $2x10^{18}$ cm^{-3}. HfO_2 is used for spacer and EOT [4][5].

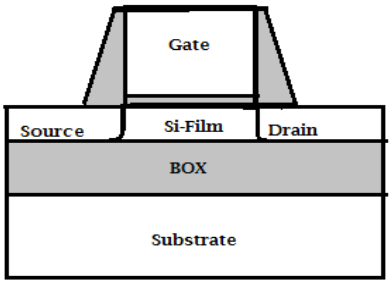


Fig. 1. Schematic of the FDSOI NMOS structure used in this work.

In conventional BULK technology, lateral Electric field coming from drain side effect the channel control which leads to overall degradation of device performance i.e. Sub-threshold slope (SS), Drain Induced Barrier Lowering (DIBL) and threshold voltage (V_T) .On the other hand UTBB FDSOI technology improves the channel electrostatic control. Therefore device

performance improves. Thickness of BOX and source/drain doping also plays an important role for performance of device. It is shown in fig. 2 and 3(a), respectively**.** Effect of power supply is also important to study. Therefore effect of supply voltage on drain current-gate voltage curve is also shown in fig. 3(b).

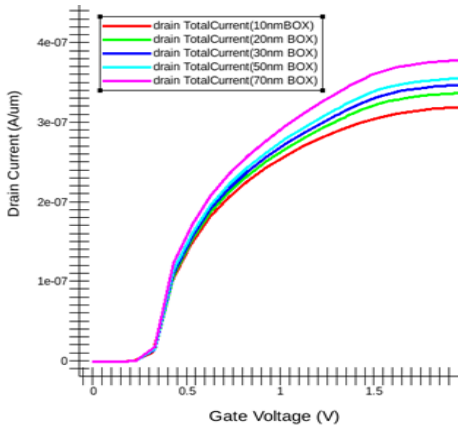


Fig. 2. Drain Current versus Gate Voltage for NMOS on various BOX thickness at $1x10^{15}$ cm^{-3} source/drain doping.

(a) (b)

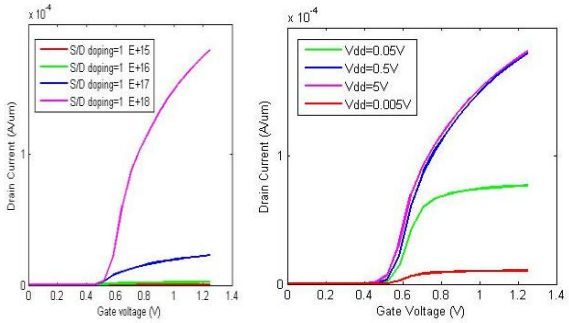


Fig. 3. Drain Current versus Gate Voltage for NMOS (a) at various doping level of source/drain and V_{dd}=0.5V (b) at various supply voltage (V_{dd}) and S/D=$1x10^{18}$ cm^{-3}.

III. Device Performance

As illustrated in Fig. 1, UTBB FDSOI has an un-doped silicon film of thickness T_{si} ~ 1/4 L_G. It also has thin BOX (10nm< T_{BOX}<30nm), covering a highly doped substrate [6]. For better understanding of concept regarding V_T and SS, we have shown curves at BOX ranging from 10nm to 70nm in Fig. 4(a), and Fig. 6(a). This device architecture helps in SCE and DIBL by reducing the source/Drain capacitance coupling to the channel.

TABLE I
ELECTRICAL CHARACTERISTICS OF UTBB FDSOI NMOS AT L_G =28 nm, BOX=10nm AND V_{DD}=0.5 V

S/D Doping	***I_{on} (A/μm)***	***I_{off} (A/μm)***	***V_T (mV)***	***SS (mV/dec)***
1E+15	$3.20x10^{-7}$	$2.61 x10^{-13}$	418	72.26
1E+16	$2.96x10^{-6}$	$5.57 x10^{-13}$	425	67.80
1E+17	$2.66x10^{-5}$	$6.53 x10^{-14}$	418	83.03
1E+18	$2.15x10^{-4}$	$8.10 x10^{-14}$	412	67.14
1E+19	$1.47x10^{-3}$	$2.02 x10^{-13}$	325	69.01

A. Threshold Voltage Charateristics

Fig. 4(a), describes the threshold voltage (extracted at specified current $10^{-7}/L_G$ (μm) and $V_{DS=}$0.5V) versus the BOX depth. It is seen clearly as the depth (or thickness) of BOX is increasing the threshold voltage is decreasing but in nonlinear fashion. Fig. 4(b), expresses the threshold voltage versus Source/Drain (S/D) doping concentration level for the device configuration defines in Table I. As S/D doping increasing, threshold voltage also decreases with it linearly.

(a) (b)

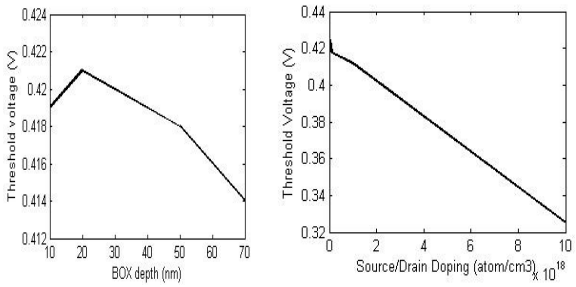


Fig. 4. Threshold Voltage versus (a) BOX depth at V_{DD}=0.5V and S/D doping= $1x10^{15}$ cm^{-3} (b) S/D doping at V_{DD}=0.5V and BOX=10nm.

Fig. 5, shows the electrostatic potential of the NMOS depicted on fig. 1. If Back Plane and well are added between BOX and substrate to perform multi V_T function then also electrostatic potential will remain same. Here, 1D cut have been extracted from the Si-film to the substrate near the drain side [7].

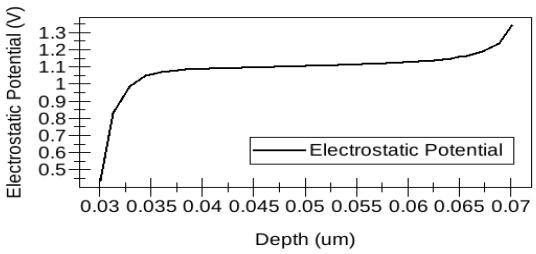


Fig. 5. Electrostatic Potential for UTBB FDSOI NMOS at L_G=28 nm, BOX=10nm AND V_{DD}=0.5 V

B. Subthreshold slope (SS) characteristics

(a) (b)

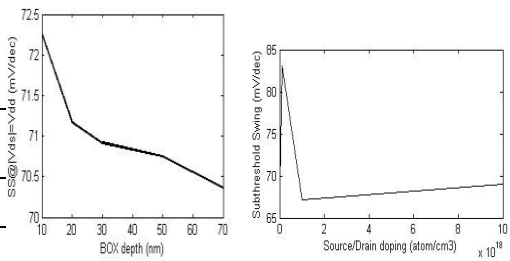


Fig. 6. SS versus (a)Box depth and (b)S/D doping at V_{DD}=0.5V

Fig. 6(a), shows the Sub-threshold slope, for UTBB FDSOI NMOS, versus BOX depth. It is clear by increasing the BOX

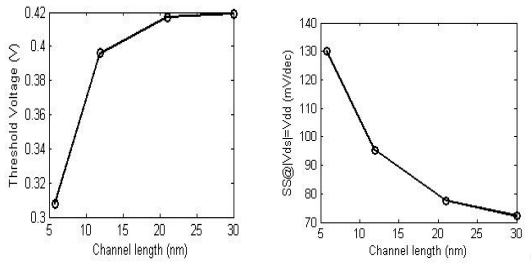
thickness, SS will reduce almost linearly. Fig. 6(b), describes SS variation with respect to change in S/D doping according to Table I. This property is quite random in nature.

C. Channel length

It is obvious from the Fig. 7(a), there will be increment in threshold voltage by increasing channel length. It is because as we keep on scale down the device, the value of drain current will decrease, which can be viewed as due to a decrease in the effective threshold voltage. In short channel, the charge in the channel region is influenced by field lines emanating from all nearby structures [8].

Fig. 7(b), shows that sub-threshold slope will also decrease as on increasing of channel length. SS value reduces almost in a linear manner.

(a) (b)



(b)Fig. 7(a). Threshold Voltage versus channel length (b) Sub-threshold Slope versus channel length. At V_{DD}=0.5V, S/D doping= 1x10^{15} cm^{-3} and BOX=10nm.

IV. CONCLUSION

In this paper, exhaustive analysis of UTBB FDSOI architecture has been presented. The effect on SS and threshold voltage has been studied for various design and technology options, such as BOX thickness, source/drain doping, drain voltage and channel length. We can conclude by saying UTBB FDSOI technology is particularly suited for LP SOC products for mobile multimedia applications and being beyond reach of any conventional technology. We have demonstrated its scalability. At the same time, UTBB remains planer and requires fewer process steps than any bulk technology.

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