

FPGA Based Digital Controller for DC-DC Buck Converter

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ABSTRACT: This paper presents performance analysis of Digital PWM control mode in DC-DC buck converter in terms of power efficiency, line regulation and load regulation. Matlab/Simulink Models are built to facilitate the analysis of various effects on power loss and conversion efficiency, including different load conditions. It introduces a fully synthesizable hybrid digital pulse width modulator (DPWM) utilizing Σ - Δ modulation technique to achieve best possible resolution of 12 bit. A type-II compensator is designed for the buck converter in order to achieve a stable closed loop operation with desired performance. FPGA implementation is carried out for both type-II compensator and DPWM using Xilinx system generator tool. A load regulation of 4% with a response time of 200us is achieved for a load change of 0.4A to 0.8A. A line regulation of 2% with a response time of 100us is achieved for a line voltage change of 3 to 4.5V. A Graph of conversion efficiency versus load current is obtained.

KEYWORDS: Buck Converter, Digital Pulse Width Modulator (DPWM), Field Programmable Gate Array (FPGA), Proportional Integral Derivative (PID), Sigma Delta (Σ - Δ) modulator, Switch mode power supply (SMPS).

I. INTRODUCTION

DC-DC converters are one of the most important electronic circuits, which are widely used in regulated SMPS, dc motor drive applications and portable electronic devices such as laptops, mobile phone, camera etc. With the improvement of various performances of portable devices, the power consumption corresponding to it rises rapidly but the battery technology doesn't. A DC-DC converter which is able to keep high efficiency through the entire range to extend the stand-by time and the battery using time is preferred. Therefore, high conversion efficiency and a stable output voltage irrespective of variation in load current or input voltage becomes the crucial parameter to design the DC-DC converter for low voltage and low power applications.

Fig. 1 shows digitally controlled buck converter. There are four functional blocks namely buck converter, analog to digital converter (ADC), digital PID controller and digital pulse width modulation (DPWM). The output of the converter i.e. V_{out} is compared with reference voltage and the error voltage is fed to the ADC block where the analog signal is converted into digital signal. The digitalized signal is fed to the PID compensator which is a type-II compensator and it creates a control signal for DPWM. The PWM pulses are generated by DPWM, which is given to the MOSFET switches.

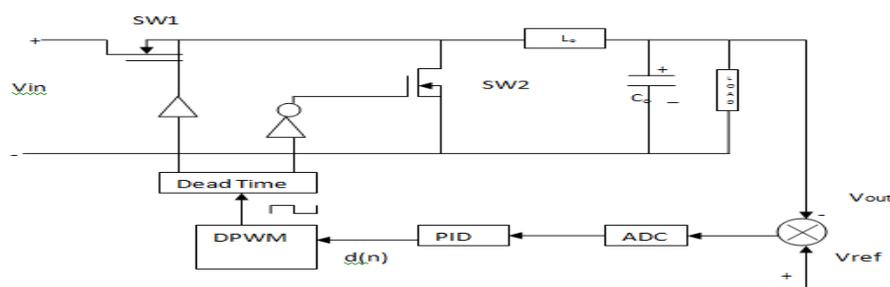


Fig 1. Block diagram of digitally controlled buck converter

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This paper describes the Design a DC-DC Buck Converter for low voltage, low power applications. A digital type-II compensator and a high resolution DPWM based on $\Sigma-\Delta$ modulation technique is designed and implemented on FPGA using Xilinx system generator tool. Power efficiency, line regulation and load regulation of digitally controlled buck converter is determined and analyzed. Section II reviews related work carried out in the field of digital control of DC-DC buck converter. Section III discusses the system architecture of type-II compensator and DPWM. Section IV analyzes various PWM power losses and its efficiency. Section V shows simulation and hardware co-simulation results using Xilinx system generator. Section VI summarizes main results of this paper.

II. RELATED WORK

In [1], a fully synthesizable hybrid digital pulse width modulator (DPWM) is introduced. The DPWM includes a digital delay locked loop around a delay-line with discretely programmable delay cells to achieve constant-frequency clocked operation over a range of process or temperature variations. It includes two outputs with programmable dead-times, suitable for DC-DC converters. It is carried for a switching frequency of 780 KHz, 10-bit FPGA realization. An integrated digital controller for DC-DC switch mode power supplies (SMPS) used in portable applications is introduced in [2]. The SMPS has very low power consumption, fast dynamic response, and can operate at constant switching frequencies In steady state, to minimize power consumption, the controller is clocked at a frequency lower than SMPS switching frequency. During transients the clock rate is increased to the switching frequency improving transient response. The controller integrated circuit is fabricated in a standard 0.18m process and tested with a 750-mW buck converter prototype. The work mentioned in [3] proposes the design of a 2 bit segmented hybrid DPWM featuring a counter with segmented delay lines and tunable digital PID controller for digital DC-DC converters using AMS 0.35J1m CMOS process. Design of digital PID regulator based on look-up tables for high frequency DC-DC switching converters is proposed in [4]. The use of the look-up tables instead of multipliers enables a small low-power implementation and operation at high switching frequencies.

III. SYSTEM ARCHITECTURE

A. Type II Compensator Design:

Fig.2 shows block diagram of PWM mode Synchronous buck converters. The power stage ($G_p(s)$) includes the switches, drivers and the output inductor and capacitor. The model of the PWM generator is simply $1/V_{osc}$, where V_{osc} is the peak to peak amplitude of the oscillator voltage. The compensator block ($H(s)$) represents the error amplifier with the compensation network[5,6].

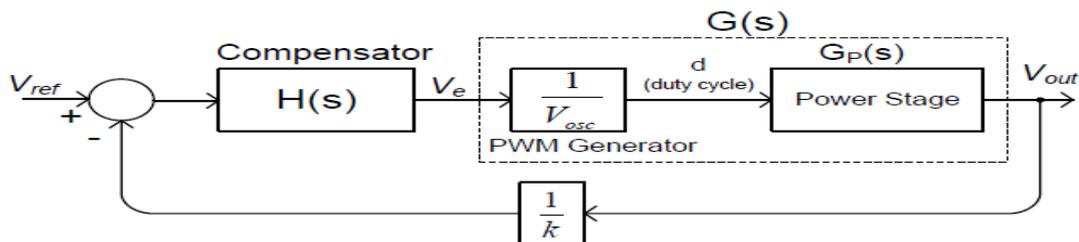


Fig 2. Block diagram model of PWM mode synchronous buck converter

The transfer function of power stage $G_p(s)$ is given by:

$$G_p(s) = \frac{V_{out}}{d} (s) = \frac{R_{load} (C_o \cdot ESR \cdot s + 1)}{L_o C_o s^2 (R_{load} + ESR) + s \cdot (L_o + R_{load} \cdot C_o \cdot ESR) + R_{load}} * V_{in} \quad (1)$$

The transfer function of PWM generator and power stage can be combined as follows:

$$G(s) = G_p(s) \cdot \frac{1}{V_{osc}} \quad (2)$$

The transfer function of the power stage is a second order system with a double pole at the resonance frequency (LC filter) and a zero produced by the ESR of the output capacitor. To have a stable closed loop buck converter with

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appropriate performance, a properly designed compensator is required. In this paper Type-II compensator is designed. The typical procedure of the Type-II compensator is as follows:

Step 1- Collect the system information such as input and output voltage and the switching frequency.

Step 2-Determine the power stage poles and zeros as given by (3) and (4):

$$F_{LC} = \frac{1}{2\pi\sqrt{L_0 C_0}} \quad (3)$$

$$F_{ESR} = \frac{1}{2\pi \cdot ESR \cdot C_0} \quad (4)$$

Step 3-Select crossover frequency to be 1/5 of the switching frequency.

Step 4-Select the type of compensator. Since, $F_{LC} < F_{ESR} < F_0 < F_s/2$, Type II compensator is selected in the presented work.

Step 5-Calculate the poles and zero of the compensator where the compensator has a pole at the origin and another pole and one zero as provided by Eq.(5) and (6):

$$F_{z1} = 0.75 \times F_{LC} \quad (5)$$

$$F_{p2} = F_s/2 \quad (6)$$

Step 6- Find the compensator transfer function.

B. DPWM Architecture

A high resolution DPWM is necessary to accomplish precise output voltage and avoid limit-cycle oscillations. In order to increase resolution and reduce power consumption simultaneously, several hybrid methods are utilized. Here as in fig.3, the 12-bit DPWM structure consists of 7-bit second-order $\Sigma-\Delta$ modulator block and 5-bit counter-comparator block.

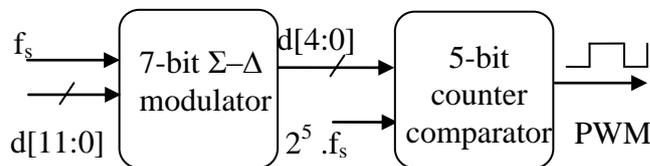


Fig 3. Structure of Proposed DPWM Architecture

i)Fast Counter Comparator Block

It is one simple hardware method to achieve digital-to-time conversion in core DPWM .It needs $2^N \cdot f_s$ clock to achieve an N-bit DPWM at switching frequency f_s . Disadvantage of this method is when operating at the high frequency , there will be very high power consumption. Fig.4 shows the structure of fast counter-comparator DPWM.

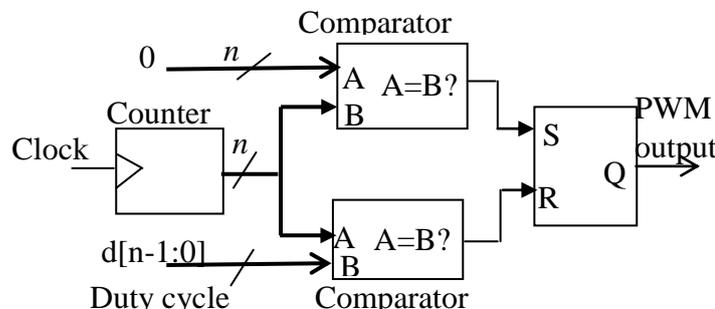


Fig 4. Fast-clocked counter-comparator of DPWM

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ii) Sigma-Delta (Σ - Δ) Modulator

It is based on the well-known noise-shaping concept which can be fabricated in low cost CMOS technologies. Fig.5 shows a general Single Stage Σ - Δ Modulator. Loop filter is to process the input signal by noise shaping mechanism, E is the noises, Q is the quantizer and V is the output signal. Fig 6. Shows the Z-domain Representation of First Order Σ - Δ Modulator.

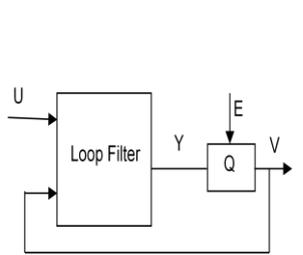


Fig 5. Single Stage Σ - Δ Modulator

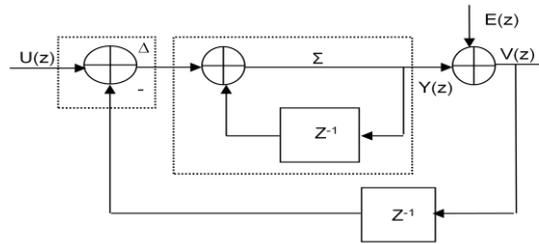


fig 6. Z-domain Representation of First Order Σ - Δ Modulator

From Fig.6,

$$Y(z) = z^{-1}Y(z) + U(z) - z^{-1}V(z)$$

$$V(z) = Y(z) + E(z)$$

$$V(z) = U(z) + (1 - z^{-1})E(z)$$

$$V(z) = \text{STF}(z) \cdot U(z) + \text{NTF}(z) \cdot E(z).$$

Under steady state conditions Σ - Δ loop, has infinite gain at zero frequency ($z \approx 1$). Hence $\|\text{NTF}\| \ll 1, \|\text{STF}\| \approx 1, V(z) \approx U(z)$. The quantization error is suppressed. The output PWM signal becomes approximately equal to input PWM signal. In this paper a second order error feedback type Σ - Δ modulator is utilized (Fig.7).

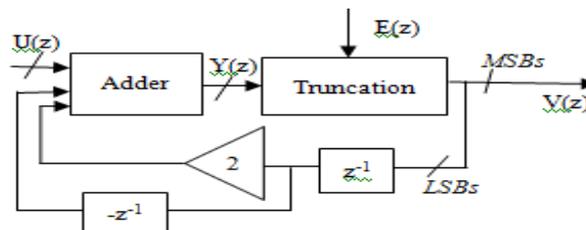


Fig 7. A second order error feedback implementation of Σ - Δ modulator

IV. PWM POWER LOSS ANALYSIS

In a DC-DC converter, the losses can be classified into two types: load dependent conduction losses and frequency dependent switching losses.

1. Conduction losses:

During the continuous conduction mode where the load current is relatively large, the main contribution of power losses are the conduction loss of the on-resistance of high-side (R_{on_PFET}) and low-side (R_{on_NFET}) switches and the series resistance of the inductor and capacitor (R_L, R_{ESR}) [7]. When in operation the upper path and lower path switches are turned on and off depending on the duty cycle. Hence, the average resistance for these switches can be expressed as the on resistance multiplied by the duty cycles. The on-resistance in one switching cycle can be written as:

$$R_{switches_on} = R_{on_PFET} * D + R_{on_NFET} * (1 - D) \quad (7)$$

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The conduction loss due to on-resistance inside the MOSFET

$$P_{switches_on} = [R_{on_PFET} * D + R_{on_NFET} * (1 - D)] I_{out}^2 \tag{8}$$

Non-ideal inductor has series resistance consuming extra power when passing through current. In steady-state the average inductor current is also the same as the load current. The power loss due to inductor can be written as:

$$P_L = R_L * (I_{load} + \Delta I_{inductor} * \sqrt{2})^2 \tag{9}$$

Where R_L is inductor resistance, I_{load} is the load current and $\Delta I_{inductor}$ is the inductor current variation.

For capacitor, ESR is the main cause for power loss and is given as:

$$P_C = (\Delta I_{inductor} * \sqrt{3})^2 * R_{ESR} \tag{10}$$

2. Switching Losses:

Switching losses are frequency dependent losses. As the transistor switches on and off the current of the transistor cannot change simultaneously. Thus, the voltage across drain and source of the MOSFET and the current flowing from drain to source would have a time window during which voltage and current are nonzero. Thus, hard switching power loss of a switch can be written as [8]:

$$P_{SWITCHING} = 0.5 * V_{IN} * I_{LOAD} * [T_{OFF} + T_{ON}] * F_s \tag{11}$$

V. SIMULATION RESULTS

The proposed digitally controlled buck converter is tested for $V_{in} = 3.6V$, $V_{out} = 1V$, $I_{out} = 1A$, $F_s = 3MHz$. The values of inductance (L_0) = $4.7\mu H$, capacitance (C_0) = $18\mu F$, $R_L = 30m\Omega$ and Equivalent Series resistance of capacitor, $ESR = 2m\Omega$, $R_{load} = 1\Omega$ are considered for simulation. Fig 8 shows Simulink model of digital voltage mode buck converter .

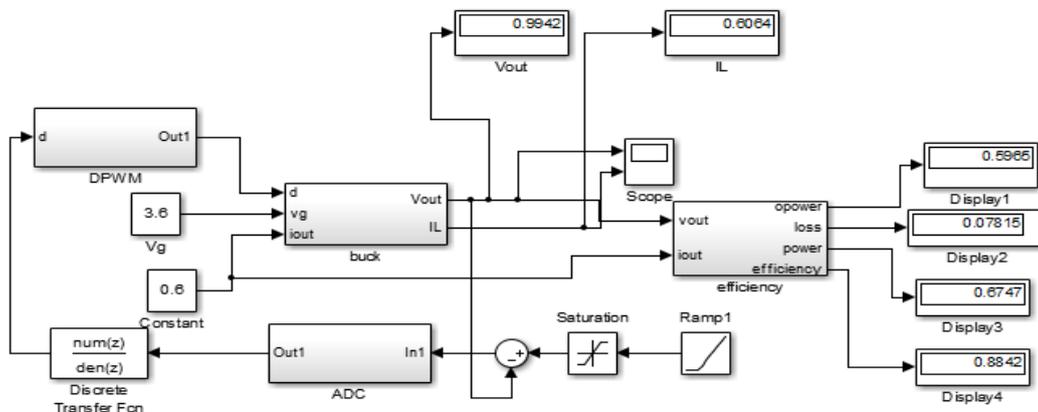


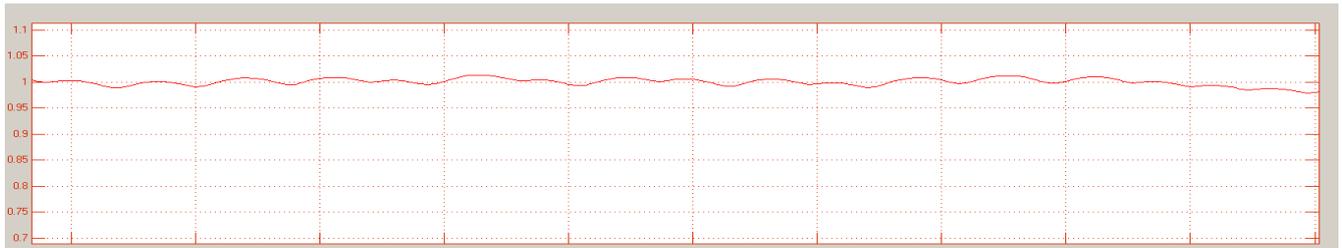
Fig 8. Simulink model of digital voltage mode buck converter

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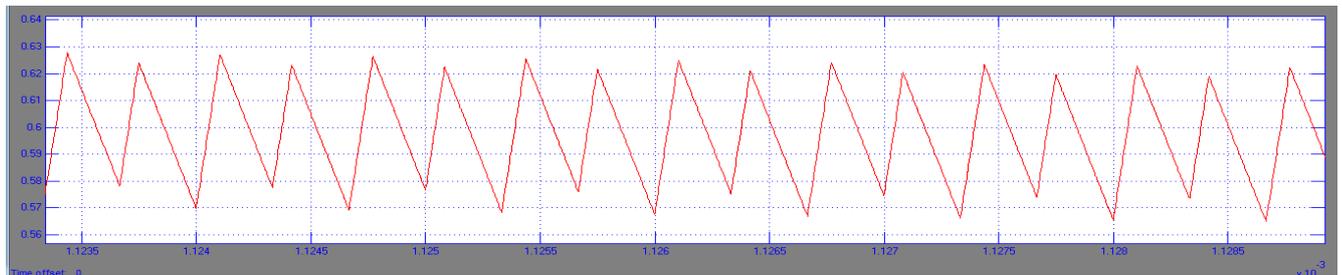
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Fig.9 shows the simulation results of output voltage and inductor current. An voltage ripple of 0.25% and current ripple of 10% is obtained which found to be satisfactory.



(a)



(b)

Fig 9.Simulation results average inductor current of digital voltage mode buck converter (a)Output Voltage(b)Average Inductor Current.

The digital Type II compensator, 12 bit $\Sigma-\Delta$ DPWM are implemented on ML605 board with the XC6VLX240T-1FFG1156 FPGA. The Xilinx system generator environment allows for Xilinx line of FPGAs to be interfaced with simulink. The hardware co-simulation is performed to validate the design operating on the ML605 board with the XC6VLX240T-1FFG1156 FPGA.A Simulink library is created containing the hardware co-simulation block, which replaces the previously used System Generator simulation blocks. The hardware implementation is then executed by connecting the board to the PC, thereby, closing the loop. The Xilinx ISE program then generates the bit file and loads it into FPGA through a standard JTAG connection. Fig. 10 shows the hardware-software co-simulation model of digital controller.

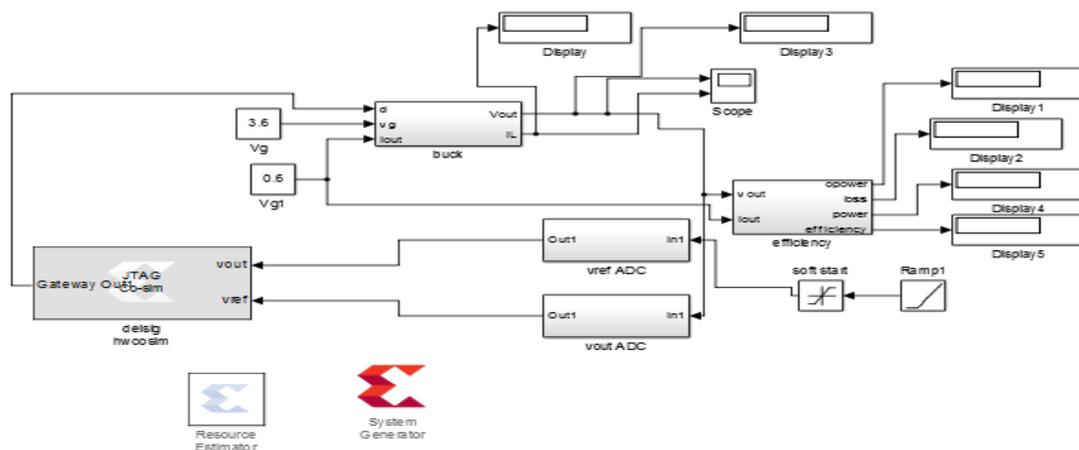


Fig 10. Hardware - Software Co-simulation model of digital controller

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Fig.11 shows the hardware-software simulation results of output voltage and inductor current. An voltage ripple of 0.5% and current ripple of 20% is obtained which found to be slightly higher than that obtained in simulink. But it is justified as it represents hardware results.

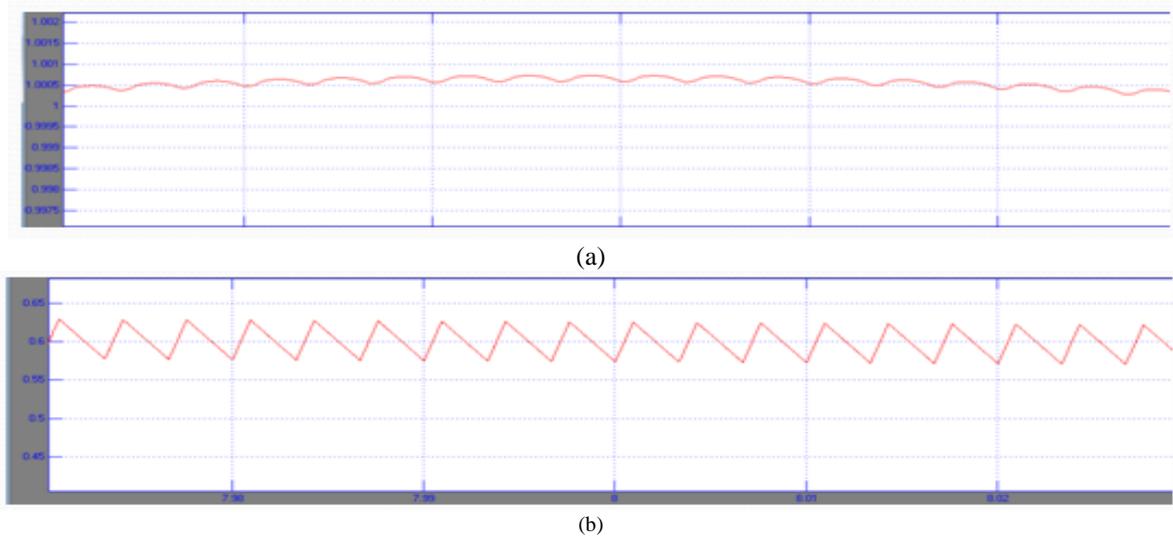


Fig 11. (a)Output Voltage (b)Average Inductor Current of DPWM mode buck converter(FPGA)

Efficiency analysis is carried out for varying load current(0.0001mA-1A) and maximum conversion efficiency of 89.91% is obtained. Fig.12 shows the plot of efficiency versus load current.

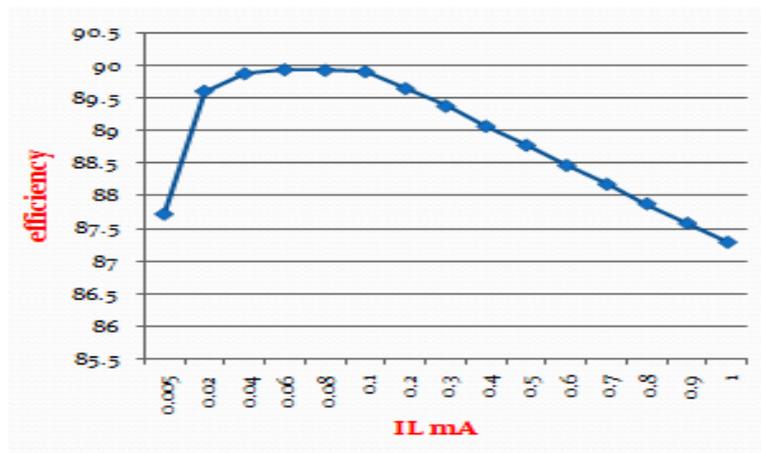


Fig 12.Plot of efficiency versus varying load current

Dynamic performance of the buck converter is analyzed by considering load and line regulation. Load regulation has an undershoot voltage of 4% having settling time 200us when load current is varied from 0.4 to 0.8A(Fig.13), where as Line regulation has an overshoot voltage of 2% having settling time 100us when line voltage is varied from 3 to 4.5V(Fig.14).

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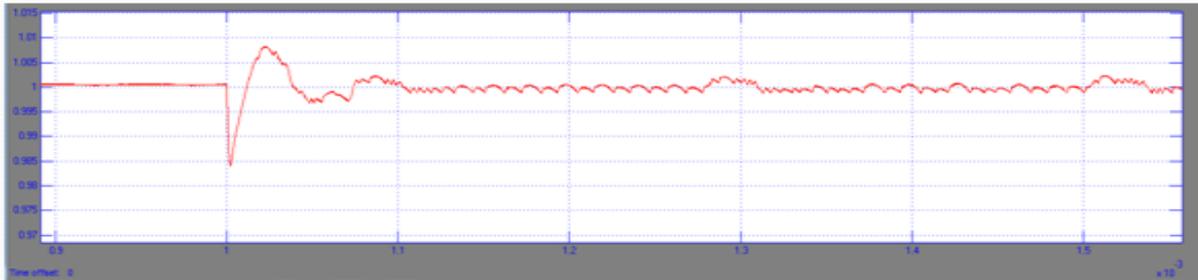


Fig 13. Output voltage when load current is changed from 0.4A to 0.8A

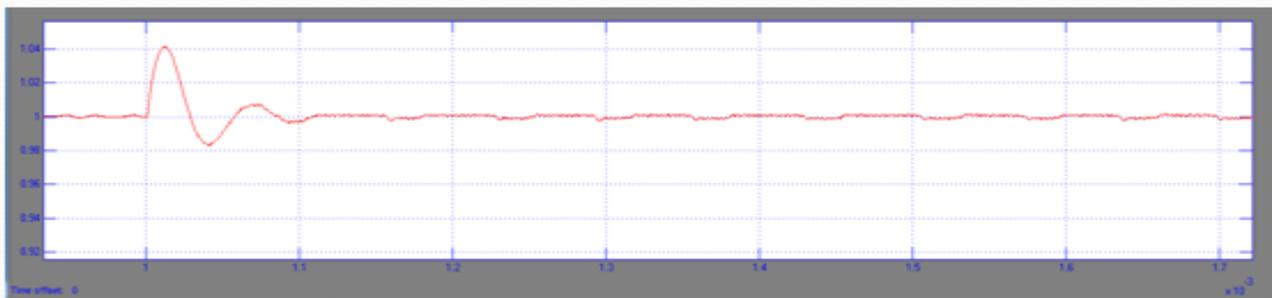


Fig 14. Output voltage when line voltage is changed from 3V to 4.5V

VI. CONCLUSION AND FUTURE WORK

FPGA prototype digital controller is implemented for high-frequency low-power DC-DC buck converter. 12 bit Σ - Δ DPWM and Type-II compensator are implemented on FPGA using Xilinx system generator. The Σ - Δ DPWM combines a counter-comparator block with a second order Σ - Δ modulator. It can achieve an equivalent 12-bit DPWM resolution using a 5-bit counter-comparator, which reduces the high clock frequency from $2^{12} \cdot f_s$ to $2^5 \cdot f_s$. A load regulation of 4% with a settling time of 200us and a line regulation of 2% with a settling time of 100us is achieved. A theoretical maximum conversion efficiency of 89.91% is obtained.

It is observed that for low load current, efficiency reduces below 60%. Hence DPFM/PSM technique can be designed at light load condition to improve the power efficiency. A combination of DPWM and DPFM/PSM technique can be used to have high efficiency over a wide load current range.

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