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FPGA Implementation of Multiply Accumulate (MAC) Unit based on Block Enable Technique

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ABSTRACT: Power dissipation is one of the most important design objectives in integrated circuit, after speed. Digital signal processing (DSP) circuits whose main building block is a Multiply Accumulate (MAC) unit. High speed and low power MAC unit is desirable for any DSP processor. This is because speed and throughput rate are always the concerns of DSP system. This paper explores the design of low power MAC unit with block enable technique to reduce power dissipation. The whole MAC unit is implemented using 90-nm CMOS process technology. The whole MAC unit is operated at 314.268MHz with 1.5V supply voltage. The result analysis shows that the power consumption is reduced by using block enable technique.

KEYWORDS: MAC; block enable; adders; low power; multipliers

I. INTRODUCTION

Due to rapid growth of portable electronic systems like laptop, calculator, mobile etc., and the low power devices have become very important in today's world. Low power and high throughput circuitry design are playing the challenging role for VLSI designer. For real-time signal processing, a high speed and high throughput MAC unit is always a key to achieve a high performance digital signal processing system [1]. The main motivation of this work is to investigate various pipelined multiplier/accumulator architectures and circuit design techniques which are suitable for implementing high throughput signal processing algorithms and at the same time achieve low power consumption. A regular MAC unit consists of multipliers and accumulators that contain the sum of the previous consecutive products. The function of the MAC unit is given by the following equation $F = \Sigma Ai X Bi$.

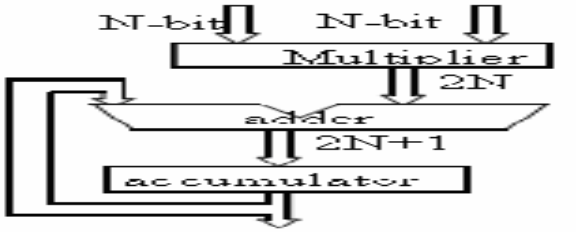

Fig. 1. Basic structure of Multiply Accumulate unit [1]

II. RELATED WORK

F.Lu et al.,[3]proposed a bit-level pipelined 12 x 12 two's-complement multiplier with a 27 bit accumulator designed and fabricated in a 1.0 µm p-well CMOS technology. A new "quasi N-P domino logic" structure has been adopted to increase the throughput rate and special pipeline structures were used in the accumulator to reduce the total latency. The chip complexity is approximately 10000 transistors and the die area is 2.5 x 3.7 mm. The measured maximum clock rate is 200 MHz (i.e., 200 million multiply-accumulate operations per second) and the power-speed ratio is 6.5mW-1MHz. A unique output buffer design was also adopted to achieve 200-MHz off-chip communication while maintaining full CMOS logic levels.

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Ashish B. Kharate et al.,[4]proposed the design and implementation of Finite Impulse Response (FIR) filter using a low power MAC unit with clock gating and pipelining techniques to save power.In the majority of digital signal processing (DSP) applications the critical operations are the multiplication and accumulation. Multiply-Accumulate unit that consumes low power is always a key to achieve a high performance in digital signal processing system. Finite impulse response (FIR) filters are widely used in various DSP applications.

Shanthala S et al.,[5] proposed the design and implementation of low power MAC unit with block enable technique. Firstly, a 1-bit MAC unit is designed, with appropriate geometries that gives optimized power, area and delay. The delay in the pipeline stages in the MAC unit is estimated based on which a control unit is designed to control the data flow between the MAC blocks for low power. Similarly, the N-bit MAC unit is designed and controlled for low power using a control logic that enables the pipelined stages at appropriate time. The adder cell designed has advantage of high operational speed, small transistor count and low power. The MAC is implemented on a 0.18um CMOS technology using CADENCE VIRTUOSO tool. Ripple Carry Adder (RCA) is mainly used as an accumulator in the design. This paper also investigates on various architectures of multipliers and adders which are suitable for implementation of high throughput signal processing and at the same time to achieve low power consumption. The whole MAC chip is operated at 125 MHz using 1.8 V power supply. The power is reduced by 27% using the block enabling technique compared to the normal design.

Vaijyanath Kunchigi et al.,[6]proposed Multiply and Accumulate (MAC) unit design using Vedic Multiplier, which is based on Urdhva Tiryagbhyam Sutra. The paper emphasizes an efficient 32-bit MAC architecture along with 8-bit and 16-bit versions and results are presented in comparison with conventional architectures. The efficiency in terms of area and speed of proposed MAC unit architecture is observed through reduced area, low critical delay and low hardware complexity. The proposed MAC unit reduces the area by reducing the number of multiplication and addition in the multiplier unit. Increase in the speed of operation is achieved by the hierarchical nature of the Vedic multiplier unit. The proposed MAC unit is implemented on a field programmable gate array (FPGA)device,3S100ETQ144-5 (Spartan 3). The performance evolution results in terms of speed and device utilization are compared to earlier MAC architecture. Though the use of Vedic mathematics methods for multiplication is reported in literature, it has been observed that the proposed method of 32-bit MAC unit implementation is using (32X32) multiplication unit and shows improvements in the delay and area.

III. PROBLEM DESCRIPTION

The traditional multiplier as array multiplier, booth multiplier, parallel multiplier etc., consumes more area and could not meet the criteria of propagation delay. This problem will affect high end processors. This has been overcome in this project by making use of Wallace tree multiplier which is much faster with minimum propagation delay. The usage of adders such as Carry Save Adder (CSA) and Carry Look Ahead (CLA) adder helps to reduce time delay with increase in speed.

IV. PROPOSED SYSTEM

A. MAC Architecture:

Multiply Accumulate (MAC) unit consists of multiplier, adder and an accumulator. For high speed MAC unit, faster adder and multiplier circuits are required. The inputs for the Multiply Accumulate (MAC) unit are fetched from memory location and fed to multiplier block of the MAC, which will perform multiplication and give the result to adder which will accumulate the result and then will store the result into a memory location. The design of MAC unit architecture from fig. 2 shows that the design consists of one register, one 8-bit Wallace tree multiplier, accumulator using carry save adder (CSA) and two accumulator register are used.

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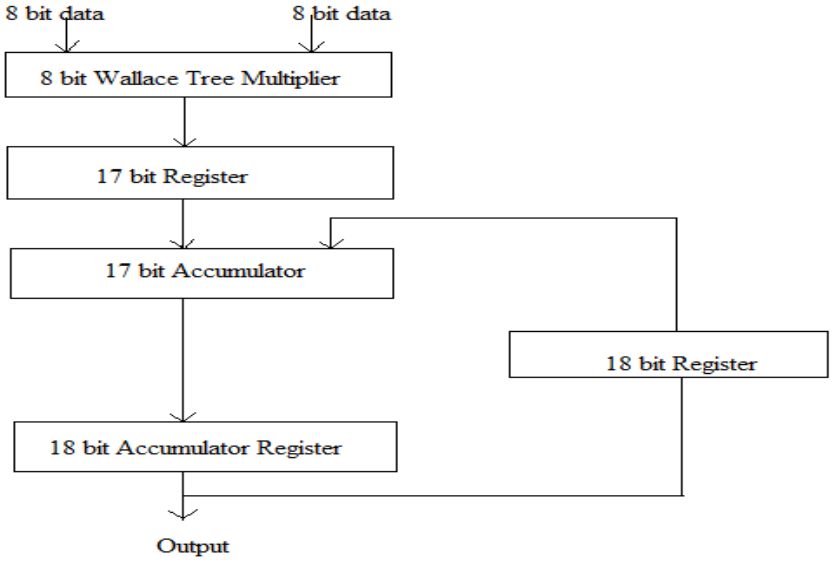

Fig. 2. Multiply Accumulate unit architecture

In this project, Wallace tree multiplier and carry save adder are used to get high performance MAC unit design. Wallace tree multiplier is used to multiply the values of A and B. Carry save adder (CSA) used in the final stage of the given multiplier for reducing power consumption of the MAC unit. The product of Ai X Bi is always fed back into the accumulator and added again with the next product Ai X Bi. This MAC unit is capable of multiplying and adding with the previous product consecutively. Output = ΣAi X Bi.

B. Wallace Tree Multiplier:

The design analysis starts with the analysis of elementary algorithm for multiplication by Wallace tree multiplier. Fig. 3 shows the algorithm for 8 x 8 bits multiplication performed by Wallace tree multiplier. There are five stages to go through, to complete the multiplication process [2]. Each stage used half adders and full adders that are denoted by the red circle for the 1bit half adder and the blue circle for the 1 bit full adder. Firstly, we had to reduce the partial products using the half adders and full adders that are combined to build a carry save adder (CSA) until there were just two rows of partial products left and Carry Save Adder is used to get the final products. Next, we add remaining two rows by using a Carry Propagate Adder (CPA).

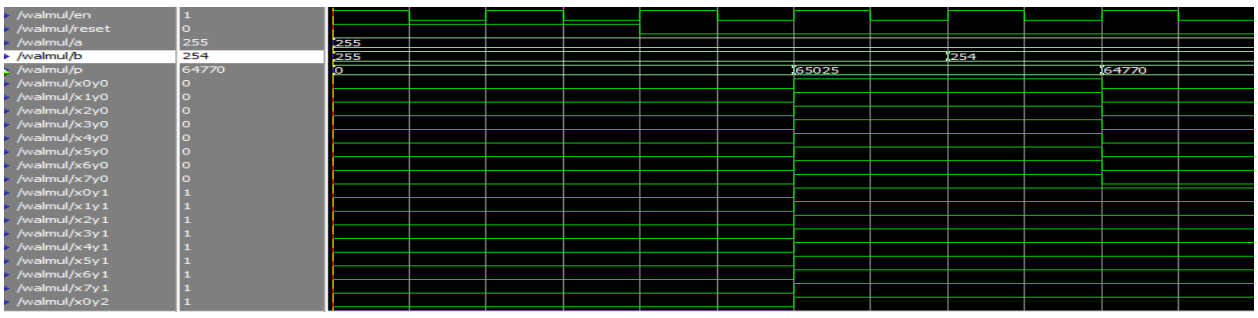

Fig. 3.Algorithm for 8 bits x 8 bits Wallace tree multiplier

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C. Block Enable Technique:

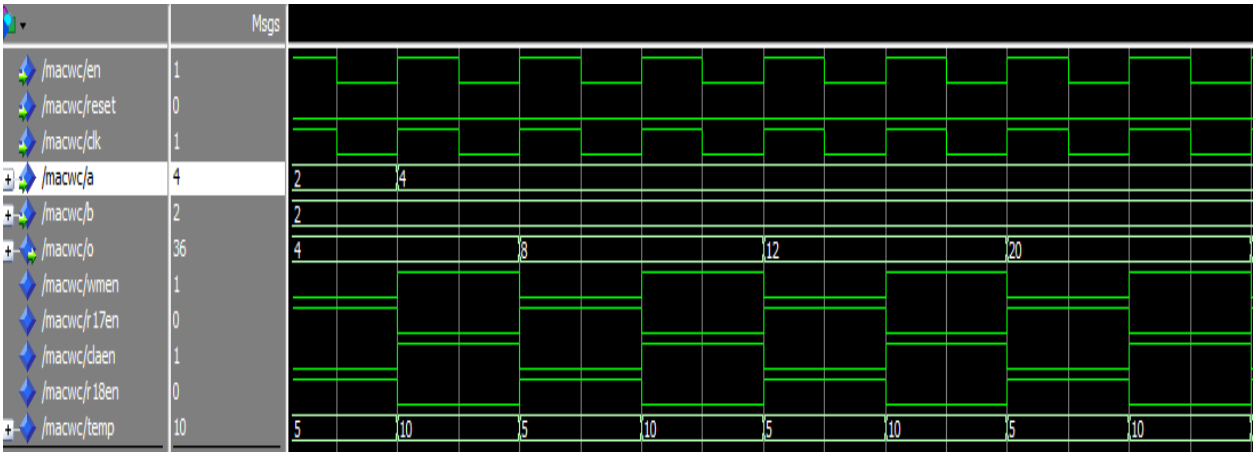

Fig. 4. Block diagram of a pipeline MAC with block enable technique

The input registers pass the data to the multiplier. Within multiplier stage, there are multiple stages of addition. During each operation of multiplication and addition, the blocks in the pipeline may not be required to be on or enabled until the actual data gets in from the previous stage. First we find out delay for each stage in block enable technique. Every block gets enabled only after the expected delay. The successive blocks are disabled until the inputs are available. This technique saves the power.

V. RESULTS AND DISCUSSION

i. Simulation results:

A. Simulation result of MAC with Block Enable Technique

Fig. 5 shows the simulation result of MAC unit with block enabling technique where in the data flows from the input register to the output register through multiple stages such as multiplier stage, adder stage and the accumulator stage only when each block is enabled.

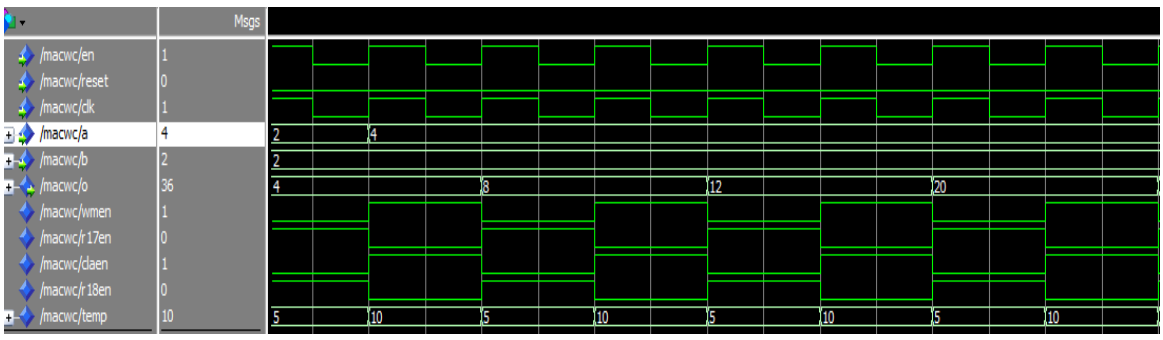

Fig. 5. Simulation result of MAC with Block Enable Technique

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B. Simulation result of 8 x 8 bits MAC unit

Fig. 6 shows the simulation result of 8 x8 bits MAC unit where there is no control signal to enable each block. This performs the normal MAC unit operation without pipeline method enabling each block whenever the user is in need.

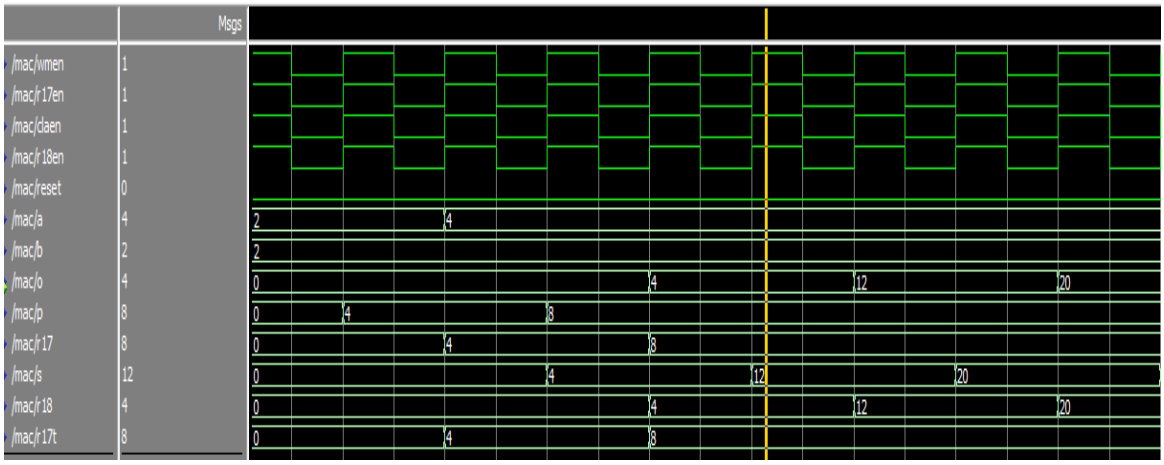

Fig. 6. Simulation result of 8 x8 bits MAC unit

ii. Power comparison :

Table 1: Comparison of power between MAC with block enable technique and 8x 8 bits MAC unit

Description	Power(Watt)
MAC with block enable technique	0.056
8 x 8 bits MAC unit	0.076

VI. CONCLUSION AND FUTURE WORK

In this project, the design of 8X8 bits MAC unit has been implemented using block enable technique to reduce the power consumption. This MAC unit has 18 bit output and its operation is to add repeatedly the multiplication results. All the basic blocks of MAC unit are identified and analyzed through its performance. The improvements achieved in low power consumption of the MAC unit can be used in high speed DSP applications. This dissertation work can be extended to the implementation of multiply accumulate operation on signed numbers as well as complex numbers. In the future work some circuit optimization and leakage reduction techniques can be used to reduce the power dissipation and area occupied. Some technique such as Spurious Power Suppression Technique (SPST) can be applied on multipliers for high speed and low power purposes. The analysis of low power multiply accumulate unit can be applied with pixel properties reusability technique for image processing systems.

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BIOGRAPHY

Tasmiya Shaikh, working as an Assistant Professor in Electronics and Communication department of Anjuman Institute of Technology and Management , Bhatkal from the year 2015.She received M.Tech degree in VLSI Design and Embedded Systems from Nagarjuna College of Engineering and Technology, Bangalore in the year 2014 and BE in Electronics and Communication from Vivekananda College of Engineering and Technology, Puttur in the year 2011.Her area of interest include low power VLSI design.

Manjunatha Beleri, working as a Telecommunication Engineer in Dar Al-Handasah Consultants India Pvt.Ltd.,Pune from 2015. He possessed M.Tech in VLSI Design and Embedded Systems from Nagarjuna College of Engineering and Technology,Bangalore in the year 2012 and BE in Electronics and Communication from R.L Jallappa Institute of Technology, Bangalore in 2010.He worked for two years as an Assistant Professor in ECE department of Nagarjuna College of Engineering and Technology, Bangalore from 2012-14.He also worked as Project Trainee for one year in ISRO Satellite Center Bangalore (Control System Group) and as Service Engineer in UPS field of Power One Microsystems Pvt.Ltd, Bangalore from the year 2005-07.His areas of interest include CMOS RF design, low power VLSI design and embedded systems.