

# **FPGA Implementation of Sigma-Delta ADC Using IC MCP3208**

B.T.Jayalakshmi<sup>1</sup>, S.Vamsee Krishna<sup>2</sup>

P.G. Student, Department of Electronics and Communications Engineering, SIETK, Andhra Pradesh, India<sup>1</sup>

Associate Professor, Department of Electronics and Communications Engineering, SIETK, Andhra Pradesh, India<sup>2</sup>

**ABSTRACT:** Analog-to-digital converters have many applications in our daily life. The Sigma-Delta converter is an attractive ADC for future communication systems due to its high number of bit rate. The aim of this project is to design of sigma-delta ADC and it is implemented using SPARTAN 3e FPGA. In this project sigma-delta conversion can be done by using the advanced IC MCP3208 and bit by bit transmission is done finally the output is displayed on monitor of pc. The main aim of this project is to power reduction and the converter is used to achieve 12-bit resolution. In MATLAB Simulink the converter done but greater filter delay in the output and it is not suitable for FPGA implementation. To overcome this problems sigma-delta conversion is done using the Xilinx ISE design tool 14.6 and the power comparison calculation is done. In its supply voltage 5v, analog input is taken as potentiometer, by varying the input voltage (12-bits)  $0-2^{12}$  that means up to 4096 range, through rs232 cable, the output is displayed on monitor. The sigma-delta analog-to-digital converter is suitable for embedded FPGA applications. The sigma-delta architecture has become more and more popular realizing high-resolution ADCs in mixed-signal VLSI processes. This converter is inherently an oversampling converter, although sigma-delta converter is just one of the techniques contributing to the overall performance.

**KEYWORDS:** Analog-to-digital converter (ADC), Field programmable gate arrays (FPGA), Sigma-Delta, VLSI, User Constraint File (UCF).

## **I. INTRODUCTION**

Analog-to-digital converters play an important role in modern audio and communication design. Nyquist converters are used efficiently only for medium resolutions and require analog components that are precise and highly immune to noise and interference. On the other hand oversampling converters are achieve high resolutions (>20bits). In conventional modulators, negative feedback is applied, to control the dynamic behaviour of a system and to realize the attenuation of the quantization noise in the signal band due to noise shaping. With the increasing demand of electronics product, the circuits are complexity to growing high. The competitive pressures available time to design products is shrinking. Field programmable gate arrays (FPGA) provides best solution to address all these issues. Field programmable gate arrays are able to offer advantages over traditional VLSI technology.

## **II. RELATED WORK**

Analog-to-digital converters are classified in two classes: (1) Nyquist rate ADC (2) Oversampled (Sigma Delta) ADC. There are some drawbacks in Nyquist rate converters as follows:

- Medium Resolution
- Require Analog components
- High noise
- High Interference

In Nyquist-rate ADC the input analog signal samples at the sampling frequency ( $f_s$ ) is equal to the twice of the highest frequency component of the input signal. It is necessary for the input signal to band limited; an anti-aliasing filter must be used before the converter to prevent aliasing. This filter must have a very narrow transition band to ensure that the filtered signal does not contain any frequency component above  $f_s/2$ . But to realize narrow transition band anti-aliasing filter is very difficult. Also Nyquist rate converters have low resolution which is not suitable for a very low voltage

# International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 5, May 2015

signal conversion. Oversampled ADCs are preferred over Nyquist rate ADC due to their high signal to noise ratio and high resolution [4].

In case of sigma-delta ADC the modulator portion behaves like a noise shaper and digital filter removes the out of band quantization noise thus ensure much higher SNR which is impossible to achieved in Nyquist ADC[5].In addition to improve SNR,sigma-delta ADC inherently possesses the motivation for prediction. When the signal is oversampled then it does not change significantly in the interval between successive samples [6].Since the values of these samples are very close, they are highly correlated and there are future samples could be predicted from the past one. The linear delta modulator is the simplest predictive modulator. By pushing most of the in-band noise outside the signal frequency band more improvement in the SNR can be achieved. This is attainable if signal transfer function is a low pass whereas and Noise transfer function is high pass. This method is called noise shaping and can be easily and efficiently implemented by modifying the delta modulator[7].Here integral of the input signal encoded rather than input signal directly. Clearly integration is a linear function does not affect system transfer function. The demodulation integrator at output can be placed at the input of delta modulator. This modification of delta modulation system results to the new system called Sigma Delta Modulator as shown in figure1.

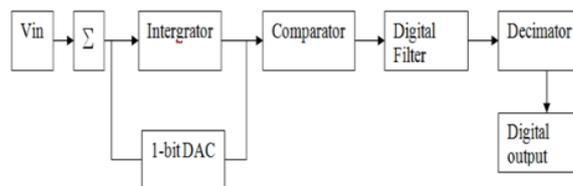


Fig1: General block diagram of Sigma-Delta modulator

## III.EXISTING SYSTEM

Sigma-delta analog to digital converter consists of analog part and digital part. Analog part contains modulator which samples the input signal at high rate and thus produces output in the form of binary sequence. Digital part contains digital decimation filter. Decimation process can be done by using single-stage as well as multi-stage decimation.

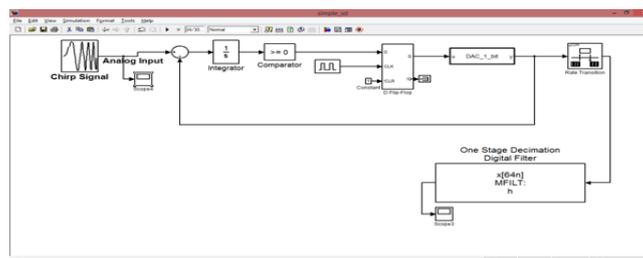


Fig 2: Delta Sigma Modulator in MATLAB Simulink

Herein the first stage, decimation is done by using single stage FIR decimator filter. The function of this filter is to calculate average value of output sequence by using low-pass decimating FIR filter.

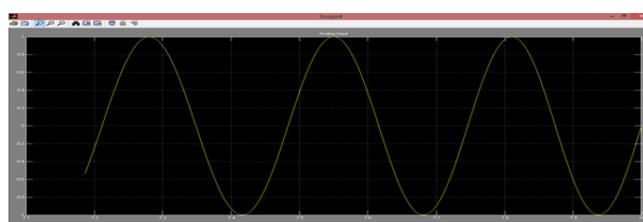


Fig 3: Waveform of the analog chirp signal

# International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 5, May 2015

The figure shows that the analog signal chirp signal in MATLAB Simulink. The first the analog signal is sampled and hold then the digital signal is obtained. In any analog input signal first it samples & holds then it convert in to digital signal. In this sine wave is the input and converts in to square wave.

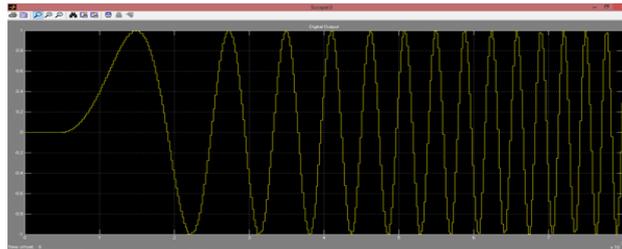


Fig 4: Waveform of the output digital signal

The designed sigma-delta ADC model is not an efficient model why because filter size is very large and not easy to implement such a large size filter on FPGA chip. Hence to overcome this problem, we can break the large decimator filter into three-stage decimation filter. The very first stage decimates the signal by the factor of 8, second stage by 2 and last stage by 4. By using decimation process which consists more than one decimator filter computational difficulties are reduced but this process provides a greater filter delay in the output.

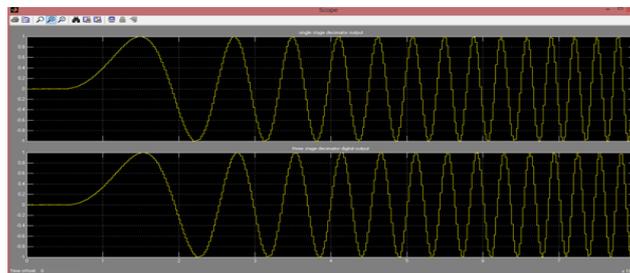


Fig 5: Waveform shows the delay in digital output signals

of single-stage and multi-stage decimator filter.

For the implementation of FPGA, designed model should be in fixed point. But our all designed models are not in fixed point; hence we convert designed sigma-delta ADC in fixed point.

## IV. PROPOSED SYSTEM

To overcome these problems the Sigma-Delta ADC is designed in Xilinx ISE 14.6 and it is implemented using SPARTAN 3e kit. It is suitable for hardware implementation. The figure shows the main block diagram of Sigma-Delta ADC. In this input is potentiometer and It consists of 3-terminals supply varying output display and gnd. The supply pin is connected to the IC supply pin similarly gnd. The second pin is connected to the channel of IC pin. Here the selection of input is the first pin channel as 000. The sigma-delta conversion is done by using the advanced IC MCP3208. Here the input is connected in real time. The IC contains 8-channels. Each and every channel consists of 12-bit resolution. The input channel acts as mux. Based on control logic it can give the output. After the output is sampled and hold value and give to the comparator block. The comparator compares the input signal with that the reference signals. The information is stored in SAR and bit by bit shifting process takes finally the outputs are come into the Dout. The JTAG is used here. The parallel ports are connected to the pc and the JTAG is connected to the FPGA kit. The JTAG is used for the purpose of program load. In this SPARATAN 3e kit is used for the implementation purpose. Here rs232 cable also used for the purpose of storing and transmitting information to the pc. The rs232 has 9-pins that mean female to USB is used and transmission is done.

Here the input is taken as potentiometer, supply voltage is 5v, According to the input analog devices the channel will be selected. by varying the input voltage (12-bits) that means  $0-2^{12}$  upto 4096 range, the output is displayed on monitor

# International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 5, May 2015

of pc. Whatever the output is comes in the Dout after transmission takes place. Here, the spi-din is used to transmit the bits one by one. The spi-cs means chip select is used to totally 8-analog channels are possibilities are there here in that which one bit converting select decided one.

The clock (clk) is used to control the IC. The spi-clk is used for the purpose of control the IC MCP3208. First analog input is given to the IC, the conversion process takes and bit by bit transmission is done on FPGA kit, finally through the rs232 cable stores and transmits the information in to pc, the output is displayed on monitor of pc.

The proposed ling adder technique is used to create the simplified group generate perform known as Pseudo carry. The factorization of 1 not kill bit makes the primary level of carry computation stage straightforward. And also the remainder of the logic of the carry tree is computed in an exceedingly similar manner because the standard theory of parallel prefix adder. The not kill term has got to be combined with the pseudo carry before computation of add at the top. As this involves no delay by the electronic device rather than X-OR circuit to reason adds, the ensuing adder becomes quicker.

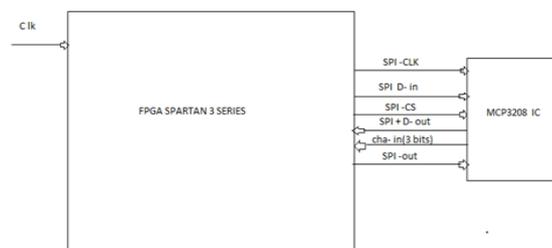
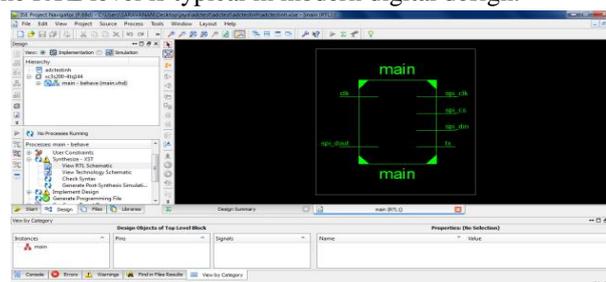


Fig 6: Block diagram of ADC in hardware implementation.

## V. SIMULATION RESULTS

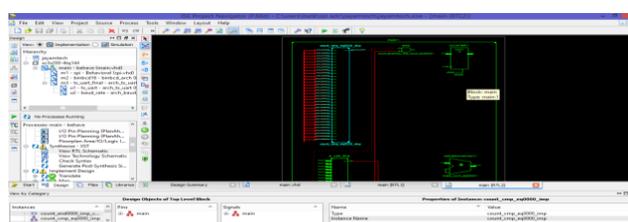
### A. RTL Schematic

RTL stands for register-transfer level and its abstraction is used in hardware description languages like Verilog and VHDL to create high-level representations of a circuit, from which lower-level representations & ultimately actual wiring can be derived. Design at the RTL level is typical in modern digital design.



### B. Technology Schematic

The technology schematic is shown below figure. It consists of inner each sub-modules of the register transfer level blocks. It gives each sub-blocks schematic of main register level main module. In this number of gates used as logic levels, number of LUTs used all things shown in this technology of sigma-delta ADC and also ASIC file also generated.



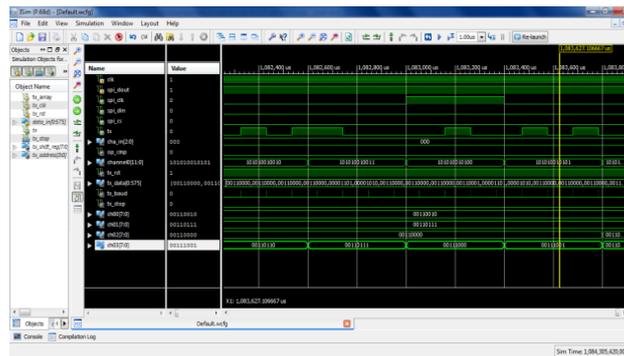
# International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 5, May 2015

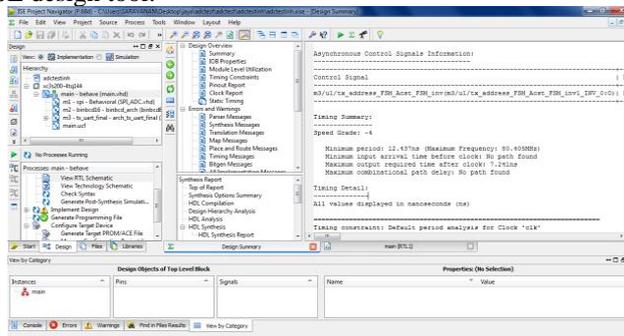
## C. Output

The cha-in(3-bits) in that first channel is selected that means '000' and the clk state force to high, the outputs are come into the dout. The 12-bit resolution is stored in to the one variable that is channel[11:0] and the output is displayed in 4 digits. so the binbcd converts into 4 characters ch0, ch1, ch2, ch3 and the each character contains 8-bits and one by one transmits and stores into tx , it contains certain baud rate, finally the output is displayed in tx-data.



## D. Delay

After simulation process complete, click the synthesis report calculate the delay. The maximum period is 12.437ns and the total delay gives the net delay and gate delay. The total overall delay of Sigma-Delta conversion is mentioned. These are seen by using the Xilinx ISE design tool.



## E. Area Utilization

The whole information regarding the used devices from available devices in proposed sigma-delta ADC as shown in table 1. In this number of slice flip-flops and number of 4 input LUTs, number of occupied slices contains related logic and unrelated logic and total number of 4 input LUTs number used as logic and route-thru, number of bonded IOBs, number of BUFGUXs and average fanout of non-clk nets. This device utilization summary gives detailed information to the overall performance and how many gates used are all gives these summary. After this UCF file is created. Acronym of UCF is user constraint file. In this pin locations are assigned.

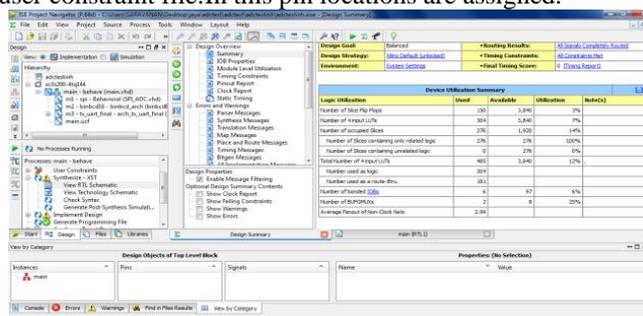


Table 1: Resource utilization for Spartan 3edevce



# International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 5, May 2015

After click the boundary scan IMPACT dialog box the architectures and user constraints file is generated. when the process is completed, implement on the FPGA kit.

## ii.Implementation on FPGA kit

This is the last step for the implementation of sigma –delta ADC on FPGA kit power input. After that download cable is connected between the FPGA kit and pc. The JTAG cable is connected between the kit and pc for the purpose of program load. Then run the configure device (IMPACT) process.When the programming is completed the window shows, the program succeeded message is displayed.



Fig 7: IMPACT boundary scan dialog box

After that that connecting cable kit to the pc.The analog input is potentiometer; the second pin is connected to the IC MCP3208 first channel pin. Supply voltage 5v is given to the Ic.The cables used are JTAG (joint test action group)and rs232 cable to store and transmitting the information. The Spartan 3e EDK board provides a powerful, self-contained development platform for designs targeting the new Spartan -3 FPGA from Xilinx. It features a 200k gate Spartan 3,one board i/o devices,1MB fast asynchronous SRAM, from a simple logic circuit to an embedded processor core. The figure shows the Tyro-Plus Spartan 3e (EDK) board.



UART stands for universal asynchronous receiver transmitter. The FPGA kit provides an RS232 port that can be driven by the Spartan 3e FPGA kit.A subset of RS232 signals in used on the Spartan 3 FPGA lab kit to implement this interface (RD&TD signals). The FPGA kit provides female DB-9 connector, labelled p2.The user provides RS232, UART code, which resides the FPGA Spartan 3kit.The female pin is connected to the kit and the USB port is connected to the pc.



After that the output is displayed on monitor of pc.



## International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 5, May 2015

The output is displayed on monitor by using the tera term software. Here using two cables one is rs232 and another one is JTAG cable. For program load purpose the JTAG is used. The parallel port is connected to the pc and the JTAG is connected to the FPGA kit. Finally the output is displayed on monitor of pc. The output is displayed between the range 0-4096 range only(12-bits)resoultion.

### VI. CONCLUSION

In this, we have designed of Sigma-Delta ADC and its implementation on SPARTAN 3eFPGA kit. It consumes only 150 number of slice Flip Flops out of available 3,840, 304 number of 4 input LUTs out of 3840 and 276 number of occupied slices out of 1,920 and number of slices containing only related logic 276, number of slices containing unrelated logic is 0 and total number of 4 input LUTs are 485 out of 3,840 in that number used as logic is 304 and number used as route-thru 181. Number of bonded IOBs 6out of 97 and number of BUFGMUXs is 2 out of 8 and average fan out of non-clock nets 299 respectively. The proposed design power consumption is 350uw. Results shows that the proposed design is quite accurate.

### REFERENCES

- [1] Eric T.King, Aria Eshraghi, Ian Galton, and Terri S.Fiez, "A Nyquist-Rate Delta-Sigma A/D Converter," IEEE Journal of Solid-State Circuits, Vol.33, no.1, pp.45-52 January 1998.
- [2] Memon T.D., Beckett P., Sadik A.Z., "power Area Performance Characteristics of FPGA based Sigma Delta FIR filters", J Sign Process System, Vol 70, no 3, pp 275-288, March 2013
- [3] Pascal Witte, Jobashn G.Kauffman, Joachim Becker, Maurits Ortmanns. A Correlation-Based Background Error Estimation Technique for Band pass Delta-Sigma ADC DACs", IEEE Trans.on Circuits&sys-tems, Vol.58, no.11, Nov.2011.
- [4] George I Bourdopoulos, Aristodemos Pnevmatikakis, Vassilis Anastassopoulos, Theodore L Deliyannis: Delta sigma Modulators, Design & simulation. Imperial college press, 2006
- [5] Yuanyuan Zhang; Yanfeng Jiang "Noise shaping sigma delta modulation techniques and models simulation, "Solid-state and Integrated Circuit Technology, 2006. ICSICT '06'. 8<sup>th</sup> International Conference, pp.23-26 October 2006.
- [6] Sangil Park "Principles of Sigma Delta Modulation for Analog to Digital Converters", Motorola Digital Signal Processors.
- [7] B.P.Lathi, "Modern Digital and Analog Communication Systems, "Oxfordpress, Third edition.
- [8] Gabor C.Temes and Richard Schreier, Understanding Delta-Sigma Data Converters, IEEE Press.

### BIOGRAPHY



**B T Jayalakshmi** completed her BTech degree in Electronics and Communication Engineering from KKC Institute of Engineering & Technology, Puttur. Presently she is pursuing her Master's degree in VLSI System design of Electronics and Communication in Siddharth Institute of Engineering and Technology, Puttur, from 2013 to 2015. She is currently working on a project titled "FPGA IMPLEMENTATION OF SIGMA-DELTA ADC USING IC MCP3208" as a partial fulfillment of her MTech degree.



**S Vamsee Krishna** completed his BTech degree in Electronics and Communication Engineering from JNTU Hyderabad in 2005 and MTech VLSI system design in 2009 JNTU Anantapuramu, A.P, India. He is currently working as an Associate professor in Department of E.C.E in Siddharth Institute of Engineering & Technology, Puttur, A.P, India.