ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 2, February 2017

High Speed IIR Notch Filter Using Pipelined Technique

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ABSTRACT:Filters are being designed using the HDL languages to increase their speed. Increase in the speed of the individual block leads to increase in the speed of complete block. Field-Programmable-Gate-Array (FPGA) based design and implementation of extremely high speed realization of Infinite Impulse Response (IIR) notch filter. The basic 2nd ordered notch filter structure is implementable in Xilinx Virtex-5 FPGA with maximum clock frequency of ~80MHz. Here, we propose a FPGA based design of extremely high speed notch filter effectively operating at maximum clock frequency of ~1200MHz with the help of Scattered-Look-Ahead (SLA) pipelining with power-of-2-decomposition approach, proper retiming and unfolding applied over its basic low-speed structure. To generalize its FPGA based design for specific speed up factor, a new efficient simpler approach utilizing Pascal's Triangle is proposed to calculate the multiplier coefficients of feed-forward and feedback sections of extremely high speed notch filter.

KEYWORDS: Scattered look ahead, pipelining, Baugh wooley multiplier, Pascal's triangle method

I.INTRODUCTION

High performance digital filter is the need of digital signal processing. The speed of a filter realization counts not alone on the potentialities ofthe hardware platform on which it is employed, but as well on the computational structure of the code. In pipelining long critical path is broken into smaller paths so as to increase the sampling speed and decrease the power consumption at same speed. IIR is the property that is applicable to linear time invariant systems. IIR filters have feedback because of which they requires less memory and more accurate frequency response as compare to FIR filters. Filters are the key functional block in the field of signal processing. The central idea behind the project is to optimize the filter by using pipelining. Notch filter is a band-stop filter with a narrow stop band. The function of the notch filter is to attenuate, if not suppress properly, the unwanted interfering signal may cause problem in present days communication like Spread Spectrum Receiver, GSM etc. similar case with the non-communication receivers like Electronic Support Measure Receivers. A band reject (band stop) filter is a filter passes the most part of frequencies unchanged but attenuates other frequencies to very low levels in a certain range. There are three kinds of notch filter (a) Fixed notch filter (b)Tunable notch filter and (c)Adaptive notch filter. In fixed type of notch filter only one frequency gets attenuate. Tunable notch filters have a range of frequencies that they can be attenuate. Adaptive notch filters (ANFs) can automatically adjust their frequency response depending upon circumstances. A band-stop filter works to screen out frequencies that are within a certain range and it gives easy passage only to frequencies outside of that range. Response of the notch filter is given as shown in the fig 1. The objective of this paper is to make notch filter that will be useful in various fields. Along with the pipelining in the IIR notch filter parallel processing of inputs can be done by using parallel adders and multipliers. Fast adders and multipliers is the need of the digital signal processing. This paper discusses about the pipelining in IIR filters for the optimization of speed and power.

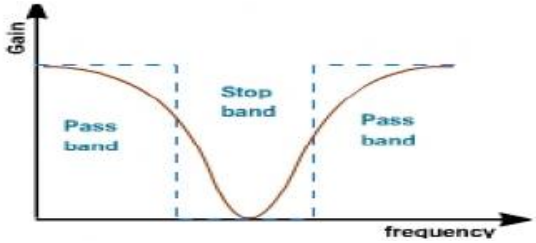

FIG 1:Notch Filter Response

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

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Vol. 6, Issue 2, February 2017

II.LITERATURE SURVEY

A. ADVANTAGES OF IIR OVER FIR FILTER

IIR filters have certain advantages over FIR filters. IIR filter involves feedback which helps to give accurate output. IIR filters make polyphase implementation possible whereas FIR filters cannot. IIR filters require less memory as compare to FIR filters.IIR filters are dependent on both input and output and consist of both poles and zeros whereas FIR filters have only zeros. FIR filters can only use for the linear phase applications whereas IIR filters can use for non-linear phase applications.

B. INFINITE IMPULSE RESPONSE FILTER

Output from a digital filter is made up from previous stage inputs and previous stage outputs, which uses the operation of convolution. The difference equation for IIR filter which defines how the output signal is related to the input signal is given by

$$y[n] = \frac{1}{a_0}(b_0\,x[n] + b_1 x[n-1] + \cdots + b_p x[n-p] a_1 y[n-1] - a_2 y[n-2] - \cdots - q_Q y[n-Q])$$

III.TYPES OF DIGITAL FILTERS

There are basically two types of digital filters Infinite impulse response filter(IIR) and the finite response filter(FIR). FIR filters have linear phase characteristics while IIR filters have non-linear phase characteristics. IIR filters have lower filter order and hence less complex circuits as compare to the FIR filters. As IIR filters involve feedback it requires less memory as compare to the FIR filters.

IV.INFINITE IMPULSE RESPONSE FILTER

The difference equation for IIR filter which defines how the output signal is related to the input signal is given by

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where P = feed forward filter order, bi = feed forward filter coefficients, Q = the feedback filter order, ai = feedback filter coefficients, x[n] = input signal ,y[n] = output signal.

Output of an IIR digital filter uses previous stage inputs and previous stage outputs, which uses the operation of convolution. An IIR filter is a recursive filter where the current output depends on previous outputs.

The compressed form of the difference equation is given by

$$y(n) = \frac{1}{a_0}\left(\sum_{i=0}^{P} b_i x[n-i] - \sum_{j=1}^{Q} a_j\, y[n-j]\right)$$

V.PROPOSED ARCHITECTURE

Fig 2. Illustrates the basic structure of the second order IIR tunable notch filter. In the below structure adder is represented by +, multiplier is represented by *, delay is represented by 'D', input signal is represented by X and output signal is represented by Y. Filter coefficients will be given to the multiplier and a1 and a2 represents the filter coefficients. The proposed methodology will imply on this basic structure of the second order IIR tunable notch filter.

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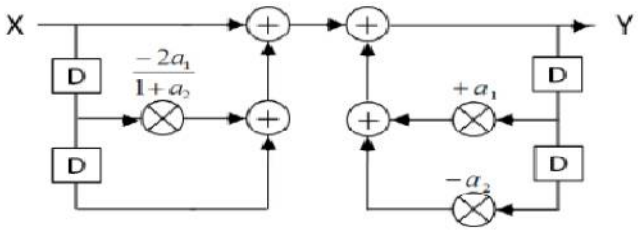

FIG 2: Second order IIR notch filter

VI.PIPELINING

Pipelining is useful for the reduction in the critical path which will either increase the clock speed(which is also known as sampling speed) or reduces the power consumption [4]. It is a key for processors to make fast. Pipelining is used to accelerate program execution time by increasing the number of instructions finished per unit [2].

For first order IIR filter Look ahead techniques can be used which adds canceling poles and zeros with angular spacing at a distance from origin which is same as that of original pole [5]. Scattered look-ahead pipelining is useful to derive stable pipelined IIR filters. Scattered look ahead pipelining along with decomposition technique is useful to obtain area-efficient implementation for higher-order IIR filters.

In scattered-look-aheadpipelining with power-of-2 decomposition[4][5][6][7], if the transfer function of a recursive digital filter be represented by

$$H(z) = \frac{N(z)}{D(z)} = \frac{\sum_{i=0}^{N} b_i z^{-1}}{1 - \sum_{i=1}^{N} a_i z^{-1}}$$

Then implementation of2-stage pipelined structure is obtained by multiplying it with the term in the numerator and denominator.

$$1 - \sum_{i=1}^{N} (-1)^i \, a_i z^{-i}$$

The implementation of 2-stage pipelined structure is given by

$$H(z) = \frac{N(z)}{D(z)}$$
$$= \frac{\sum_{i=0}^{N} b_i z^{-i}(1 - \sum_{i=1}^{N}(-1)^i \, a_i z^{-1})}{[1 - \sum_{i=1}^{N} a_{iz}{}_{-1}][1 - \sum_{i=1}^{N}(-1)^i \, a_i z^{-1}]} = \frac{N'(z)}{D'(z)}$$

In the same way, log2M (M being power-of-2) sets of such transformations can be applied to achieve M-stage pipelined implementations. Pipelined implementation is given by fig 3. where M1, M2, M3…. represents filter coefficients.

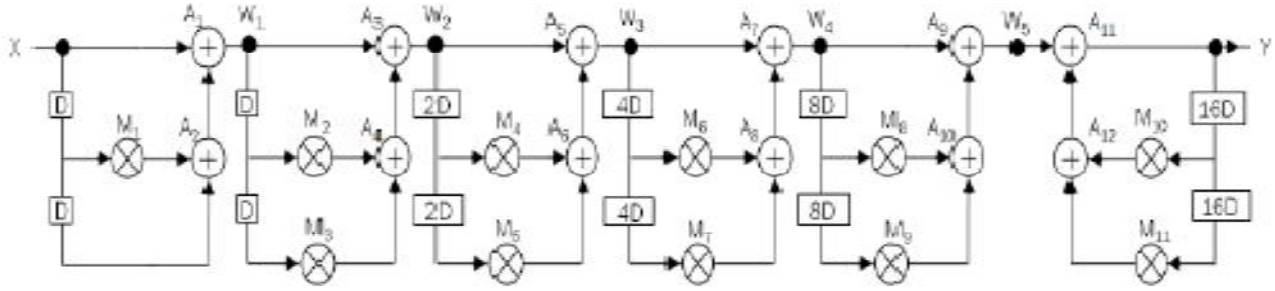

FIG3: Pipelined Second Order IIR Filter

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ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

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VII.METHODOLOGY

A. FAST ADDER

Adders form an almost obligatory component of every contemporary integrated circuit. The necessary condition of the adder is that it is primarily fast and secondarily efficient in terms of power consumption and chip area. There are various adder topologies present like ripple carry adder, carry look ahead adder, carry save adders, carry select adder etc. out of which we have selected a carry select adder for its low power consumption and lower delay [12]. Fig 4 illustrates the architecture of carry select adder. But carry select adder leads to increase of hardware.

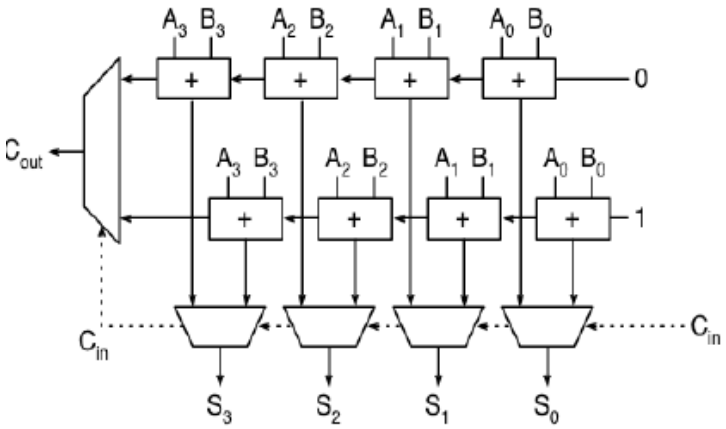

Fig 4:Carry Look Adder

B. FAST MULTIPLIER

Multiplication is an important arithmetic operation. There are various types of multipliers present. Out of which Baugh Wooley multiplier is selected for low power consumption and less delay as compare to other multipliers [8]. Fig. 5 illustrates the algorithm for an 8-bit multiplication. In this multiplier the partial product bits are reorganized according to Hatamian's scheme [9]. The creation of the reorganized partial-product array of an N-bit wide multiplier comprises three steps: i) The most significant bit (MSB) of the first N −1 partial-product rows and all bits of the last partial-product row, except its MSB, are inverted. ii) A '1' is added to the Nth column iii)Inverted MSB is obtained in result.

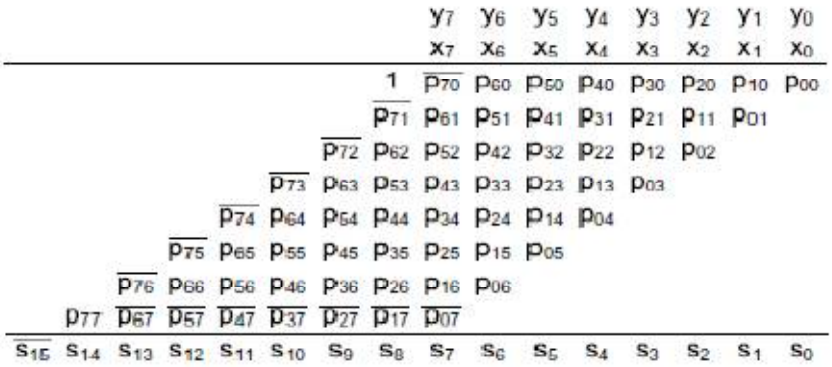

Fig 5: Illustration of an 8-bit Baugh-Wooley multiplication

Baugh-Wooley Multiplier which is used for both unsigned and signed number multiplication. Signed Number operands which are represented in 2's complemented form. Arrangement of partial products is such that negative sign move to

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last step, which maximizes the regularity of the multiplication array. Baugh-Wooley Multiplier performs on signed operands with 2's complement representation to make sure that the signs of all partial products are positive [10,11].

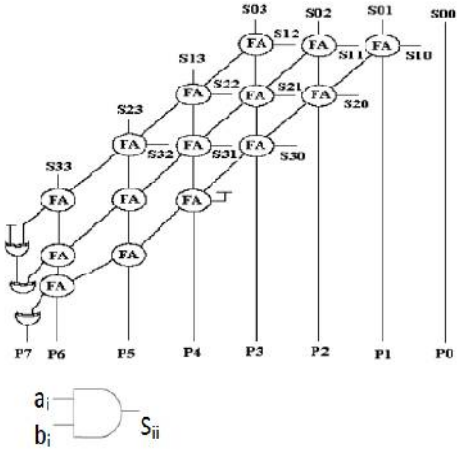

Fig 6:Block Diagram of 4*4 Baugh-Wooley Multiplier

C. DELAY BLOCK

Delay block used in the circuit is used to delay the input signal by the number of clock cycles. There are 1D, 2D, 4D, 8D and 16D delays. 1D delay will delay the input signal by one delay than 2D will delays by 2, 4D will delays by 4 an so on. Hence the function of the delay block is to make signal reach at certain point late by N numbers of delay.

D. PASCAL'S TRIANGLE METHOD

A new and simpler approach for the calculation of IIR filter coefficients is Pascal's triangle [3,13]. Pascal's triangle has proved very useful applications in mathematics as well as other fields. Out of such applications one wonderful application is to calculate filter coefficients of IIR filter. Simply by subtracting the values of upper row (shown in square box) from the lower row (shown in circle) ex-first coefficient is given by 10-0=10 next given by 36-1=35 and so on. Pascal's triangle is as shown in the fig.

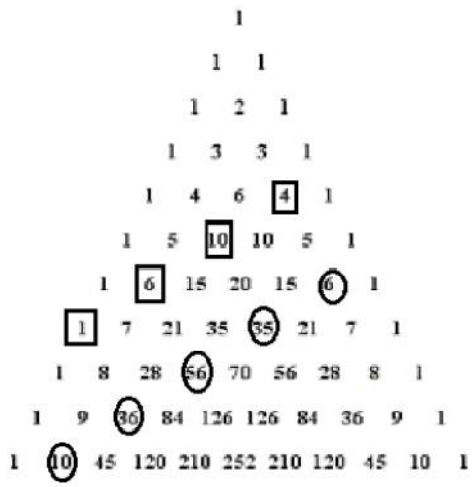

Fig 7:Pascal's Triangle

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Vol. 6, Issue 2, February 2017

VIII.STAGES

For the convenience in coding complete circuit is divided into sub stages as shown below.

STAGE 1: Below Fig. 8 shows output of Stage 1.

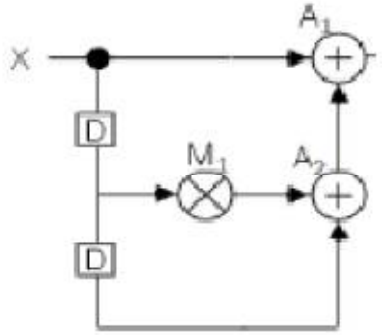

Fig 8:Output of the stage1.

STAGE N: Below Fig.9 shows output of Stage N.

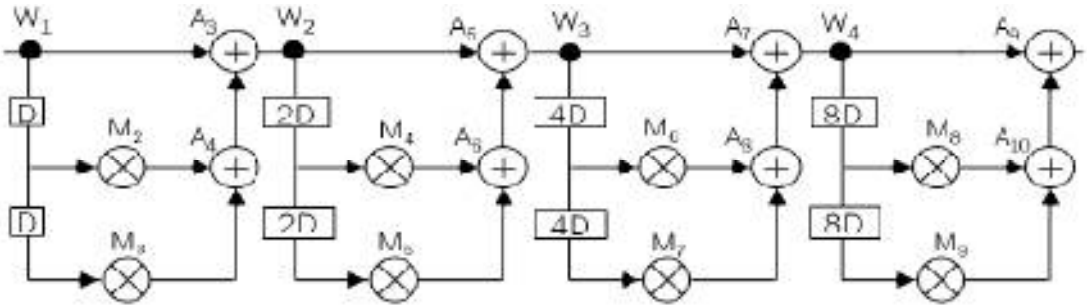

Fig. 9: Output of the stage N.

IX.RESULT

A. Carry Select Adder: Below fig.10 shows Xilinx ISE Simulation of Carry select adder

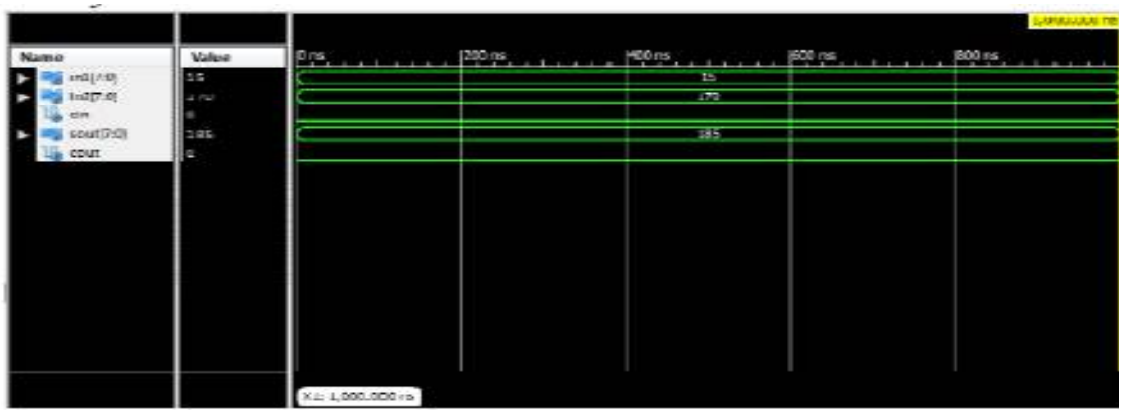

Fig 10: Xilinx ISE Simulation of carry select adder

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B. Baugh Wooley Multiplier: Below fig.11 shows Xilinx ISE Simulation of Baugh Wooley Multiplier

Fig 11: Xilinx ISE Simulation of Baugh Wooley Multiplier

C. Delay Block: Below fig.12 shows Xilinx ISE Simulation of Delay block

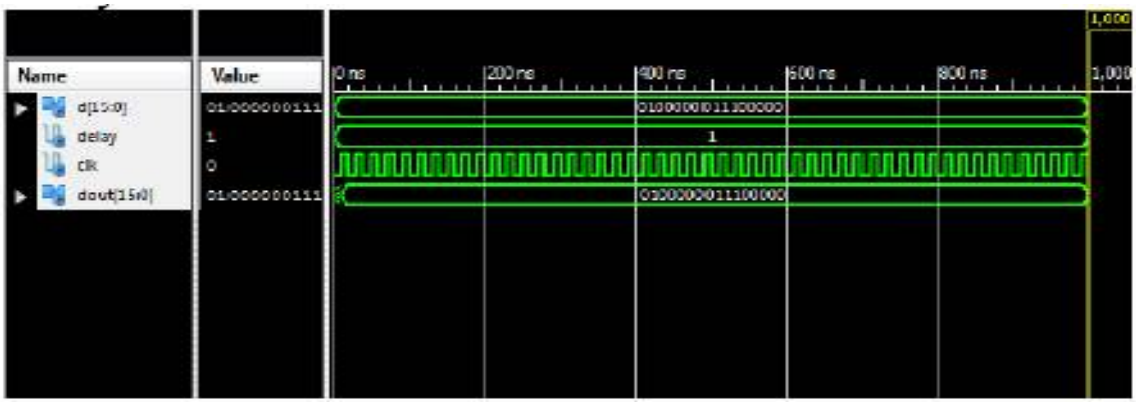

Fig 12: Xilinx ISE Simulation of Delay block

D.Stage1: Below Fig. 13 shows Xilinx ISE Simulation of Stage 1

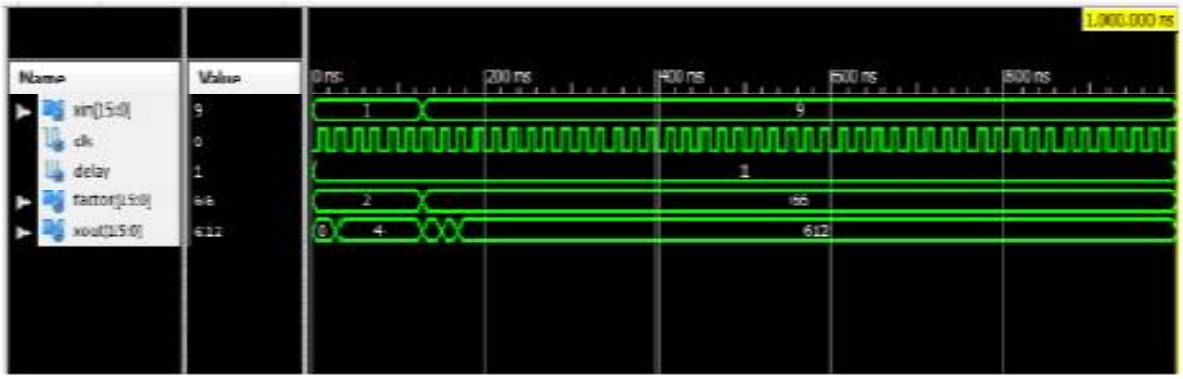

Fig 13: Xilinx ISE Simulation Result of Stage 1

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ISSN (Online): 2278 – 8875

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E.Stage N: Below Fig 14 shows Xilinx ISE Simulation of stage N

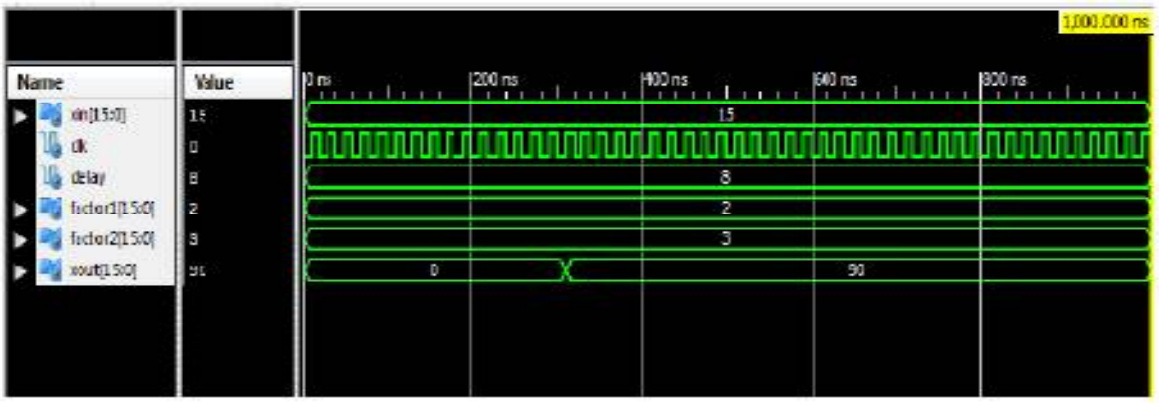

Fig 14: Xilinx ISE Simulation Result of Stage N

X.CONCLUSION

The proposed Scattered look ahead(SLA) pipelining along with the fast adders and multipliers is introduced throughout this research work. Second order IIR notch filter is being implemented by using the SLA pipelining with power ofdecomposition 2. The proposed is useful in communication as well as non-communication field where noise suppression is required. This can beimplementable on virtex-5 having the clock frequency of 80 MHz. following are the results obtained.
Number of slice LUTs used= 2%
Power = 105mW
Maximum frequency=3 MHz.
Minimum period=0.333 usec.

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