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IMPROVEMENT OF THE QUALITY OF VLSI CIRCUIT PARTITIONING PROBLEM USING GENETIC ALGORITHM

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Abstract: In this paper, Genetic algorithm for circuit partitioning has been attempted. In this practical paper solution is easy and we can easily apply genetic operator in this type of problem. Complexity is measured in both time and space, provided size of problem an as integer (count is infinite).This paper shows multiway circuit partition using genetic algorithm. The technique of our approach is to be design module trick. We can be realizing with self standard IC chip. Obviously we have taken into account minimum power conjunction. The solution of a circuit partitioning problem is global optimum. Result obtained versatility of the proposed method in solving NP-hard problem. Like circuit partitioning is the more critical step in the physical design of various circuit in VLSI.In the partitioning main objective is to minimize the number of cuts. This chapter addresses the problem of partitioning and particular the use of the genetic algorithms for circuit partitioning. The objects to be partitioned in VLSI design are typically logic gates or instances of standard cell.
Circuit partitioning is one of the important parts in chip designing. The algorithm can partition circuit into a number of sub-circuits. Our method calculates the fitness value and discards solution with low fitness value. The increase in number of crossover point does not necessarily increase the fitness, as the fitness achieved depends on crossover as well as mutation probability. Especially in the paper find minimum cut size. Crossover boundary will be changed when fitness value is low in previous generation.
The main superiority of the circuit partitioning using genetics algorithm is "we can easily multiway partitioning in many types of VLSI circuit".

Index terms: Partitioning, Genetic Algorithm, NP-hard, Net list, Crossover, Mutation, cut size

Partitioning:

a. Divides the circuit into smaller partition that can be efficiently handled.
b. Start with initial partition.
c. Count cut size.
d. Find best partitioning (minimum cut size).

Genetic algorithm:

The genetic algorithm involves the following basic steps-
(a). Evaluation.
(b). Crossover.
(c). Mutation.

Encoding:

There are many ways of representing individuals' genes.
(a). Binary encoding.
(b). Octal encoding.
(c). Hexa-decimal encoding.
(d). Permutations encoding.

Crossover:

(a). One point crossover :-
Part of the first
Parent copied rest is copied from second parent.
(b). Two point crossover :-

Two crossover:

points are selected, binary or octal string from beginning of chromosome to the first crossover point is copied from parent 1. The part from the first to the second crossover point is copied from the second parent and the rest is copied from the first parent.

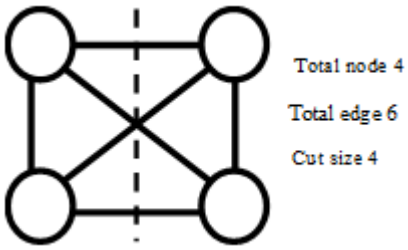
- Multi-point crossover.

Mutation:

For chromosome using binary or octal encoding randomly selected bits are inverted.**********

Mutation probability (Pm):-

Mutation rate is the probability of mutation which is used calculates number of bits to be muted. The mutation operator preserves the diversity among the population which is also very important for the search. Mutation probabilities are smaller in natural population leading us to conclude that mutation is appropriately considered a secondary mechanism of genetic algorithm adoption.
Individual → 011101001011 and Pm = 0.25
Then we say, 3 bit will be inverted.



INTRODUCTION

The advancement in VLSI semiconductor technology has led to a phenomenal development in Electronics Industry, leading to more chip complexity and higher integration. However as the chip density increases numerous issues like ease of design, testing, increased delay, interconnect area optimization arise which need to be handled at the design stage. Improved physical design tools are necessary to handle these issues. Circuit net list partitioning is an important step in VLSI physical design.

With the development in technology and growing demand for system on a chip (SOC) integrated circuit had become more and more complicated. This creates a big challenge in IC design. Among steps in the design process the circuit

partitioning which is required as the first step in physical design has especially become very important. A better circuit partitioning will reduce connection among sub-circuits and result in better routing area of layout. The main objective of circuit partitioning include minimization of number of inter connection between the partitions.

Efficient easily applied algorithms for optimal clustering to minimize delay in digital networks were developed by Lawler at al. kernighan and lin proposed heuristic for two way partitioning which was the first iterative algorithm based on swapping of vertices.

Circuit partitioning consist of dividing a circuit into parts each of which can be implemented as a separate component(e.g. a chip) that satisfies certain design constraints one search constraintsis the area of the component. The limited area of a component forces the designer to lay out a circuit on several components. There has been a larger amount of work done in the area of circuit partitioning and clustering. In circuit partitioning, the circuit is divided into two (Bi-partitioning) or more (Multi-way partitioning) parts.

This chapter addresses the problem of partitioning and particular the use of the genetic algorithms for circuit partitioning. The object to be partitioned in VLSI design is typically logic gates or instances of standard cell. The main advantage of circuit partitioning using genetics algorithm is "we can easily multiway partitioning in many types of circuit"

The different objectives that may be satisfied partitioning are:-

a. The minimization of number of cuts:

The number of inter-connection among partitioning has to be minimized. Reducing the inter-connection not only reduce the delay but also reduce the interface between the partitioned making it easier for independent design and fabrication. It is also called min-cut problem.

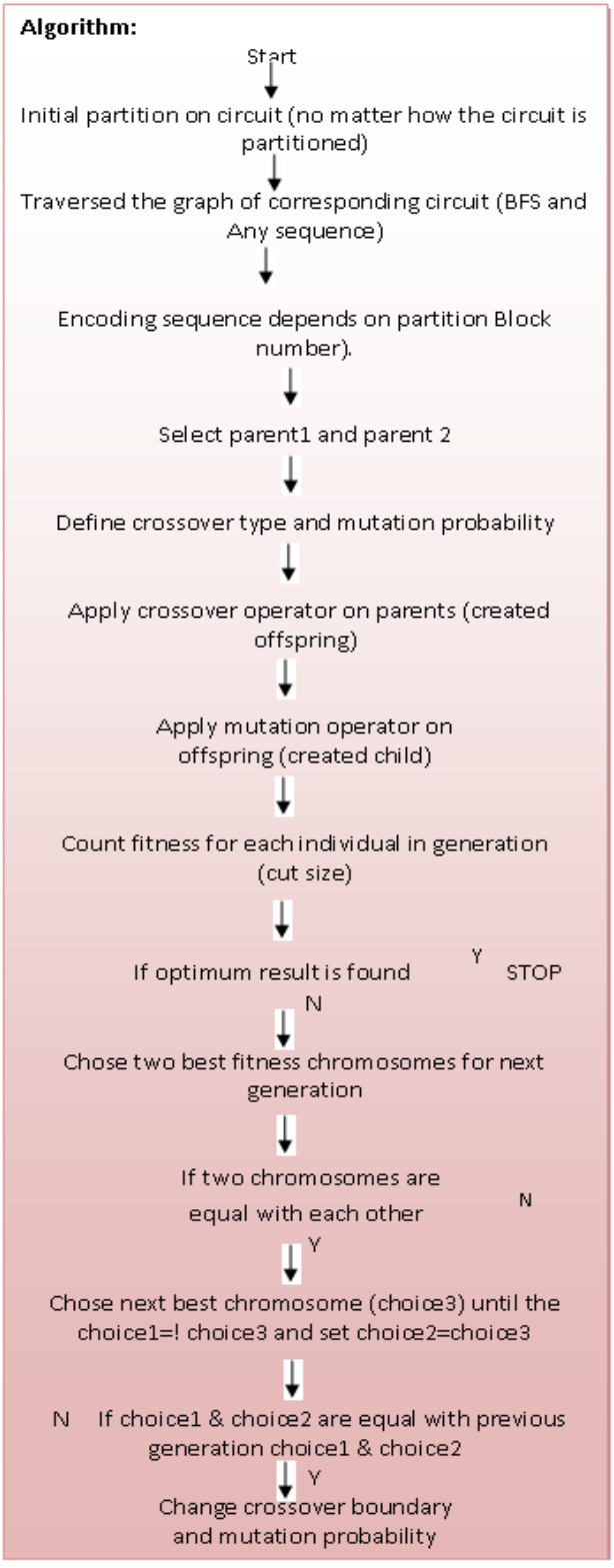
b. Area of each partition is used as a constraint to reduce the fabrication cost with minimum area or as a balance constraint so that partitions are of all most equal size. Various researchers have achieved varying level of success using various optimization techniques. The current work attempts to use simple genetic algorithm for multiway VLSI circuit partitioning. Because genetic algorithm is an emerging technique. This technique has been applied to several problems, most of which are graph related because the genetic metaphor can be most easily applied to these types of problems. Genetic requires more memory but take less time.

The main superiority of the circuit partitioning using genetics algorithm is "we can easily multiway partitioning in many types of VLSI circuit".

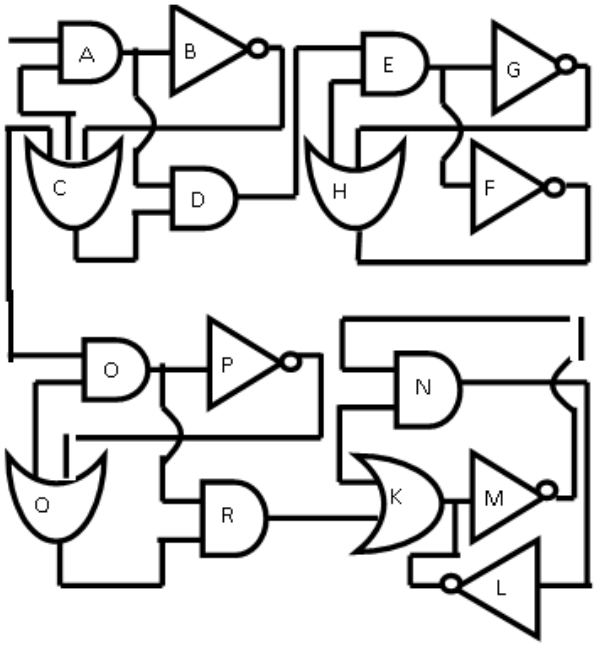
SOLUTION METHODOLOGY

Initially the circuit will be cut. It is point less to consider the cut cost of such nets, since no matter how the circuit is partitioned. And the net-list is traversed in a breadth-first-search order and the cells are assigned to the chromosome in this order. If two cells are directly connected to each other, there is a high probability that there partition bits will be closed to each other in the chromosome.

The BFS sequence of the net-list will be parent 1 and any sequence of the net-list will be parent2. The genetic algorithm are not guaranteed to find the minimum cost (optimum), but able to find very good solutions for a wide range of problem. Each generation choice to best chromosome (Best fitness) from previous generation for parent.



Chromosome representation:



The corresponding graph will be-----

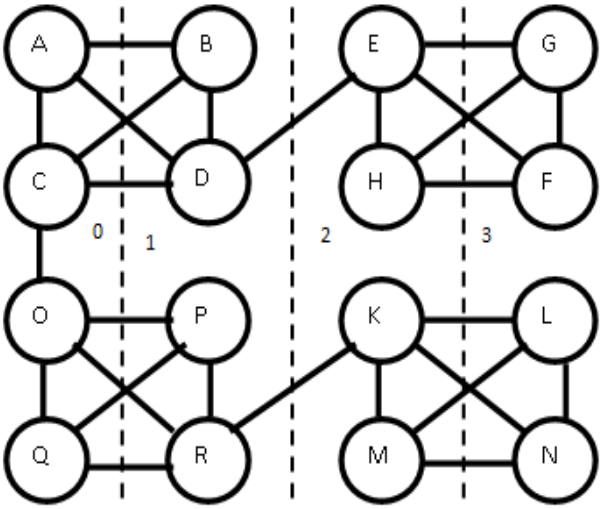
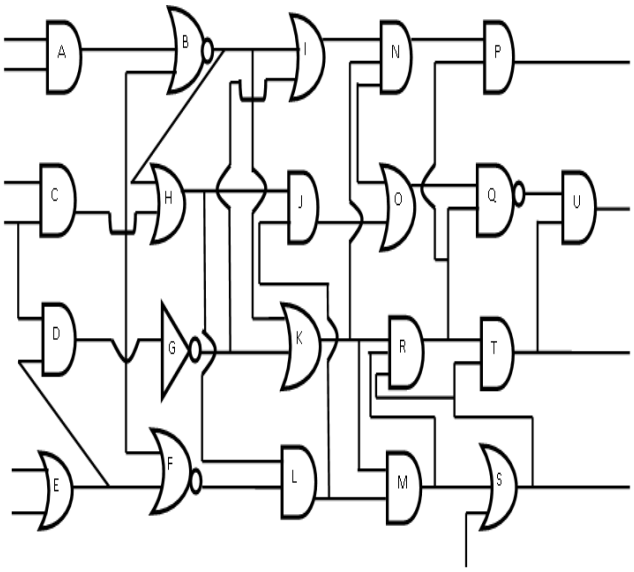


Table: 1

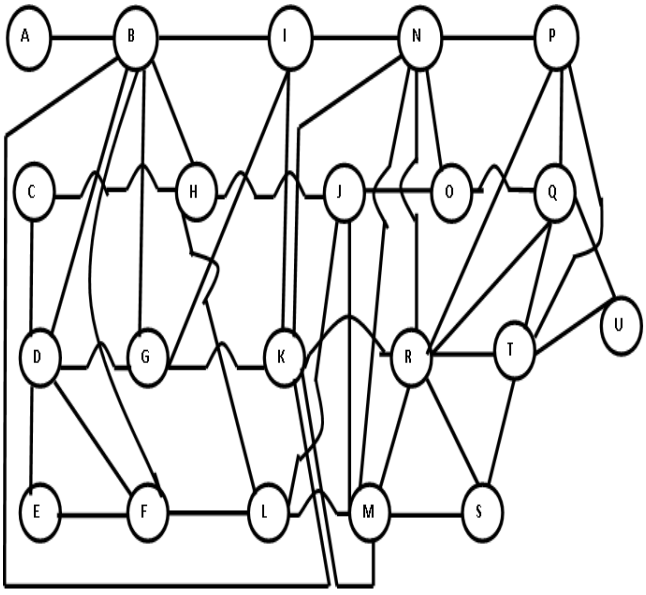
INDIVIDUAL	MIN_CUT	AVG_CUT
0 0 1 1 0 2 0 1 1 2 3 3 2 2 3 3	19	
0 0 0 1 1 2 3 2 3 3 1 1 2 0 3 1	19	
0 0 1 1 1 2 3 2 3 3 1 1 2 2 3 3	19	19
0 0 0 1 0 2 0 1 1 2 3 3 2 0 3 1	18	
0 0 1 1 2 3 1 2 3 3 1 1 2 2 3 3	19	
0 0 0 1 2 0 0 1 1 2 3 3 2 0 3 1	23	

EXPERIMENTAL RESULT

The genetic algorithm has been used to minimize the interconnections that are the min cut problem with a balance constraint. The coding has been done using MATLAB r2012a (7.3 versions). The above graph contains 21 gates, and the proposed algorithm is applied by the MATLAB r2012a on above graph and run the programme and takes the result after 10 generation.



The corresponding graph will be-----



parent1=[1 1 1 0 0 0 1 1 1 1 0 0 0 2 0 2 2 2 2 2 2 2]; % BFS order

parent2=[2 1 1 0 0 0 2 1 2 1 0 0 0 0 1 2 2 1 1 2 2]; % any order

Table: 2

No. of iteration	Min cut	Avg.cut	Max cut
10	15	18	26
20	15	18	24
30	15	18	24
40	15	18	24
50	13	17	24
60	13	17	24
70	13	17	24
80	13	17	24
90	13	17	25
100	13	17	25
110	13	17	25
120	13	17	25
130	13	17	24
140	13	17	24

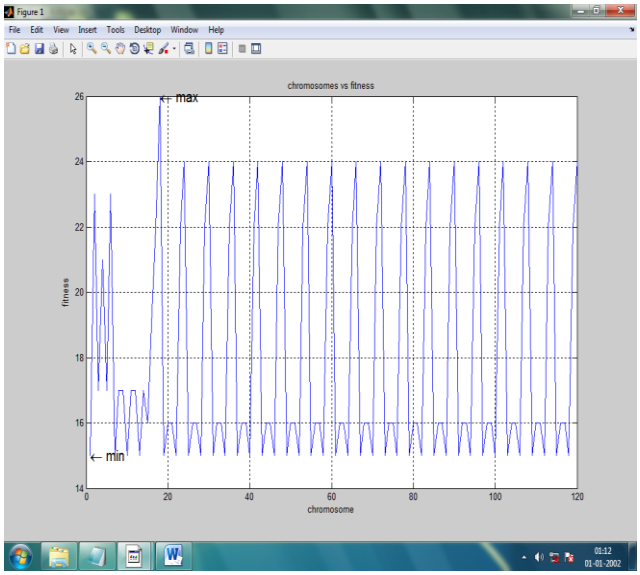


Figure 1: Plot for Fitness vs. Chromosome in 1:10 generation.

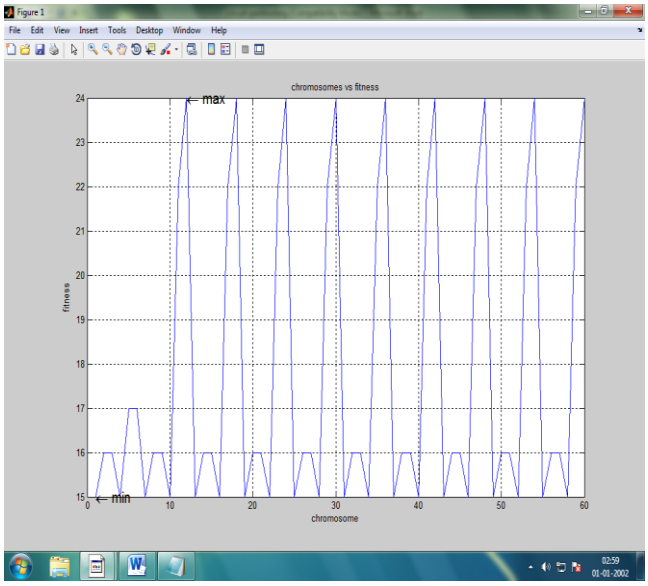


Figure 2:Plot for Fitness vs. Chromosome in 11:20 generation

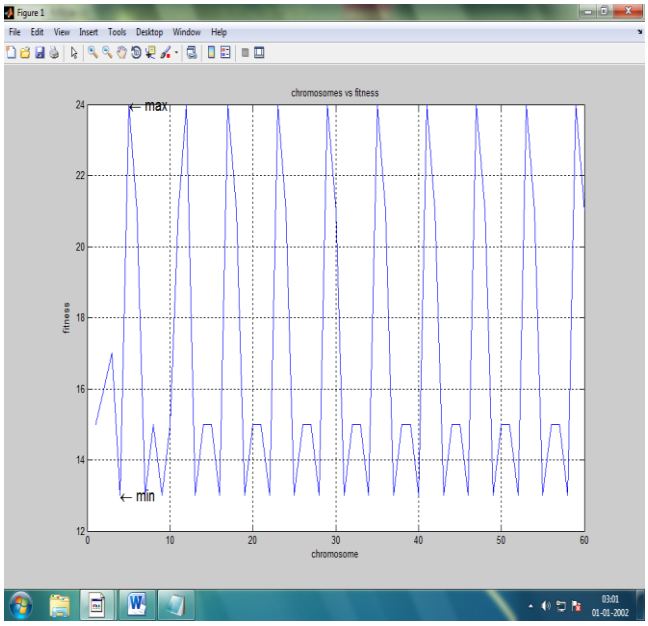


Figure 3:Plot for Chromosome vs. Fitness in generation 41:50

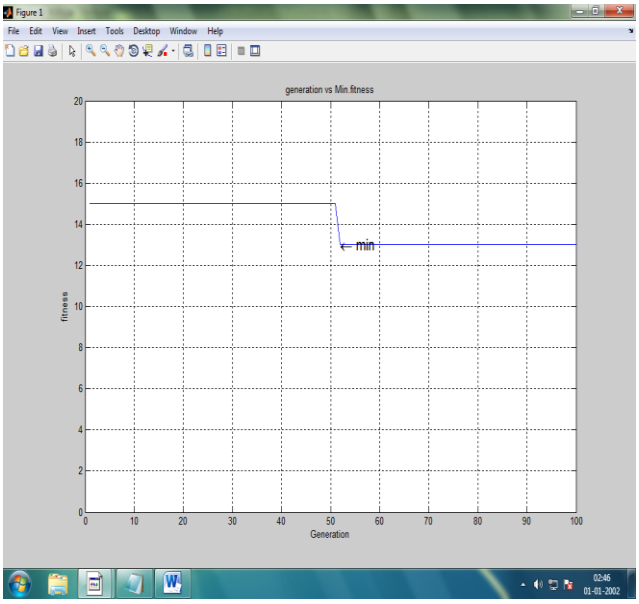


Figure 4: Plot for minimum fitness in 100 generation

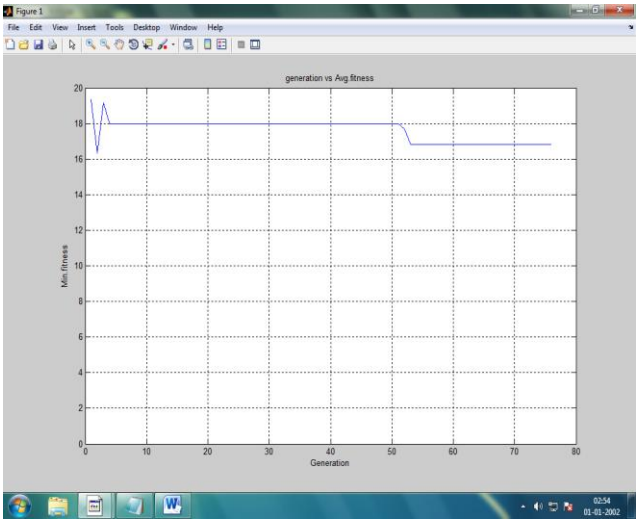


Figure 5: Plot for Avg. fitness in 1:75 generation.

As seen from the results in Fig.1 when increasing the no.of itaration 1:10 we get the one time maximum fitness and many times minimum fitness.But when we increasing no.of itaretion 11:20 in Fig.2 we see minimum fitness is constant but maximum fitness is lowered better than the figure.1.According to Itaration 31:40 minimum result,maximum result and avarage result same as Fig.2.

After a certain generation 50:140 the desired optimum results is 13 and nearest maximum results 24 are found in fig.3.The Fig.4 reflex minimum fitness in each generetion between iteration number 1 to 100 .The Fig.5 shows avarage fitness in each generation between 1 to 75.

After some generation mutation probability will be changed.We see when we increasing the mutation probability we can not get always optimum value but there is a probability.

CONCLUSION

We have followed survival of the fittest of Charles Darwin's theory. Main philosophy of genetic algorithm is followed to Holland. Circuit partition is one of the key

areas in chip designing. The algorithm can partition circuit into a number of sub-circuits. Our method calculates the fitness value and discards solutions with low fitness value. The increase in number of crossover points does not necessarily the fitness, as the fitness achieved depends on crossover as well as mutation probability.

The main advantage of the circuit partitioning using genetics algorithm is "we can easily multi way partitioning in many types of VLSI circuit".

Specially, in this paper find minimum cut size but not reduce the time.

REFERENCES

[1]. P.Mazumdar and K. Shahookar. "Genetics algorithms for VLSI design"

[2]. G.A.Vijaylakshmi Pai and S.Rajasekarna - "Genetic algorithms synthesis and application "

[3]. Dr.Ashwani Chandel, Dr.Rajeevan Chandel, Sandeep Sing Gill- "Genetic algorithms based circuit partitioning"

[4]. B.W.Kernighan and S-lin " An efficient heuristic procedure for partitioning Graph".

[5]. G. Wang, R.Kastner, W. Gang - "Application Partitioning on programmable platforms using Ant Colony Optimization", journal of Embedded Computing Vol.2 Issue 1, 2006.

[6]. Naveed Sherwani, "Algorithms for VLSI Physical Design and Automation", third edition, Springer (India) Private Limited, New Delhi, 2005

[7]. E. Mirhard, M.Anis, M. Elmary, P. Ghafari, S. Areibi- " A low power partitioning methodology by maximizing sleep time and minimizing cut nets", IWSOC, Bauf, Alberta,Canada,pp368-371, July,2005.

[8]. D. Kolar, Ivan Branica and J. Divokovic Puksec " VLSI Circuit partitioning using Simulated annealing Algorithm", IEEE Melecon, Dubrovnik, Croatia,May 12-15,2004.

[9]. D.E. Goldberg, "Genetic Algorithms in Search, Optimization and Machine learning", Pearson Education, 2004.

[10]. Frank Vahid ,Greg Stitt, Roman Lysecky "Dynamic Hardware software Partitioning: A First Approach" ACM/IEEE Design Automation Conference 2003, Anaheim, California, USA,pp 250-255, June 2-6, 2003.

[11]. Maurizio Palesi,Tony Givargis, "Multi-Objective Design Space Exploration Using Genetic Algorithms", Proceedings of the 10th international symposium on Hardware/software code sign, ACM Press, Estes Park, Colorado , .pp 67-72 ,2002.

[12]. C. Ababei, G. Karypis, K. Bazargan and S.Navaratnasothie "Multi-objective Circuit partitioning for Cutsize and path-base delay Minimization", IEEE International Conference on Computer aided Design, 2002.

[13]. S. Areibi, "Memetic Algorithms for VLSI Physical Design: Implementation Issues", Genetic and Evolutionary computation Conference, San Fransisco, California, pp140-145, July, 2001.

[14]. H.Youseff and S.M.Sait "VLSI Physical Design Automation", McGraw Hill Publishers, New Jersey, 1995.

[15]. Davis, L (1991), Handbook of genetic algorithms, New York Van Nostrand, Reinhold.

[16]. Jenkins, W.M. (1991), Towards structural optimization via the genetic Algorithms, Computers and Structures, Vol. 40, No. 5, pp. 1321-1327.

[17]. José Ignacio Hidalgo, Juan Lanchares, Roman Hermida - Graph partitioning methods for Multi-FPGA systems and Reconfigurable Hardware based on Genetic Algorithms, Computer Architecture Department, Spain.

