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Integration of Two Flyback Converters at Input PFC Stage for Lighting Applications

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ABSTRACT: An electronic driver with higher efficiency for lighting system is proposed in this paper. In the proposed converter, two flyback topologies are connected at the input stage with different polarity in order to avoid the input diode bridge rectifier. The design of proposed converter for 50W light emitting diode lamp is presented. In the proposed flyback, the numbers of switching devices are minimized when compared to other converter configurations found in the literature, thus reducing the conduction and switching losses and thereby increasing the efficiency of the converter. The output stage is boost converter circuit. The proposed converter is simulated using SIMULINK and the simulation results are presented in this paper to validate the proposed converter.

KEYWORDS: Electronic ballasts, Flyback converters, Lighting, Power factor correction (PFC).

I.INTRODUCTION

Electronic ballast is a device which uses solid state electronic circuit to control the starting voltage and operating currents of lighting device. It usually supplies power to the lamp at a frequency of 20 KHz or higher which eliminates the stroboscopic effect of flicker. By using electronic ballast, the efficiency and life of the lighting system can be improved. Light emitting diode (LED) sources are more compact, less dissipative and more durable, are finding more applications in domestic, commercial and industrial environments.



Fig. 1. (a) Block diagram of electronic ballasts for lighting systems (b) Block diagram of the proposed scheme for lighting systems

The block diagram of electronic ballast for lighting systems is shown in Fig 1(a). First stage is the diode bridge rectifier stage to convert AC (alternating current) to DC (Direct current). The rectifier stage is connected to the input power factor correction (PFC) stage. The input PFC stage supplies a capacitor which provides constant voltage across the output stage. The output stage is a DC-DC converter stage, used to supply lighting systems.

The block diagram of proposed scheme stages for lighting systems is shown in Fig 1(b). It consists of a Bidirectional input stage consisting of two Flyback converters with different polarities, in order to avoid the use of the diode bridge rectifier stage. The input stage supplies a capacitor, which provides constant voltage across the output stage. The output stage is a boost converter which supplies the lighting systems.

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II. LITERATURE SURVEY

In the literature, many topologies have been used for this input stage, which have some drawbacks. For example, the use of bridgeless high power factor buck converter as the input stage, although minimizes the number of conducting semiconductor components, works as a voltage doubler. As the output voltage is doubled, the switching losses of the primary switches of the output stage increases. Therefore, if an isolated input stage is used, the output voltage bus value can be made lower. The paper mainly deals with the use of Bidirectional flyback topology, to eliminate the use of diode bridge rectifier in order to improve the efficiency.

III.INPUT PFC STAGE

The PFC power topology presented in the paper is based on the integration of two flyback converters, one for each polarity of the line voltage, thereby completely eliminating diode bridge rectifier and avoiding the losses of input diode bridge rectifier. Here, the discontinuous conduction mode of the flyback is considered. The proposed topology is shown in the Fig. 2



Figure 2: Proposed input stage

A. Operation under Positive Input voltage

The operation can be explained in two modes

Mode 1: This mode begins when switch M_1 is turned ON. When the switch M_1 is turned ON, the input line voltage Vac is applied across the first primary winding of the transformer. The current through the primary inductor and switch increases with a rate of $V_{ac'} L_P$ where L_P is the inductance as seen from the primary. The magnetizing inductance of the transformer begins to charge during this period. From Fig 3(a), the diode D_1 is reverse biased and therefore no current flows through the secondary winding connected to D_1 .



(b) Mode 2 of positive line voltage



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Mode 2: This mode begins when switch M_1 is turned OFF. The magnetizing inductance discharges through the secondary side of the transformer, and the polarity of the winding reverses. The diode D_1 results in forward bias as shown in Fig 3(b). The stored inductor energy now flows through the secondary diode and into the capacitor and the load. The rate of this current is V_{ac}/L_s where L_s is the inductance as seen from the secondary.Once the magnetizing inductor of the flyback transformer is fully demagnetized, the diode D_1 results in reverse biased and no current flows through the transformer.

B. Operation under Negative Input voltage

The operation can be explained in two modes

Mode 1: This mode begins when switch M_2 is turned ON. When the switch M_2 is turned ON, the input line voltage Vac is applied across the second primary winding of the transformer. The current starts to build up and the magnetizing inductance of the transformer begins to charge. During this mode, the diode D_1 is reverse biased as shown in Fig. 4(a) and therefore no current flows through the secondary winding of the transformer.



Figure 4: (a) Mode 1 of negative input voltage (b) Mode 2 of negative input voltage

Mode 2: This mode begins when switch M_2 is turned OFF. The magnetizing inductance discharges through the secondary side of the transformer, and the polarity of the winding reverses. The diode D_1 becomes forward biased as shown in Fig 4(b) and current flows through the secondary winding connected to diode D_1 .

Once the magnetizing inductor of the flyback transformer is fully demagnetized, the diode D_1 results in reverse biased and no current flows through the transformer

IV.DESIGN DETAILS OF THE INPUT STAGE FOR 50W LED LAMP

The design inputs for input flyback stage are given in this section.

 $\dot{\eta}_{FLY} > 90\% \tag{1}$

$$f_{switch} = 100 KHz \tag{2}$$

$$V_{AC RMS MAX} = 276 V_{RMS} \tag{3}$$

$$V_{AC RMS MIN} = 92 V_{RMS}$$
(4)

$$d_{AC} = 0.5 \tag{5}$$

$$P_{FLY} = \frac{P_{LEDs}}{\dot{\eta}_{OUT}} = \frac{50}{0.9} = 55W$$
(6)





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Where η_{FLY} is the estimated efficiency of the flyback stage, f_{switch} is the switching frequency of the flyback stage, V_{AC} _{RMS} is the RMS value of the line input voltage, d_{AC} is the duty ratio of the input flyback stage, P_{FLY} is the required power output of the flyback stage, P_{LED} is the load power, η_{OUT} is the output stage efficiency.

The magnetizing inductance of the flyback converter can be given as

$$L_{\mu} \leq \frac{(V_{AC RMS MIN} \sqrt{2})^2 d_{AC}^2 \dot{\eta}_{FLY}}{4 P_{FLY} f_{switc h}}$$
(7)

Substituting the values in equation 7,

$L_{\mu} \leq 172 \, \mu H$

During Mode 2, the stored inductor energy transferred to the capacitor has to supply power *Po* to the load and also to replenish the energy lost by the capacitor during the previous Mode (Mode 1). Thus,

 $P_{FLY} T_S = (1/2)L_S (I_{S+}^2 - I_{S-}^2)$ (8) Where T_s is the switching period of the input flyback stage, L_s is the inductance as seen from the secondary, I_s is the current flowing through the secondary side of the transformer

ntinuous Mode,
$$I_{S-} = 0$$
 (9)
 $L_S = \frac{2P_{FLY}T_S}{I_{S+}^2}$ (10)
ate I_{S+} :-

<u>To calculate</u> I_{S+} :-

For disco

Desired power output of flyback stage $P_{FLY} = 55W$ Desired output voltage of flyback stage, $V = 70 V$	(11) (12)
Load Resistance of flyback stage $R = \frac{V^2}{P_{ELV}} = 89'\Omega$	(13)
Output current of flyback stage, $I_R = \frac{V}{R}$	(14)

Where V is the required output voltage of the flyback stage, P is the required power output of the flyback stage. From the circuit shown in the Fig. 2.

Diode current I_{S+} = Capacitor current + Resistor current

Assuming output capacitor $C = 47\mu F$ (16)

Hence
$$I_{S+} = 1.81 A$$
 (17)

$$L_S = 335 \,\mu H \tag{18}$$

$$L_{P1} = L_{p2} = \frac{V_{AC RMS}^2}{8P_{FLY} f_{Switc h}} X \,\dot{\eta}_{FLY}$$
(19)

$$= 1100 \,\mu H$$
 (20)

(15)

Where L_{P1} and L_{p2} are the inductances as seen from the primary.

V. OUTPUT STAGE

The CCM Boost converter is used as the output stage. The switching frequency considered is 100 KHz. The Circuit diagram of the Boost converter (output stage) is as shown in the Fig 5. When the MOSFET is turned ON, the inductor current rises and energy is stored in the inductor. If the MOSFET is turned OFF, the energy stored in the inductor is transferred to load (LED).

Input voltage $V_{IN} = 70V$

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Required output voltage = 140V



Figure 5: Proposed output stage

For Boost converter.

$$\frac{V_0}{V_{IN}} = \frac{1}{(1-D)}$$
 (21)

By substituting the values of V_0 and V_{IN} , the duty ratio of the boost converter is 0.5

Target power output of the boost converter W = 50watts(22)

Output current of the boost converter
$$I_{OUT} = \frac{W}{V_0} = \frac{50}{140} = 350 \, mA$$
 (23)

Load resistance of the boost converter
$$R = \left(\frac{V_0}{I_{OUT}}\right) = 400'\Omega$$
 (24)

The value of boost inductor,
$$L_{boost} \ge \frac{D(1-D)^2 X R}{2f} \ge 250 \mu H$$
 (25)
The value of the boost capacitor is calculated considering 10% output ripple voltage

of the boost capacitor is calculated considering 10% output ripple voltage

$$C_{boost} \geq \frac{D}{R X f (\Delta V_0 / V_0)} \geq 122 nF$$
(26)

Where R is the load resistance and f is the switching frequency of the boost converter

VI. SIMULATION RESULTS OF THE PROPOSED CONVERTER

A. Simulation results of the proposed input stage

The simulink model of the proposed input stage is shown in Fig 6. In the model, the simulation parameters for Lp₁ and Lp_2 are set to 1100 µH, $L_s = 335$ µH, C = 47µF.



Figure 6: SIMULINK Model of the proposed input stage

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The gate pulses required for MOSFET's M_1 and M_2 are obtained by comparing the sinusoidal waveform (reference signal) with the repetitive triangular waveform (carrier signal) in the relational operator block and the required pulses are generated at the output of the relational operator block as shown in Fig. 6. These gate pulses are needed to turn on MOSFET's M_1 and M_2 alternatively i.e during positive cycle of the applied voltage, the MOSFET M_1 is turned ON and during negative half cycle, the MOSFET M_2 is turned ON. The gate pulses given to MOSFET's M_1 and M_2 connected in the primary winding of the Flyback transformer is shown in Fig 7(a) and 7(b) respectively. The output voltage and current waveforms of Flyback stage is shown in Fig 7(c) and Fig 7(d) respectively



Figure 7: Simulation result waveforms of the input Flyback stage

The voltage magnitude required for output stage is 70 V, and the same is obtained at the output of the input flyback stage. From Fig. 7(c), it is evident that the required voltage of 70 V (steady state value) is obtained across the load resistance of the flyback stage and the same is applied to the output stage. Further, from Fig. 7(d), it is clear that the output current of 0.73A (steady state value) is obtained in order to get the desired output power.

B. Simulation Results of the output stage

The output voltage of 70 V which is obtained from input flyback stage is applied to the input terminals of the output stage. The SIMULINK model of the output stage (Boost converter) is shown in Fig. 8. The boost converter is needed to step up the voltage from 70V to 140V. The MOSFET in the output stage is turned ON and turned OFF with a switching frequency of 100 kHz. An output capacitor is used to reduce the ripple in the output voltage. The output voltage waveform of the Boost converter is shown in Fig. 9, it is observed that the input voltage 70V is increased to 140V which is desired voltage required to supply LED lighting system.



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Figure 8: SIMULINK Model of the Output stage

Figure 9: Output waveform of the Boost converter



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The complete simulink model of the proposed converter i.e along with input flyback stage and output stage is shown in Fig 10. From Fig. 10, it is clear that the complete setup has got two stages which are cascaded.



Figure 10: SIMULINK Model of proposed converter

VII. LOSSES AND EFFICIENCY OF THE PROPOSED CONVERTER

The various losses i.e conduction and switching losses of different components used in the proposed converter are determined from the practical considerations and are depicted in Table I.

From Table-1, it is clear that the total conduction losses across the diodes and MOSFET are 1.37 mW and 39.6 mW respectively. Further it is observed that the conduction losses occurred across the switching devices is less than the losses that are occurred across the secondary winding of the transformer. Moreover, the switching losses are found to be about 1.2 W.

Description	Related Equations	Value
Conduction losses in diode D1 of flyback stage for $I_d = 1.1A$, $R_{don} = 0.001\Omega$	$I_d^2 R_{don}$	1.21mW
Conduction losses in secondary winding of flyback transformer for $I_S = 1.1A$, $R_S = 2 \Omega$	$I_S^2 R_S$	2.42 W
Conduction losses in diode of the boost converter stage for I_d = 0.4A, R_{don} = 0.001 Ω	$I_d^2 R_{don}$	0.16mW
Conduction losses in MOSFET of the output boost converter for for $I_d = 0.6A$, $R_{don} = 0.11\Omega$	$I_d^2 R_{don}$	39.6mW
Switching losses in diode D_1 of flyback stage for $I_f = 1.1A$, $V_f = 0.8V$	$V_f I_f$	0.88 W
Switching losses in diode of boost converter stage for $I_f = 0.4A$, $V_f = 0.8V$	$V_f I_f$	0.32 W

Table I: Losses in various components of the proposed converter

Efficiency $\dot{\eta} = \frac{Power Output X 100}{Power Input} = 93.05\%$





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The conduction and switching losses of the proposed converter and converter [1] is given in Table II. From Table-II, it is clear that the conduction and switching losses of the proposed converter is lower than the losses of converter topology [1]. Hence, the efficiency of the proposed converter is higher than the converter [1]. Table III gives the efficiency of the proposed converter [1].

Table II: Conduction and switching losses				
	Conduction+	conduction+		
	switching losses of	switching losses		
	converter[1]	of proposed		
		flyback		
$V_{AC} = 230$				
V_{RMS} , 50 Hz	4.3 Watts	3.65 Watts		

ruble III. Converter Enterency				
	Efficiency of converter[1]	Efficiency of proposed flyback converter		
$V_{AC} = 230 V_{RMS}$, 50 Hz	91.9%	93.05%		

Table III: Converter Efficiency

VIII. CONCLUSION

An efficient electronic driver for lighting application has been designed and presented in this paper. The design for the proposed converter has been carried out for a 50 W LED lamp. The proposed converter circuit is designed and tested through SIMULINK. The efficiency and losses of the proposed converter are calculated using simulation results and it is found that the proposed converter configurations gives better efficiency as compared to the other converter topologies that has been presented in the literature. In the proposed converter, the number of switching components is minimized when compared to the other converter configurations. Hence the conduction and switching losses are minimised and thereby increasing the efficiency of the converter.

REFERENCES

- [1] Garcia, D Gacio, M.A. Dalla-costa and A.J. calleja, "A Novel Flyback- Based Input PFC Stage for Electronic Ballasts in Lighting Applications", IEEE Trans. Ind. Electron., vol. 49, no. 2, March/April 2013.
- Y. Jang and M. M. Jovanovic, "Bridgeless high-power-factor buck converter," IEEE Trans. Power Electron., vol. 26, no. 2, pp. 602–611, Feb. 2011.
- [3] W. Yan, S. Y. R. Hui, and H. Chung, "Energy saving of large-scale highintensity-discharge lamp lighting networks using a central reactive power control system," IEEE Trans. Ind. Electron., vol. 56, no. 8, pp. 3069–3078, Aug. 2009.
- [4] R. Orletti, M. A. Co, D. S. L. Simonetti, and J. L. de Freitas Vieira, "HID lamp electronic ballast with reduced component number," IEEE Trans. Ind. Electron., vol. 56, no. 3, pp. 718–725, Mar. 2009.
- [5] W. Kaiser, "Hybrid electronic ballast operating the HPS lamp at constant power," IEEE Trans. Ind. Electron., vol. 34, no. 2, pp. 319–324, Mar./Apr. 1998.
- [6] F. J. Azcondo, F. J. Diaz, C. Branas, and R. Casanueva, "Microcontroller power mode stabilized power factor correction stage for high intensity discharge lamp electronic ballast," IEEE Trans. Power Electron., vol. 22, no. 3, pp. 845–853, May 2007.
- [7] M. A. Dalla Costa, J. M. Alonso, J. C. Miranda, J. Garcia, and D. G. Lamar, "A single-stage high-power-factor electronic ballast based on integrated buck flyback converter to supply metal halide lamps," IEEE Trans. Ind. Electron., vol. 55, no. 3, pp. 1112–1122, Mar. 2008.

BIOGRAPHY

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