Linked State Machine Approach to Industrial Process Control Systems Design

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ABSTRACT: The use of microcontroller embedded systems in the design of industrial process control systems is limited by the level of complexities involved in actualizing a desired control automation. Adding intelligence and self diagnostic features to such systems usually increase the complexity of the machine. This paper studies the *Linked-State Machine* approach as a design alternative to overcome the challenges of designing complex industrial process control systems. The complexity of an intelligent class C water level and temperature control system with self diagnoses is simplified by breaking the system into three simpler class A machines. Each of the three simple machines is designed separately as embedded systems by looking at the Algorithm State Machine (ASM), the State Transition Table (STT) and the linked path Addressable ROM structure model for the Hardware implementation. The three simple machines are then linked together as State Machines to actualize the desired operation of the original complex system.

I.INTRODUCTION

Industrial intelligence suggests that a system of industrial process should be designed to exhibit well defined level of automation that should ensure:-

- Accurate monitoring of process involved.
- Self diagnosis in the event of fault.

In designing an intelligence process control system, a number of design approaches can be adopted. The level of intelligence built in the system determines the complexity of the machine, which determines the most suitable approach to use.

A simple microcontroller based design can achieve a very good level of automation and intelligence, but will lead to a lot of complexity with higher level of intelligence. A good approach to ease the design of complex systems is to break the system into a number of smaller systems (or modules) which can be linked together to give the desired intended system.

II. A TYPICAL PROCESS CONTROL SYSTEM:

Consider a system under design, where the parameters of interest are resource level and temperature. The process control system is expected to be equipped with a microcontroller based liquid level and temperature control system as well as automatic self-diagnostic features. This system is expected to serve an industrial set-up where a reservoir tank supplies a feeder tank from which water can now be dispensed or collected at a given temperature. As already stated above, the system should be equipped with some level of intelligence to enable it detect when a faulty condition occurs in the process flow and even suggest possible solution(s). i.e. it will have self diagnostic capabilities.

The control algorithm for the above system is represented by the ASM chart of fig.1. The rectangular boxes in the ASM chart of fig.1 are state boxes with the state names indicated by the circular inscription of numbers by the side of each box. Other forms of outputs as indicated by the oblong boxes like the UMDLTRG, VLVTST1, HTRTSTTRG and UTNKTRG are conditional outputs each of which triggers a retriggarable monostable timer, whose output goes HIGH

for the desired time interval. In effect, the ASM chart of fig.1 has six state outputs namely UTNKEMPTY, HVALVE 1, VLV1FLT, HEATER and HVALVE 2. In addition to the outputs, it also has four conditional outputs namely: - UTNKTRG, UMDLTRG, VLV1TST and HTRTSTTRG. It is important to note at this point, that it is on these four conditional outputs that the intelligence and self diagnostic features of this control system is anchored.
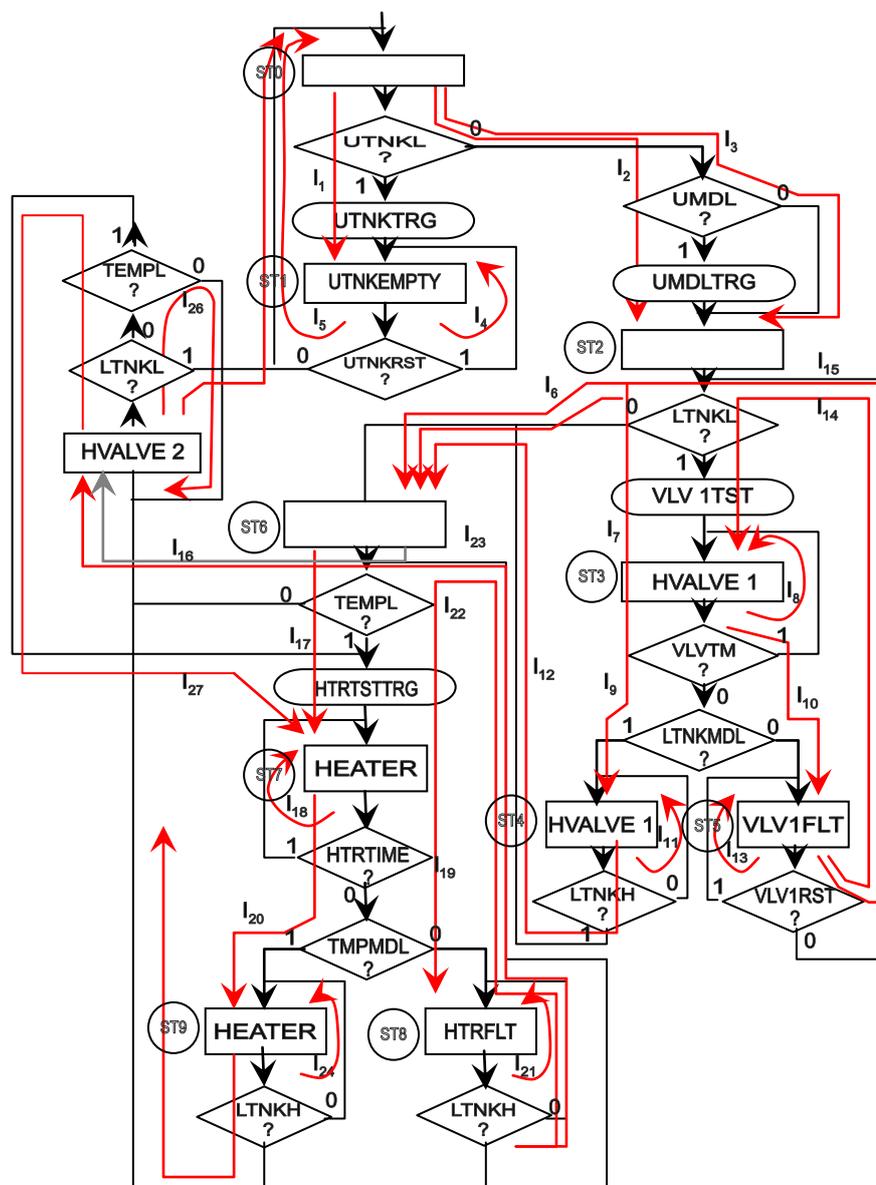
Fig. 1: Automatic / Intelligent water level and Temperature process control system with self diagnostic features.

Figure 1 shows the ASM chart of the process control system with the link paths between states clearly indicated.

The state codes of the system are generated with the help of the state map as shown below in tables 1a and 1b.

Table 1a: State Map

ST0	ST7	ST8	*
ST1	ST6	ST9	*
ST2	ST5	ST10	*
ST3	ST4	*	*

Table 1b:State Assignments

State Name	STATE CODE			
	D	C	B	A
ST0	0	0	0	0
ST1	0	0	0	1
ST2	0	0	1	1
ST3	0	0	1	0
ST4	0	1	1	0
ST5	0	1	1	1
ST6	0	1	0	1
ST7	0	1	0	0
ST8	1	1	0	0
ST9	1	1	0	1
ST10	1	1	1	1

NOTE: With the help of the karnaugh map, the state map is obtained by inserting the state names serially in adjacent cells whose codes are chosen such that only one bit changes level as one progresses from one state of the control system to the other, as clearly represented in the resulting state assignment of Table 1b.

III.THE STATE TRANSITION TABLE FOR THE INTELLIGENT SYSTEM

As already stated, every ASM chart has an equivalent tabular representation known as state transition table (STT). The state transition table for the intelligent control system is presented in table 2. This is the tabular representation of the information contained in the ASM chart of fig 1. As usual, every data row under the table's column headings corresponds to a link path. In effect, just as 28 link paths fully describe the ASM chart, so also does the STT have 28 data rows, one row per link path.

The state transition table for the above system has eight main column as follows;-
1. The link path column featuring L1through L28.
2. The input qualifies column; UTNKL, UTNKRST, UMDL, LTNKL, VLVTM, LTNKMDL, VLV1RST, TEMPL, HTRTIME, TMPMDL, HTRRST, UTEMP.
3. The present state name featuring ST0 through ST10.
4. The present state code featuring DCBA=0000, 0001, 0011 e.t.c.
5. The NEXT state name featuring ST0 through ST10.
6. The NEXT state code featuring D`C`B`A`=0001, 0011, 0001, 0000 e.t.c.
7. The state outputs; - UTNKEMPTY, HVLVE1, VLV1FLT, HEATER, HTRFLT, HVALVE 2.
8. The conditional outputs;- UTNKTRG, UMDLTRG, VLV1TST and HTRTSTTRG.

IV. FULLY EXPANDED STATE TRANSITION TABLE FOR THE INTELLIGENT SYSTEM

The STT of table 1 expectedly contains a number of dashes under the columns headed by the input qualifiers. These dashes normally imply two things:-

1. That the input qualifier above that column is not relevant for the transition being made in the link path where the dash appeared.
2. That the input qualifier heading above the dash may be at logic 0 without affecting the control process at that material time.

Irrespective of the above design implications, it is important to accommodate all the possible combinations of logic values that can present its self in the design, considering the fact that to program a ROM, one need to define all (address) inputs including qualifiers as either 0 or 1 and none as a dash.

The state transition table (STT) of table 4.9 would be fully expanded when all the dashes on each row are given all possible combinations of logic values, leading to new rows in the STT, one for each combination of logic values for the dashes on that row. The implication here is that a total of 46080 rows would be required to fully expand the state transition table for the system

Ie.
$$= (2^{10} \times 11) + (2^{11} \times 17)$$
$$= (1024 \times 11) + (2048 \times 17)$$
$$= 11264 + 34816$$
No of rows required = 46080

This is a very large number of rows to deal with manually and of course presents a very complex class C machine to design using this approach. Even when a software approach is used for generating the rows and obtaining the expanded STT, the complexity of the resulting machine will make it prone to possible and inevitable design errors as well as difficulty in maintainability.

V. LINKED STATE MACHINE APPROACH

It is possible to break the complex class C machine represented by the ASM chart of fig1 into simpler machines of class A category and then link the simple machines together to actualize the overall operation of the original complex machine. The machine can be separated into three simple machines as follows;-

1. The upper tank control system.
2. The lower tank control system.
3. The heater control system.

Each of these three simple machines can now be developed with each fully automated and intelligent enough to handle diagnostic features. The three can then be linked together to effect full operation of the complex machine earlier conceived.

VI.THE UPPER TANK CONTROL SYSTEM

The upper tank control system is designed to monitor the state of the upper tank that constantly supplies the lower distribution tank with resource whenever it is needed. It is therefore expected that the system should be able to monitor the state of the valve that controls its supply and report eventual fault conditions and also know when to supply resource to the lower tank. Control algorithm for the sub-system is represented by the ASM chart of fig2 with the link paths included.
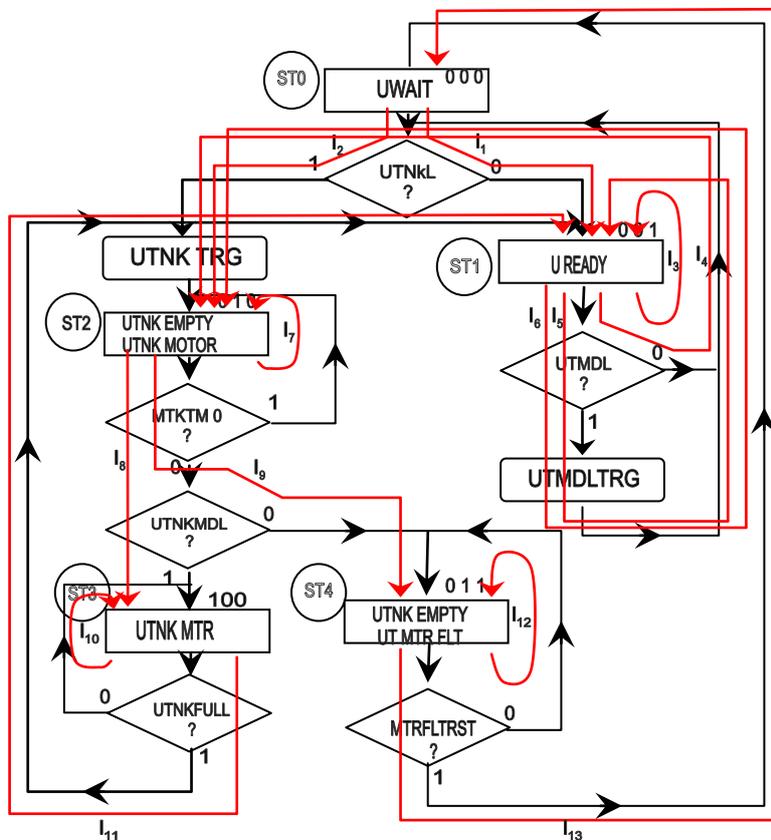
Fig.2: ASM Chart for the Upper Tank Control System

Figure 2 shows the ASM chart representation of the Upper Tank control unit as a sub-unit of the original complex system being designed.

VII. THE STATE TRANSITION TABLE FOR THE UPPER TANK CONTROL SYSTEM

The state transition table for the upper tank control system, which is an equivalent tabular representation of the ASM chart of fig 2 is developed in table 2 with the necessary columns clearly stated.

Table 2: State Transition Table for Upper Tank Control

LINK PATHS	UTNKL UTMDL MTRTIMO UTNKFULL MTRFLTRST	PRESENT STATE NAME	PRESENT STATE CODE C B A	NEXT STATE NAME	NEXT STATE CODE $C^I B^I A^I$	UTNKWAIT UREADY UTNKEMP / MTR UTNK MTR UTNKEMP / MTRFLT
L1	0 - - - -	ST 0	0 0 0	ST 1	0 0 1	1 0 0 0 0
L2	1 - - - -	ST 0	0 0 0	ST 2	0 0 1	1 0 0 0 0
L3	- 0 - - -	ST 1	0 0 1	ST 1	0 0 1	0 1 0 0 0

L4	1 0 - - -	ST 1	0 0 1	ST 2	0 1 1	0 1 0 0 0
L5	- 1 - - -	ST 1	0 0 1	ST 1	0 0 1	0 1 0 0 0
L6	1 1 - - -	ST 1	0 0 1	ST 2	0 1 1	0 1 0 0 0
L7	- - 1 - -	ST 2	0 1 1	ST 2	0 1 1	0 0 1 0 0
L8	- 1 0 - -	ST 2	0 1 1	ST 3	0 1 0	0 0 1 0 0
L9	- 0 0 - -	ST 3	0 1 0	ST 4	1 1 0	0 0 1 0 0
L10	- - - 0 -	ST 3	0 1 0	ST 3	0 1 0	0 0 0 1 0
L11	- - - 1 -	ST 3	0 1 0	ST 1	0 0 1	0 0 0 1 0
L12	- - - 0 -	ST 4	1 1 0	ST 4	1 1 0	0 0 0 0 1
L13	- - - 1 -	ST 4	1 1 0	ST 0	0 0 0	0 0 0 0 1

VIII. EXPANDED STATE TRANSITION TABLE FOR THE UPPER TANK CONTROL:

As usual, for a ROM based design approach, the above STT for the Upper tank Control, should be expanded to accommodate all the possible states of the system based on the outputs of the input qualifiers. Table 3 shows the expanded STT for the upper tank control up to link-path **L5**.

Table3: Expanded STT for the Upper Tank Control System.

LINK PATHS	Location Address (Hex)	UTNKL	UTMDL	MTRTIMO	UTNKFULL	MTRFLTRST	C	B	A	UTNKWAIT	UREADY	UTNKEMP / MTR	UTNK MTR	UTNKEMP / MTRFLT	C	B	A	Location Content (Hex)
L1	00	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	30
	08	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0	0	30
	10	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0	30
	18	0	0	0	1	1	0	0	0	0	0	1	1	0	0	0	0	30
	20	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	30
	28	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	30
	30	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0	30
	38	0	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	30
	40	0	1	0	1	0	0	0	0	0	0	1	1	0	0	0	0	30
	48	0	1	0	1	0	0	0	0	0	0	1	1	0	0	0	0	30
	50	0	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	30
	58	0	1	0	1	1	0	0	0	0	0	1	1	0	0	0	0	30
	60	0	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	30
	68	0	1	1	0	1	0	0	0	0	0	1	1	0	0	0	0	30
	70	0	1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	30
	78	0	1	1	1	1	0	0	0	0	0	1	1	0	0	0	0	30
L2	80	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	70
	88	1	0	0	1	0	0	0	0	0	1	1	1	0	0	0	0	70
	90	1	0	0	1	0	0	0	0	0	1	1	1	0	0	0	0	70
	98	1	0	0	1	1	0	0	0	0	1	1	1	0	0	0	0	70

	Code	Byte 1	Byte 2	Val
	A0	1 0 1 0 0 0 0 0	0 1 1 1 0 0 0 0	70
	A8	1 0 1 0 1 0 0 0	0 1 1 1 0 0 0 0	70
	B0	1 0 1 1 0 0 0 0	0 1 1 1 0 0 0 0	70
	B8	1 0 1 1 1 0 0 0	0 1 1 1 0 0 0 0	70
	C0	1 1 0 0 0 0 0 0	0 1 1 1 0 0 0 0	70
	C8	1 1 0 0 1 0 0 0	0 1 1 1 0 0 0 0	70
	D0	1 1 0 1 0 0 0 0	0 1 1 1 0 0 0 0	70
	D8	1 1 0 1 1 0 0 0	0 1 1 1 0 0 0 0	70
	E0	1 1 1 0 0 0 0 0	0 1 1 1 0 0 0 0	70
	E8	1 1 1 0 1 0 0 0	0 1 1 1 0 0 0 0	70
	F0	1 1 1 1 0 0 0 0	0 1 1 1 0 0 0 0	70
	F8	1 1 1 1 1 0 0 0	0 1 1 1 0 0 0 0	70
L3	01	0 0 0 0 0 0 0 1	0 0 1 0 1 0 0 0	28
	09	0 0 0 0 1 0 0 1	0 0 1 0 1 0 0 0	28
	11	0 0 0 1 0 0 0 1	0 0 1 0 1 0 0 0	28
	19	0 0 0 1 1 0 0 1	0 0 1 0 1 0 0 0	28
	21	0 0 1 0 0 0 0 1	0 0 1 0 1 0 0 0	28
	29	0 0 1 0 1 0 0 1	0 0 1 0 1 0 0 0	28
	31	0 0 1 1 0 0 0 1	0 0 1 0 1 0 0 0	28
	39	0 0 1 1 1 0 0 1	0 0 1 0 1 0 0 0	28
	81	1 0 0 0 0 0 0 1	0 0 1 0 1 0 0 0	28
	89	1 0 0 0 1 0 0 1	0 0 1 0 1 0 0 0	28
	91	1 0 0 1 0 0 0 1	0 0 1 0 1 0 0 0	28
	99	1 0 0 1 1 0 0 1	0 0 1 0 1 0 0 0	28
	A1	1 0 1 0 0 0 0 1	0 0 1 0 1 0 0 0	28
	A9	1 0 1 0 1 0 0 1	0 0 1 0 1 0 0 0	28
	B1	1 0 1 1 0 0 0 1	0 0 1 0 1 0 0 0	28
	B9	1 0 1 1 1 0 0 1	0 0 1 0 1 0 0 0	28
L4	81	1 0 0 0 0 0 0 1	0 1 1 0 1 0 0 0	68
	89	1 0 0 0 1 0 0 1	0 1 1 0 1 0 0 0	68
	91	1 0 0 1 0 0 0 1	0 1 1 0 1 0 0 0	68
	99	1 0 0 1 1 0 0 1	0 1 1 0 1 0 0 0	68
	A1	1 0 1 0 0 0 0 1	0 1 1 0 1 0 0 0	68
	A9	1 0 1 0 1 0 0 1	0 1 1 0 1 0 0 0	68
	B1	1 0 1 1 0 0 0 1	0 1 1 0 1 0 0 0	68
	B9	1 0 1 1 1 0 0 1	0 1 1 0 1 0 0 0	68
L5	41	0 1 0 0 0 0 0 1	0 0 1 0 1 0 0 0	28
	49	0 1 0 0 1 0 0 1	0 0 1 0 1 0 0 0	28
	51	0 1 0 1 0 0 0 1	0 0 1 0 1 0 0 0	28
	59	0 1 0 1 1 0 0 1	0 0 1 0 1 0 0 0	28
	61	0 1 1 0 0 0 0 1	0 0 1 0 1 0 0 0	28
	69	0 1 1 0 1 0 0 1	0 0 1 0 1 0 0 0	28
	71	0 1 1 1 0 0 0 1	0 0 1 0 1 0 0 0	28
	79	0 1 1 1 1 0 0 1	0 0 1 0 1 0 0 0	28
	C1	1 1 0 0 0 0 0 1	0 0 1 0 1 0 0 0	28
	C9	1 1 0 0 1 0 0 1	0 0 1 0 1 0 0 0	28
	D1	1 1 0 1 0 0 0 1	0 0 1 0 1 0 0 0	28
	D9	1 1 0 1 1 0 0 1	0 0 1 0 1 0 0 0	28

	E1	1 1 1 0 0 0 0 1	0 0 1 0 1 0 0 0	**28**
	E9	1 1 1 0 1 0 0 9	0 0 1 0 1 0 0 0	**28**
	F1	1 1 1 1 0 0 0 1	0 0 1 0 1 0 0 0	**28**
	F9	1 1 1 1 1 0 0 1	0 0 1 0 1 0 0 0	**28**

IX. THE LINK PATH ADDRESSABLE ROM STRUCTURE FOR THE UPPER TANK CONTROL SUB SYSTEM

Having obtained the Location Address and the Location Content for the upper tank control system form the expansion of the STT, the Hardware implementation of the upper tank control system can now be implemented using the link path addressable ROM structure model by setting up as ROM address, the value under LOCATION ADDRESS (HEX), one at a time and storing in each address the corresponding value under the LOCATION CONTENT (HEX) column.

Fig 3 shows in block diagram form, how the link path addressable ROM structure would be for the hardware implementation of the upper tank control system:
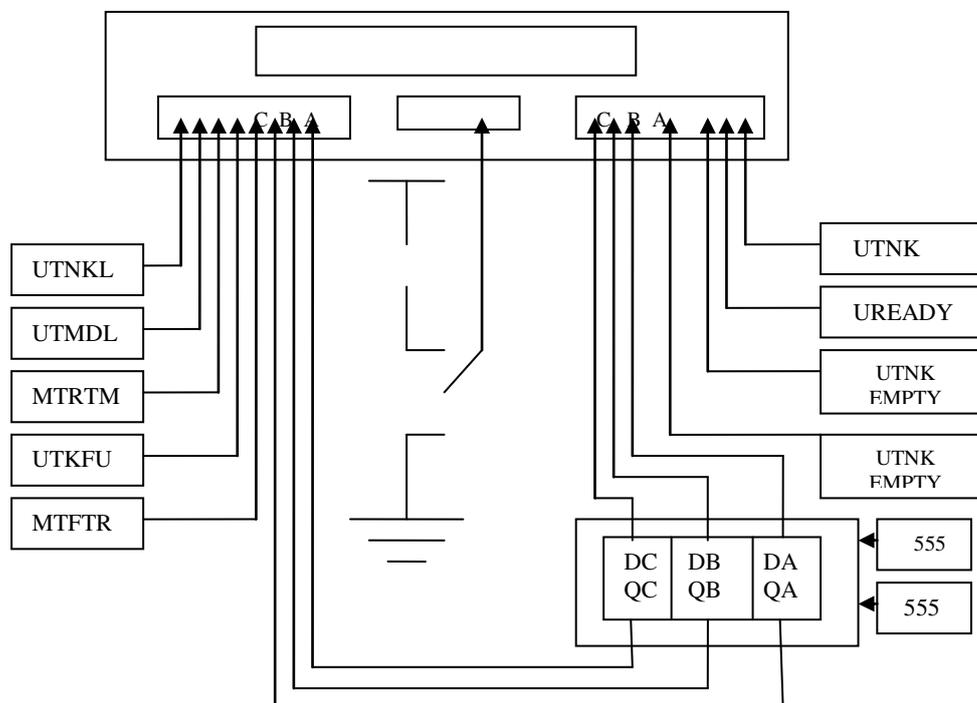
Fig 3: Rom Structure Model for the Upper Tank control system.

The same process as in 6,7,8 and 9 are repeated for the lower tank control system as well as the Heater control system. This means that the control algorithm, the algorithm state machine [ASM] chart, the state transition table (STT) as well as the fully expanded STT for the lower tank and the Heater systems is developed and from there the link path addressable ROM structure for the Hardware implementations designed.

X. CONTROL ALGORITHM FOR THE LOWER TANK CONTROL SYSTEM

The lower tank control system is linked to the upper tank control system such that it is intelligent enough to know when it is running out of resource and needed to be supplied by the upper tank. For it to be able to do this, it is equipped with enough intelligence to monitor the state of the upper tank as well as its own. It also has the capability of controlling the

opening and closing of the supply valve to this effect and is able to carry out diagnostic check on the condition of the valves. The control algorithm to implement these features is presented as an ASM chart in figure4
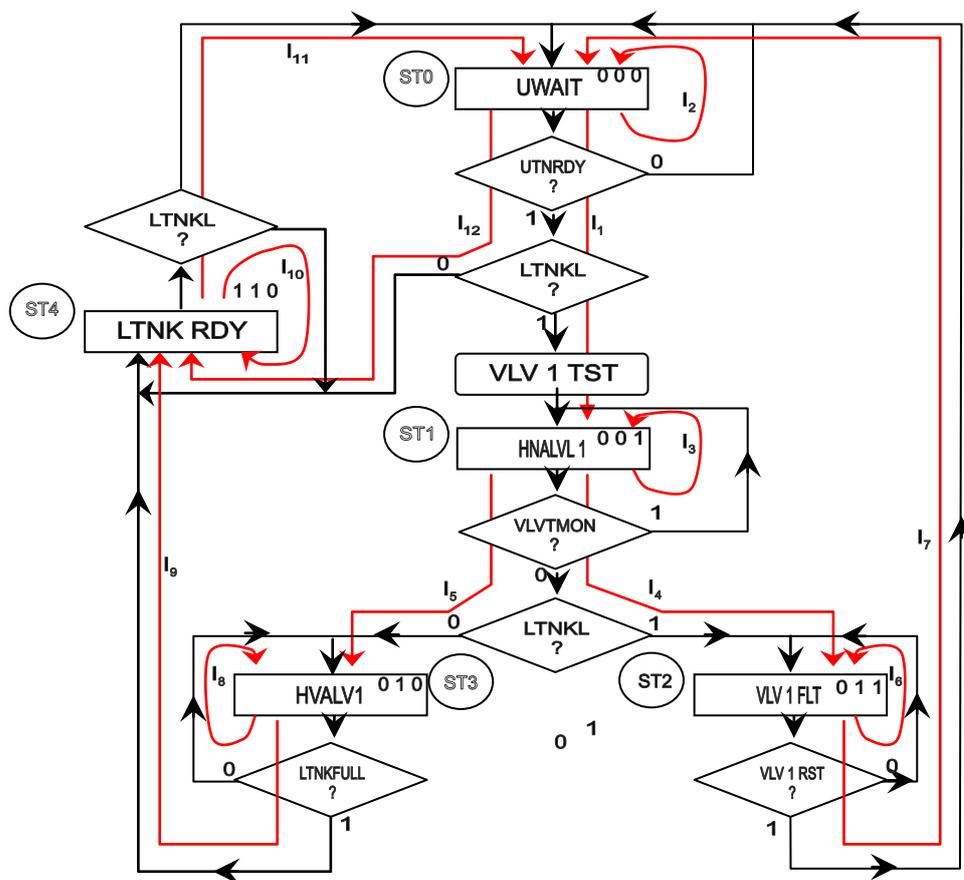
Fig. 4: ASM chart for the Lower Tank Control System

Figure 4 shows the ASM chart representation of the Lower Tank control unit as a sub-unit of the original complex system being designed. Also indicated are the various states and link paths that connect to constitute the logical operation of the sub-system.

XI. STATE TRANSITION TABLE FOR LOWER TANK CONTROL

From the ASM chart of figure 4, the STT for the Lower Tank Control is obtained as presented in table 4. The STT is expanded and the Hardware implemented exactly as in the case of the Upper Tank Control, using the link path addressable ROM structure model.

Table 4: STT for the Lower Tank Control System.

LINK PATHS	UREADY LTNKL VLVTMO VLV 1 RST LTNKFULL	PRESENT STATE NAME	PRESENT STATE CODE C B A	NEXT STATE NAME	NEXT STATE CODE $C^I B^I A^I$	UWAIT HVALV 1 VLV 1 FLT LTNK RDY
L1	1 1 - - -	ST 0	0 0 0	ST 1	0 0 1	1 0 0 0
L2	0 - - - -	ST 0	0 0 0	ST 0	0 0 0	1 0 0 0
L3	1 0 - - -	ST 0	0 0 0	ST 4	1 1 0	1 0 0 0
L4	- - 1 - -	ST 1	0 0 1	ST 1	0 0 1	0 1 0 0
L5	- 1 0 - -	ST 1	0 0 1	ST 2	0 1 1	0 1 0 0
L6	- 0 0 - -	ST 1	0 0 1	ST 3	0 1 0	0 1 0 0
L7	- - - 0 -	ST 2	0 1 1	ST 2	0 1 1	0 0 1 0
L8	- - - 1 -	ST 2	0 1 1	ST 0	0 0 0	0 0 1 0
L9	- - - - 0	ST 3	0 1 0	ST 3	0 1 0	0 1 0 0
L10	- - - - 1	ST 3	0 1 0	ST 4	1 1 0	0 1 0 0
L11	- 0 - - -	ST 4	1 1 0	ST 4	1 1 0	0 0 0 1
L12	- 1 - - -	ST 4	1 1 0	ST 0	0 0 0	0 0 0 1

XII. THE HEATER CONTROL SYSTEM;

Once the lower tank is ready with resource, the overall system control is transferred to the heating section of the process. The heater control system like the other sub systems is equipped with adequate intelligence and self diagnostic features to ensure that the heater is always in good working condition. To this effect, the control algorithm for the Heater Control System is presented as an ASM chart of fig 5 while the state transition table is as shown in table 5.
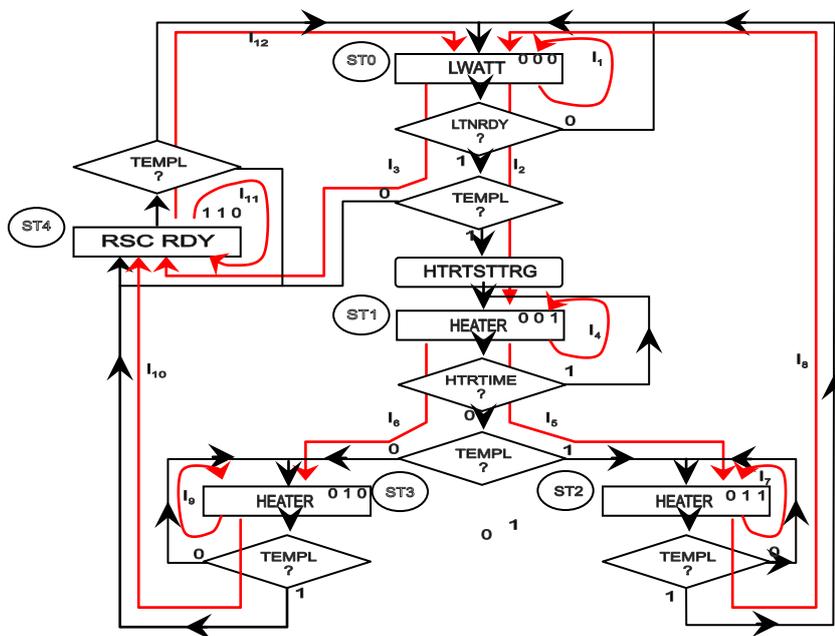
Fig. 5: ASM chart for the Heater Control System

Figure 5 shows the ASM chart representation of the Heater control unit as a sub-unit of the original complex system being designed.

Table 5: State Transition Table For Heater Control System

LINK PATHS	LTN K RDY TEMPL HTRTIME HTR RST UTEMP	RESENT STATE NAME	PRESENT STATE CODE C B A	NEXT STATE NAME	NEXT STATE CODE C^I B^I A^I	LWAIT HEATER HTR FLT RSC RDY
L1	0 - - - -	ST 0	0 0 0	ST 0	0 0 0	1 0 0 0
L2	1 1 - - -	ST 0	0 0 0	ST 1	0 0 1	1 0 0 0
L3	1 0 - - -	ST 0	0 0 0	ST 4	1 1 0	1 0 0 0
L4	- - 1 - -	ST 1	0 0 1	ST 1	0 0 1	0 1 0 0
L5	- 1 0 - -	ST 1	0 0 1	ST 2	0 1 1	0 1 0 0
L6	- 0 0 - -	ST 1	0 0 1	ST 3	1 1 0	0 1 0 0
L7	- - - 0 -	ST 2	0 1 1	ST 2	0 1 1	0 0 1 0
L8	- - - 1 -	ST 2	0 1 1	ST 0	0 0 0	0 0 1 0
L9	- - - - 0	ST 3	0 1 0	ST 3	0 1 0	0 1 0 0
L10	- - - - 1	ST 3	0 1 0	ST 4	1 1 0	0 1 0 0
L11	- 0 - - -	ST 4	1 1 0	ST 4	1 1 0	0 0 0 1
L12	- 1 - - -	ST 4	1 1 0	ST 0	0 0 0	0 0 0 1

XIII.

LINKING THE SUBSYSTEMS

Having developed the three subsystems as three separate simple machines, each fully equipped with adequate intelligence and self diagnostic features that will ensure complete functionality of the original complex system, the three simple machines can now be linked together to function as one complete system. Block diagram of the resultant Linked State Machine is shown in figure 6.
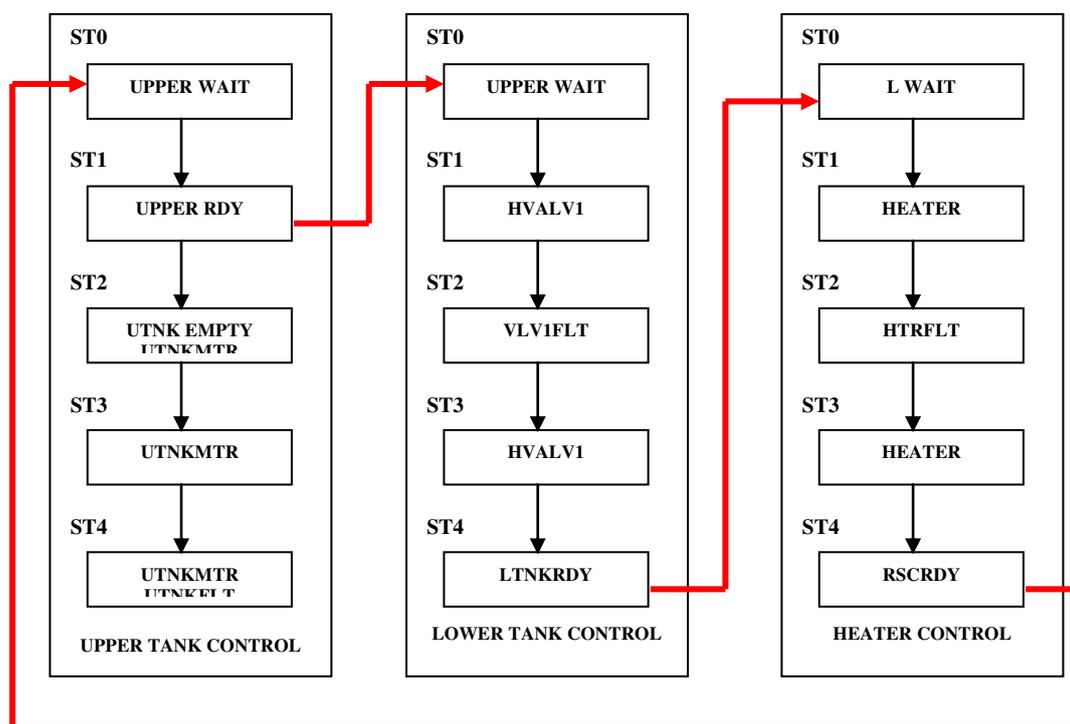
Fig. 6: Block diagram of the System as Linked State Machine.

Figure 6 shows the block diagram of the resultant system as three simple sub systems logically linked together to achieve the originally intended system.

XIV. CONCLUSION

A detailed approach to the design of complex industrial process control system is presented to show how machine complexities can be simplified in design. Increase in the functional features of control systems increases the complexities of such system and when such is the case, it is possible to break such machine into subsystems of simpler machines which can now be linked together to actualize the full potential of the originally intended system.

The author presented a detailed example showing how giving parameters of interest in a typical process control system were monitored and controlled by separate simple control systems which are now linked together to bring about a complete process control system.

Although link-state machine approach in design of process control systems suggests the development of multiple systems with implications of higher cost of production and resource usage, it is a very efficient way of dealing with machine complexities which would have been very difficult to handle.

REFERENCES

[1].   Inyiama H.C and Okezie C.C, "Designing microcontroller based universal process control systems" Electroscope: international journal of Electrical & Telecommunication systems Research, vol. 2, no. 1 pp 11-26, November, 2007.
[2].   C.R Clare, "Designing logic systems using state machines" MacGraw-Hill, UK. 1973.
[3].   Mancharka A.V, Behere S.H , " Intelligent Universal Sensor Interface development using microcontrollers" Dept. of Electronic Science, NAC & S.C College Alimednegar, India, 2005.
[4].   Ingham, M.D, Rasmussen, R.D, et.al. "Engineering Complex Embedded Systems with State Analysis and the Mission Data System", AIAA Intelligent Systems Technical Conference, Chicago, IL, 2004.
[5].   Melin, P. and Castillo, O., Hybrid Intelligent Systems, Springer-Verlag Berlin Heidelberg, New York, NY, 2005.
[6].   Akpado K.A, Inyiama H.C, and Okezie C.C; " Simplifying Industrial Process Control monitoring Using Linked State Machine Approach," international journal of Electrical and Telecommunication system research, Vol. 4, No. 4, 2011.
[7]   H.C Inyiama, Unpublished Lecture Notes on Microcontroller based Process Control Systems, Department of Electronic and Computer Engineering , Nnamdi Azikiwe University Awka, 2010.