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Low Power Design of Schmitt Trigger Based SRAM Cell Using NBTI Technique

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ABSTRACT: In this paper we are going to modify the Schmitt Trigger based SRAM cell using Negative Bias Temperature Instability (NBTI) for the purpose of more reduced power than the existing type of designs. As well as the new design which is combined of virtual grounding with read error reduction logic is compared with existing Schmitt trigger based SRAM technologies. Negative bias temperature instability (NBTI) is an important lifetime reliability problem in microprocessors. The Schmitt Trigger operation gives better read-stability as well as enhanced write-ability compared to the standard 6T bit cell. The aim of this project is to develop a circuit level technique that takes advantage of program behavior to reduce power consumption with no performance degradation. These simulations are implemented by the mentor graphics tool.

I. INTRODUCTION

To attain higher density performance and lower power consumption, CMOS devices have been scaled for more than 30 years. Transistor delay times decrease by more than 30% per technology

Generation, resulting in doubling of microprocessor performance every two years. The main intention of this work focuses on the reduction of power consumption in SRAM cells. This paper presents a low power consumption SRAM cell and array architecture targeting high performance, low power embedded memory. For reducing the power consumption at the circuit, architectural and system level we are introducing various techniques at the different levels in the designing process.

In the designing of the system we are using SRAM or DRAM memories. SRAM or Static Random Access Memory is a form of semiconductor memory widely used in electronics, Microprocessor and general computing applications. This form of semiconductor memory gains its name from the fact that data is held in there in a static fashion, The main reasons are its design tradeoffs include density, speed, volatility, cost and custom features. SRAMs are mostly used in the circuit designs for its efficiency and cost is overhead. Since SRAM cells are high power consuming elements so we introducing the Schmitt Trigger based designs to remove the unwanted power consumption. In the transactions of SRAM cell requires minimum voltage for its operation [2], then it will search for Vmin. This will leads to delay in the circuit operation and gives the power leakage from the design. To reduce this type of power leakage and delays in the circuit we are introducing the new design. If the operating voltage of the design is reduces, it leads to reduction in the power dissipation, then stability of the SRAM cell is disturbed. So the SRAM cell will not operates the read and write operations properly. For getting better stability we are introducing 8T/10T SRAM cells [7].

This paper demonstrates the power consumption of various models of SRAM cell with feedback mechanism circuit technique. All the circuit simulations have been done using mentor graphics tool. Finally, the analysis of the power consumption of various SRAM designs with the proposed design is shown. To increase the read stability extra peripheral circuitry can be added to 6T SRAM bit cell at the cost of increased area overhead and power consumption. Several SRAM bit cell topologies have been proposed in the recent past to improve read stability.

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II. STANDARD 6T SRAM CELL

The CMOS 6T SRAM bit cell design is shown in figure 1. 6T cell is most widely used in embedded memory because of its fast access time and comparatively small area [1]. The standard 6T SRAM cell forms two cross-coupled inverters. Which are controlled by the word line (WL) signal, This storage cell has two stable states which are used to denote 0 and 1.during the read operation the '0' storing node voltage is disturbed which might flip the stored data. For reliable read operation the design requirement is such that the data should not be flipped

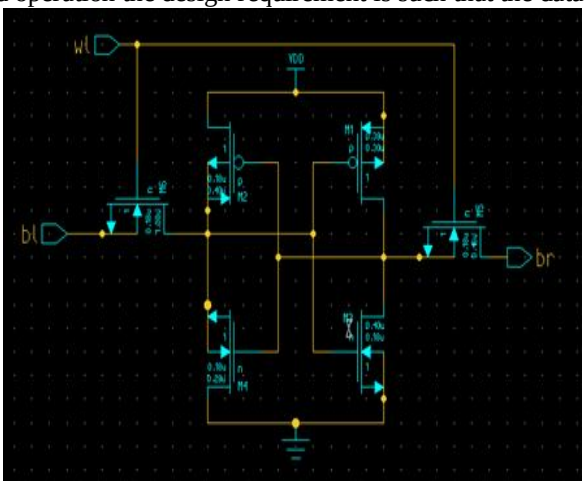

Figure1: Standard 6T SRAM CELL

During write operation the design recruitment is such that the data should be flipped as easily as possible. In order to tenacity the read versus write operation in the 6T cell, we apply Schmitt trigger principle for the cross -coupled inverter pair. A Schmitt trigger principle is used to vary the switching threshold of an inverter depending on the direction of input transition

III. SCHMITT TRIGGER PRINCIPLE

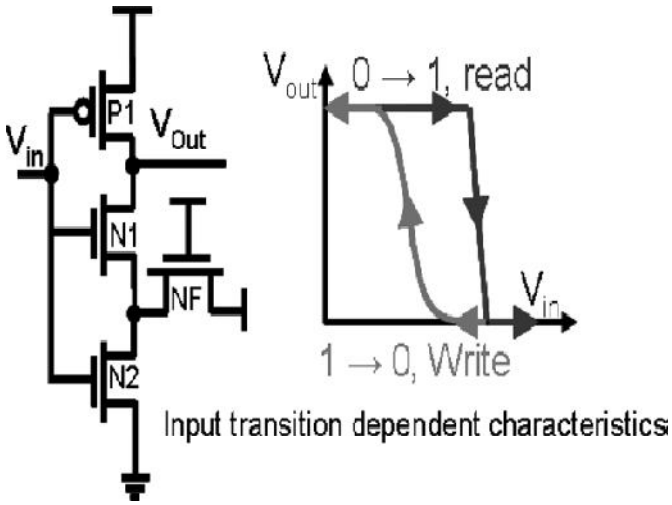

Figure2: Basic Schmitt trigger

In order to resolve the read versus write conundrum in the 6T cell, we apply Schmitt trigger principle for the cross coupled inverter pair. A Schmitt trigger is used to modulate the switching threshold of an inverter depending on the direction of the input transition. In the proposed Schmitt trigger SRAM cell, the feedback mechanism is used only in the pull down path as Shown in Fig. 2. During 0 to 1 input transition, the feedback transistor tries to preserve the logic

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'1' at output (Vout) node by raising the source voltage of pull down NMOS (N1). These Consequences in higher switching threshold of the inverter with very sharp transfer characteristics. For the 1 to 0 input transition the feedback mechanism is not present. This results in smooth transfer characteristics essential for easy write operation. Thus input dependent transfer characteristics of the Schmitt trigger improves both read-stability as well as write–ability of the SRAM cell. the Schmitt Trigger (ST) cell is in termed as "ST-1" bit cell while the other Schmitt Trigger bit cell is termed as 'ST-2" bit cell.

IV. EXISTING TECHNIQUES

ST-1 Bit cell:

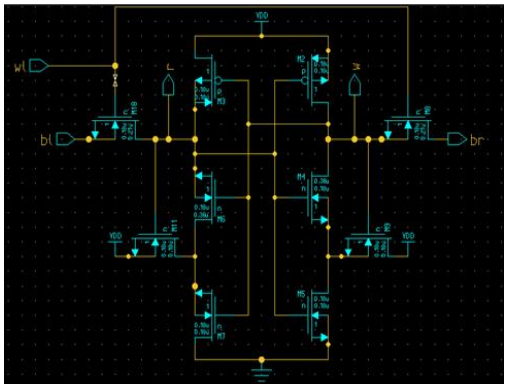

Figure3: Schmitt trigger-1 Bit cell

Fig. 3 shows the schematics of the ST-1 bit cell. The ST-1 bit cell utilizes differential sensing with ten transistors, one word-line (WL), and two bit lines (BL/BR). Transistors M2-M5-M6-M10 forms one ST inverter while M1-M3-M4-M8 forms another ST inverter. Feedback transistors M8/M10 raise the switching threshold of the inverter during the input transition giving the ST action. Detailed operation of the ST-1 bit cell can be found in [3].

ST-2 Bit cell:

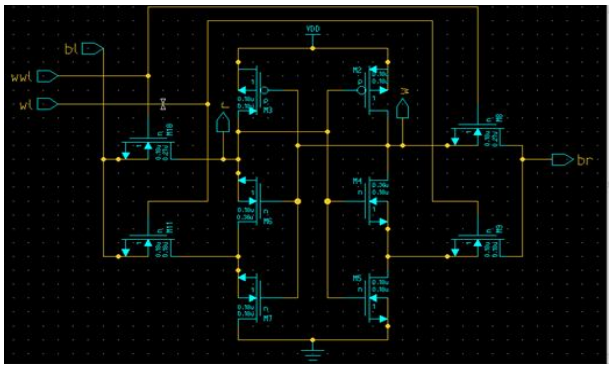

Figure4: Schmitt trigger-2 Bit cell

	WL	WWL
WRITE	1	0
READ	1	1
HOLD	0	0

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Fig. 4 shows the schematics of the ST-2 bit cell utilizing differential sensing with ten transistors, two word-lines (WL/WWL), and two bit lines (BL/BR). The WL signal is asserted during read as well as the write operation, while WWL signal is asserted during the write operation. During The hold-mode, both WL and WWL are OFF. In the ST-2 bit cell, feedback is provided by separate control signal (WL) unlike the ST-1 bit cell, where in feedback is provided by the Internal nodes.

During the read operation **r** is storing logic '0'and **w** is storing logic '1'. When WL is turned ON,(WWL is OFF for the duration of read) For the inverter storing '1' the feedback mechanism is provided by the WL access transistor (M8) compared to the 6T cell the results are better by read stability.

During the write operation, assume **r=0** and **w=1**. In write mode both WL and WWL are turned on while BR is pulled to GND and BL is charged to VDD. For the left-side inverter, both access transistors M9 and M10 might current through the pull down transistor M6 .increased current through M6 increases the voltage at the node **r** to be higher than the read mode voltage.

In the ST-1 bit cell, the feedback mechanism is effective as long as the storage node voltages are maintained. Once the storage nodes start transitioning from one state to another state, the feedback mechanism is lost [6]. To improve the feedback mechanism, separate control signal WL is employed for achieving stronger feedback. Exhaustive operation of the ST-2 bit cell is explained in our earlier work [4].

V. MODIFIED DESIGN

Figure. 5 show the schematic of Read error reduction technique with the eight transistor count. As the Schmitt trigger based designs are having high number of transistor to construct the read stability that is 10T SRAM cell. which are very high, when compared to the existing 6T SRAM Design

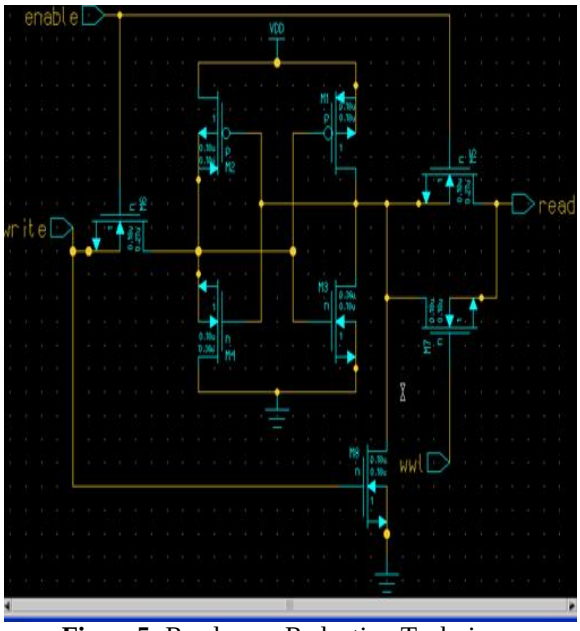

Figure5: Read error Reduction Technique

we are going to combine the mentioned read stability at the above part to our proposed work to reduce the count than the Schmitt trigger based designs at the same time we are going to achieve reduced power consumption with reduced transistor count without affecting the read stability [5].

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VI. PROPOSED DESIGN

NEGATIVE BIAS TEMPERATURE INSTIBILITY

NBTI is a key reliability issue in MOSFETs. it is of immediate concern in p-channel MOS Devices, since they almost always operate with negative gate-to-source voltage; however, the very same mechanism affect also NMOS transistors when biased in the accumulation region. That is with a negative bias applied to the gate terminal

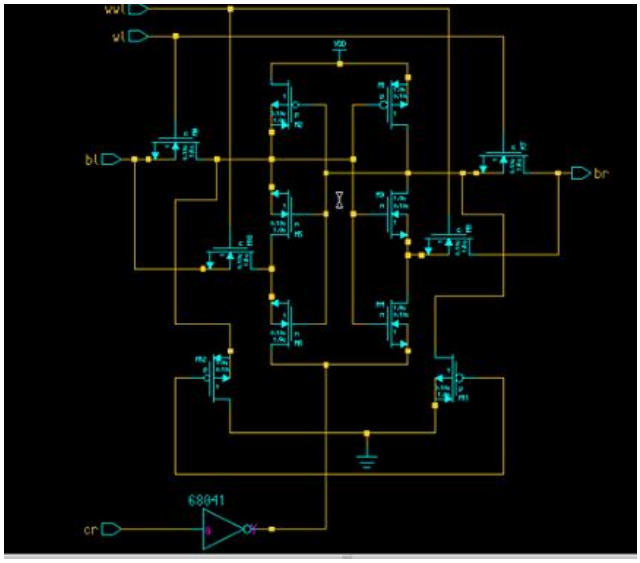

Figure6: Schmitt Trigger based using NBTI Technique

NBTI manifests as an increase in the threshold voltage and consequent decrease in drain current and Trans conductance. The degradation exhibits logarithmic dependence on time. This NBTI makes PMOS threshold voltage to increase. In order to reduce this NBTI problem of SRAM network here we introduce a recovery boosting technique. in this technique SRAM operates in two modes of operation by switching CR line. One was normal mode which acts like normal SRAM network and another was recovery mode which makes PMOS to off and acts like a recovery transistor. here we apply recovery boosting technique to Schmitt trigger SRAM based designs, For reducing leakage power as well as to reducing total power also.

TECHNIQUE	LEAKAGE POWER
ST-2	4.231434e-17A
Read error reduction	- 4.5347FA
NBTI	-18.299FA

Table1: **Leakage power comparisons**

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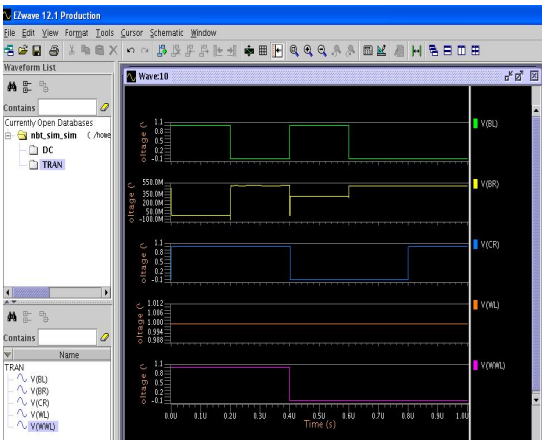
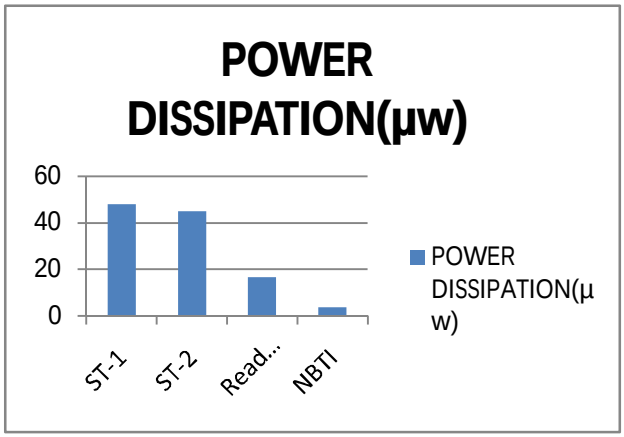


Figure6.1: Output waveforms for NBTI Technique



Graph: Comparisons of Total power dissipation

Table2: Comparisons of Total power dissipation

TYPE	POWER DISSIPATION(µW)
ST-1	**48.2405**
ST-2	**45.0106**
Read error Reduction Technique	**16.8817**
NBTI	**3.8080**

VII. CONCLUSION

In this paper proposed design shows less power than the existing ones 3.8080uwatts at the standard cell, this design combined with 6T, ST CELLS&NBTI circuit with 180nm technology. And it is having much reduced power and leakage power which does not affect any performance of conventional SRAM designs. Hence this design can be used for future SRAM core memories

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