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Mathematical Implementation of MAX LOG MAP Algorithm for Low Power Applications in Turbo Decoders

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ABSTRACT: In Turbo decoding the design of Log MAP algorithm is more complicated with the exponential sum. In this paper a mathematical model is designed with a jacobian logarithm which consists of a max function along with the exponential correction function. The complexity of the jacobian logarithm is also reduced by the Max Log Map algorithm by eliminating the correction term. Multistep Log Map algorithm is used to approximate the correction function. A Dual Mode (SB/DB) procedure is used to compute the log likelihood ratio in order to increase the speed of the computation. The performance of this algorithm is similar to the Log Map algorithm. This method will be incorporated into VLSI technology to design a High Speed MAP Decoder (15% to 25 % as in existing) with less area Utilization (8% as in existing) and low Power (74.95mW)

KEYWORDS: MAP Algorithm, Log MAP Algorithm, Jacobian logarithm, SB/DB and Log Likelihood ratio.

I. INTRODUCTION

The MAP algorithm which is used in the turbo decoders is operated in the logarithmic domain in order to reduce the computational complexity [1]. The computation of log likelihood ratio with the values of state metrics is more complicated with log exponential sum calculation. The log exponential sum can be simplified by Jacobian algorithm by adding a correction term along with the max operator. The correction function calculation is critical because of the performance and complexity of the turbo decoder. So a lot of methods [2][3][4] are used to simplify the computation to satisfy the performance requirements.

This paper proposes an algorithm to compute the correction function that will be used to calculate the state metrics and log likelihood values. Furthermore this Log Likelihood values can be modified into SB/DB mode with a new set of equations and this will increase the performance parameters of the Turbo decoders.

The rest of the paper is organized as follows: in section II, brief introduction and derivation of basic MAP and Log MAP algorithmic equations. Section III reviews different methods of approximation of the correction function. In Section IV, the SB/DB mode calculations are presented. Section V presents the results and discussions. This paper is finally concluded in the Section VI.

II. DIFFERENT METHODS OF MAP ALGORITHM

In this section different method of MAP algorithms were discussed. The mathematical equations required for the Log Map algorithm is introduced with a max operator and the Max Log Map algorithm is also presented.

A. DIGITAL COMMUNICATION SYSTEM MODEL.

A Digital communication system is represented by figure 1.Map algorithm for the block of binary data input sequence D=D1, D2....DN is represented in figure 1. The encoder consists of two identical recursive systematic Convolutional



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encoders (RSC) with M memory elements. The code rate of the encoder is $\frac{1}{2}$ with two outputs which is the sequence of Xs = Xs1, Xs2...XsN. and the parity bit sequence Xp = Xp1, Xp2...XpN.



Figure1. Digital communication system

The corresponding received sequence from the channel with the noise is Y=Ys, Yp which consist of pair of received systematic and parity bits.

B. MAXIMUM A POSTERIORI (MAP) ALGORITHM

The objective of the MAP algorithm is to calculate Log Likelihood Ratio (LLR) (Λ (Dk)) of the a posteriori probability (APP) of Dk = 1 to Dk = 0. The state of the encoder is represented by Sk at time k. The state transition is from k-1 to k. The LLR value can be given by equation 1.

$$\Lambda (D_{k}) = \ln \frac{\sum_{s_{k}} \sum_{s_{k-1}} \gamma_{1}(y_{k}, S_{k-1}, S_{k}) \alpha_{k-1}(S_{k-1}) \beta_{k} S_{k}}{\sum_{s_{k}} \sum_{s_{k-1}} \gamma_{0}(y_{k}, S_{k-1}, S_{k}) \alpha_{k-1}(S_{k-1}) \beta_{k} S_{k}}$$
(1)

The forward state metric αk can be expressed as

1

$$\alpha(S_{k}) = \frac{\sum_{S_{k-1}} \sum_{i=0}^{1} \gamma_{i}(y_{k}, S_{k-1}, S_{k})\alpha_{k-1}(S_{k-1})}{\sum_{S_{k-1}} \sum_{i=0}^{1} \gamma_{i}(y_{k}, S_{k-1}, S_{k})\alpha_{k-1}(S_{k-1})}$$
(2)

and the backward state metric βk can be expressed as

$$\beta(S_{k}) = \frac{\sum_{\substack{s_{k+1} \ i=0}} \sum_{i=0}^{1} \gamma_{i}(y_{k+1}, S_{k}, S_{k+1}) \beta_{k+1}(S_{k+1})}{\sum_{\substack{s_{k} \ s_{k+1}}} \sum_{i=0} \sum_{j=0}^{1} \gamma_{i}(y_{k+1}, S_{k}, S_{k+1}) \alpha_{k}(S_{k})}$$
(3)

The branch transition probabilities γ i can be calculated by the equation (4).

$$\gamma_{i} ((y_{sk}, y_{pk}), S_{k-1}, S_{k}) = e^{\sqrt{x_{sk} (L_{e} + (x_{sk}) + L_{c} (y_{sk}) + L_{c} y_{sk} x_{pk}}}$$
(4)

The channel reliability value $Lc = 2 / \sigma^2$ with σ^2 is the noise variance and Le is the extrinsic information which gives a priori information.

C. LOG MAP ALGORITHM

The complexity in the MAP algorithm can be reduced by Log MAP algorithm. To avoid complicated calculations in the MAP algorithm, the entire MAP algorithm is calculated in Logarithmic domain. So the basic equations in the MAP algorithm (2), (3) and (4) are converted into log domain which reduces the number of multiplications and addition operations used. So, $\hat{\alpha}k(Sk) = \ln \alpha k(Sk)$.



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$$\overset{\Lambda}{\alpha} (S_{k}) = \ln \left(\sum_{S_{k-1}} \sum_{i=0}^{1} e^{\ln(\gamma_{i}(y_{sk}, y_{pk})S_{k-1}, S_{k}) + \ln \alpha_{k-1}(S_{k-1})} \right) - \sum_{S_{k}} \sum_{S_{k-1}} e^{\ln(\gamma_{i}(y_{sk}, y_{pk})S_{k-1}, S_{k}) + \ln \alpha_{k-1}(S_{k-1})}$$
(5)

$$\begin{split} & \bigwedge_{\beta} (S_{k}) = \ln \left(\sum_{S_{k+1}} \sum_{i=0}^{1} e^{\gamma_{i} (y_{S}(k+1), y_{p}(k+1), \cdot S_{k} \cdot S_{k+1})\beta_{k+1}(S_{k+1})} \right) - \\ & \sum_{S_{k}} \sum_{S_{k+1}} \sum_{i=0}^{1} e^{\ln(\gamma_{i} (y_{S}(k+1), y_{p}(k+1), \cdot S_{k} \cdot S_{k+1})\alpha_{k}(S_{k}))} \end{split}$$
(6)
$$\begin{split} & \bigwedge_{\alpha} (S_{k}) = \ln \left(\sum_{S_{k-1}} \sum_{i=0}^{1} e^{\ln(\gamma_{i} (y_{S_{k}} \cdot y_{pk}) \cdot S_{k-1} \cdot S_{k}) + \ln \alpha_{k-1} (S_{k-1})} \right) \\ & - \sum_{S_{k}} \sum_{S_{k-1}} e^{\ln(\gamma_{i} (y_{S_{k}} \cdot y_{pk}) \cdot S_{k-1} \cdot S_{k}) + \ln \alpha_{k-1} (S_{k-1})} \end{split}$$
(7)

The above equation (5), (6) and (7) can be simplified into general form, which is given by the equation (8).

$$F(x_1, x_2, x_3 \dots x_N) = \ln(\sum_{i=1}^n e^{x_i})$$
(8)

The jacobian logarithm for two variable expressions is given by max * $(x_1, x_2) = \ln (e^{x1} + e^{x2}) = \max (x_1, x_2) + \ln (1 + e^{-|x_1 + x_2|})$ $= \max (x_1, x_2) + C(x)$ (9)

The calculation of the correction term C(x) in (9) is more complicated in Log MAP algorithm. The same form of log exponential sum occurs in the calculation of backward state metrics (βk), and LLR A (Dk). So, to improve the performance of the Log Map Algorithm, a simple method of implementation of correction function must be required. The easiest method of finding out the correction function is presented in [5]. But this requires more memory to store the table sequences. A new method used in this calculation is presented in Section III.

D. MAX LOG MAP ALGORITHM

The max log map algorithm introduces an approximation $\max^*(x_1,x_2) \approx \max^*(x_1,x_2)$. This Max log map algorithm simply omitting the correction term C(x).But the performance of the Log Map algorithm is dropped by 10% compared to Log Map algorithm. Even though the Max Log Map algorithm is least complex, it gives worst BER. So, in Max Log Map algorithm, a simple implementation of correction function is required to improve the performance of the turbo decoders.

III DIFFERENT ALGORITHMS FOR THE CALCULATION OF CORRECTION FUNCTION

In this section a different methods of existing algorithms which are approximates the correction function are discussed. The performance tradeoff for adding the correction elements with these algorithms are also discussed.

In the Linear Log Map algorithm proposed in [6], the MacLaurin Series expansion is used and it is observed that the correction function is approximately zero.

$$C(x) \approx \max(0, \ln 2 - \frac{1}{2}x)$$
⁽¹⁰⁾

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This approximation offers a good result than the Constant Log Map Algorithm presented in [7] where

$$C(x) = \begin{cases} \frac{3}{8}, -2 \le x \le 2\\ 0, otherwise \end{cases}$$
(11)

An accurate method of approximation proposed in [8] is Multistep Log Map Algorithm.

$$C(x) \approx \frac{\ln 2}{2^{[x+0.5]}}$$
 (12)

This method of correction is more accurate. This method of algorithm employs with shift registers storing the ln(2).For fast computation, a speed registers are required for this algorithm. Figure 2 shows the graphical comparison of various Approximations to the correction function.

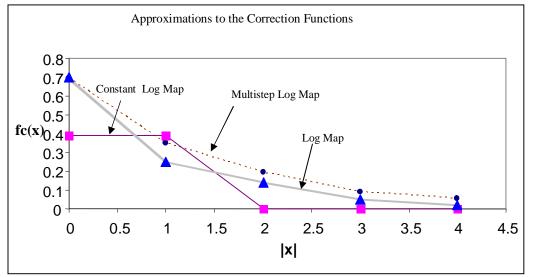


Figure2. Comparison of Various Correction functions

IV. DUAL MODE SINGLE BINARY/DOUBLE BINARY (SB/DB) MAP DECODING

The SB/DB Map decoding is introduced by Y.Sen [9] and C.Y Shen [10] for radix 4 Map architecture to achieve high hardware usage and shared storage information. In general, the MAP is composed of branch metrics, forward recursion state metrics, backward recursion state metrics, a priori LLR, a posteriori LLR, and extrinsic information. For the dual-mode MAP decoding, the radix-4 SB MAP decoding and radix-4 DB MAP decoding are employed because of their computational similarity. So, the equations of branch metrics, forward state metrics, backward state metrics, a priori LLR, a posteriori LLR, and extrinsic information are reformulated for SB / DB Decoding.

A) RADIX-4 SB MAP DECODING

The arithmetic operations of the of the Radix-4 SB MAP are described as

$$\alpha_{k}(S_{k}) = \max_{S_{k-1}, S_{k-2}} (\gamma_{k}(S_{k-2}, S_{k}) + \alpha_{k-2}(S_{k-2}))$$
(13)



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$$\beta_k(S_k) = \max_{S_{k+1}, S_{k+2}} (\gamma_{k+1}(S_k, S_{k+2}) + \beta_{k-2}(S_{k-2}))$$
(14)

$$\gamma_{k}(S_{k-2}, S_{k}) = (\Lambda_{apr,k-1}(u_{k-1}) + y_{s(k-1)})x_{s(k-1)} + \sum_{i=1}^{m} y_{k-1}^{pi} x_{k-1}^{pi} + (\Lambda apr, k(u_{k}) + y_{sk})x_{sk} + \sum_{i=1}^{m} y_{pk} x_{pk}$$
(15)

m - number of parity bit and the sign bit of posteriori LLR value decides whether uk=0 or uk=1.

B) RADIX-4 DB MAP DECODING

In DB mode two binary bits are encoded uk= u1k,u2k. The arithmetic operations of the of the Radix-4 DB MAP are described as

$$\alpha_{k}(S_{k}) = \alpha_{k}(S_{k}) = MAX_{S_{k-1}}(\gamma_{k}(S_{k-1}, S_{k}) + \alpha_{k-1}(S_{k-1}))$$
(16)

$$\beta_k(S_k) = MAX_{S_{k+1}}(\gamma_{k+1}(S_k, S_{k+1}) + \beta_{k+1}(S_{k+1}))$$
(17)

$$\gamma_k(S_{k-1}, S_k) = \Lambda_{apr,k}^{(z)}(u_k = z) + 2y_k^{s_1} x_k^{s_1} + 2y_k^{s_2} x_k^{s_2} + 2\sum_{i=1}^m y_k^{p_i} x_k^{p_i}$$
(18)

The reformulated equations for SB/DB are used for the calculation of Log Likelihood Ratio (LLR) calculations. By writing the MAX operations in the equations of LLR value in SB Mode, We can define $\operatorname{Es}(z^2)$

$$\in_{s} (00) = MAX_{s_{k-2}, s_{k}, u_{k-1=0}, u_{k=0}} (\alpha_{k-2}(S_{k-2}) + \gamma_{k}(S_{k-2}, S_{k}) + \beta_{k}(S_{k}))$$
(19)

$$\in_{s} (01) = \max_{S_{k-2}, s_k, u_{k-1=0}, u_{k=1}} (\alpha_{k-2}(S_{k-2}) + \gamma_k(S_{k-2}, S_k) + \beta_k(S_k))$$
(20)

$$\in_{s} (10) = \max_{S_{k-2}, s_k, u_{k-1=1}, u_{k=0}} (\alpha_{k-2}(S_{k-2}) + \gamma_k(S_{k-2}, S_k) + \beta_k(S_k))$$
(21)

$$\in_{s} (11) = \max_{S_{k-2}, s_{k}, u_{k-1=1}, u_{k=1}} (\alpha_{k-2}(S_{k-2}) + \gamma_{k}(S_{k-2}, S_{k}) + \beta_{k}(S_{k}))$$
(22)

Where z'=(uk-1,uk)

Therefore the LLR value can be defined by

$$\Lambda(D_{k-1}(\mathbf{u}_{k-1})) = \mathbf{MAX}(\in_{s} (10), \in_{s} (11)) - \mathbf{MAX}(\in_{s} (00), \in_{s} (01))$$

$$\Lambda(D_{k-1}(\mathbf{u}_{k-1})) = \mathbf{MAX}(= (01) = (11)) - \mathbf{MAX}(= (00) = (10))$$
(23)

$$\Lambda(D_k(\mathfrak{u}_k)) = \mathrm{MAX}(\epsilon_s(01), \epsilon_s(11)) - \mathrm{MAX}(\epsilon_s(00), \epsilon_s(10))$$

$$\tag{24}$$

By writing the MAX operations in the equations of LLR value in DB Mode, We can define $\mathcal{E}d(z')$

$$\in_{d} (00) = MAX_{S_{k-1}, s_k, u_k = 00} (\alpha_{k-1}(S_{k-1}) + \gamma_k(S_{k-1}, S_k) + \beta_k(S_k))$$
(25)

$$\in_{d} (01) = \underset{S_{k-1}, s_k, u_k=01}{MAX} (\alpha_{k-1}(S_{k-1}) + \gamma_k(S_{k-1}, S_k) + \beta_k(S_k))$$
(26)

$$\in_{d} (10) = \underset{S_{k-1}, S_{k}, u_{k}=10}{MAX} (\alpha_{k-1}(S_{k-1}) + \gamma_{k}(S_{k-1}, S_{k}) + \beta_{k}(S_{k}))$$
(27)

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$$\in_{d} (11) = MAX_{S_{k-1}, s_k, u_{k-1}}(\alpha_{k-1}(S_{k-1}) + \gamma_k(S_{k-1}, S_k) + \beta_k(S_k))$$
(28)

Where z'=(uk) Therefore the LLR value can be defined by

$$\Lambda^{00}(D_k(\mathbf{u}_k)) = 0 \tag{29}$$

$$\Lambda^{01}(D_k(\mathbf{u}_k)) = \epsilon_d \ (01) - \epsilon_d \ (00) \tag{30}$$

$$\Lambda^{10}(D_k(\mathbf{u}_k)) = \epsilon_d \ (10) - \epsilon_d \ (00) \tag{31}$$

$$\Lambda^{11}(D_k(\mathbf{u}_k)) = \epsilon_d \ (11) - \epsilon_d \ (00) \tag{32}$$

By comparing the LLR values of both SB & DB the MAX operations of Cs(z') & Cd(z') are same. Therefore the hardware can be also shared. So, the implementation of this LLR unit in the VLSI tool, the area of utilization is also reduced up to 8 % as existing.

V.RESULTS AND DISCUSSIONS

A mathematical model is designed with a jacobian logarithm which consists of a max function along with the exponential correction function. The complexity of the jacobian logarithm is also reduced by the Max Log Map algorithm by eliminating the correction term. Multistep Log Map algorithm is used to approximate the correction function. By this model of correction function the BER of the turbo decoder is greatly reduced. This is shown in the figure 3. A Dual Mode (SB/DB) procedure is used to compute the log likelihood ratio in order to increase the speed of the computation. This method will be incorporated into VLSI technology to design a High Speed MAP Decoder (15% to 25% as in existing) with less area Utilization (8% as in existing) and low Power (74.95mW).

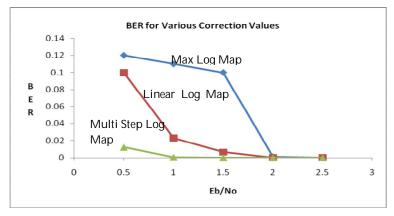


Fig. 7. Comparison of BER for Various Correction functions

The proposed decoder can be designed using Verilog HDL, a descriptive hardware language for architectural module design. This designed architectural module is simulated using Modelsim 5.5e simulating tool, synthesized using Xilinx Project Navigator 10.2i synthesis tool and tested on a Spartan3E family device XC3S500E. This proposed scheme utilized 1972 LUTs and 476 FFs at a maximum frequency of 125MHz. The proposed work results shows that the pipelined metric MAP decoding system incorporated with SB/DB mode leads to lower power consumption in terms of slices, Look Up Tables and Flip Flops.



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Table I

Comparison of power consumptions of Spartan-3 family

FPGA Family	Device Specifications	Power Consumption
Spartan-3E	Xc3s1200E	158.9mw
Spartan-3E	Xc3s500E	81.8mw
Spartan-3E	Xc3s250E	52.27mw

The various devices in the Spartan-3 family are tested against their frequency and power and tabulated in Table 1.

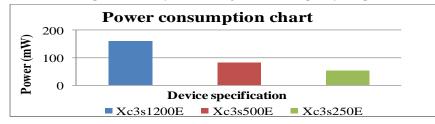


Fig. 8. Comparison of power consumptions of Spartan-3 family

Table 2 illustrates the investigation parameters, such as number of slices, LUTs, etc. required in SB and in DB mode. The values are graphically plotted and depicted in Fig. 9.

Table II

Performance Analysis of hardware utilization

Parameters	SB Mode	DB Mode
Slices	128	98
LUTs	72	64
Gate counts	1800	1785
IOBs	21	21

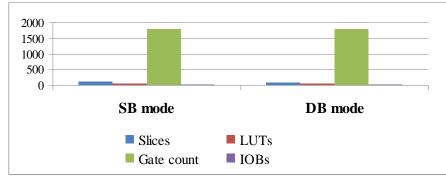


Fig. 9. Graphical representation of Hardware Utilization



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VI. CONCLUSION

The optimum performance of Log Map Algorithm involves complex operations. By neglecting the correction function in the Max Log Map algorithm gives the capacitive loss and hence the correction term must be added which gives the optimal Log Map algorithm. The shared dual mode MAP decoder achieves low computational costs and low storages. This MAP processor achieves high throughput rates and high area efficiency.

REFERENCES

- C. Shannon, "A Mathematical Theory of Information", Bell System Technical J., vol. 27, July 1948, pp. 379-423. [1].
- C. Berrou, A. Glavieux, and P. Thitimajshima, "Near Shannon Limit Error-Correcting Coding and Decoding: Turbo-Codes(1)", Proc. ICC'93, [2]. Geneva, Switzerland, May 1993, pp. 1064-1070.
- C. Schurgers, F. Catthoor, and M. Engels, "Memory optimization of MAP turbo decoder algorithms," IEEE Trans. Very Large Scale Integr. [3]. (VLSI) Syst., vol. 9, no. 2, pp. 305-312, Apr. 2001.
- [4]. M. M. Mansour and N. R. Shanbhag, "VLSI architectures for SISO-APP decoders," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 11, no. 4, pp. 627-650, Aug. 2003.
- S.-J. Lee, N. R. Shanbhag, and A. C. Singer, "Area-efficient highthroughput MAP decoder architectures," IEEE Trans. Very Large Scale Integr. [5]. (VLSI) Syst., vol. 13, no. 8, pp. 921-933, Aug. 2005.
- L.Bahl,J.Cocke,F.Jelinek and J.Raviv,"Optimal decoding of linear codes for minimizing symbol error rate." IEEE Trans.Information Theory, [6]. Vol.20, PP.284-287, Mar 1974.
- W.J.Gross and P.G.Gulak, "Simplified MAP algorithm suitable for implementation of turbo decoders" Electronics Letters, IET Journal, Vol 34, [7]. pp 1577-1578, Aug 1998.
- [8]. S.Talakoub,L.Sabeti,B.Shahrrava and M.Ahamadi,"A Linear log Map algorithm for turbo decoding and turbo equalization" IEEE International conference on Wireless And Mobile Computing, Networking and Communications, Vol 1, pp 182-186 Aug 2005.
- Hao Wang, Hongwen Yang and Dacheng Yang " Improved Log Map decoding algorithm for turbo like codes", IEEE Communication letters, [9]. Vol 10, pp 186-188, Mar 2006.
- P.Robertson, E.Vilebrun and P.Hoecher,"A Comparison of Optimal and sub optimal MAP decoding algorithms operating in log domain", IEEE [10]. International conference on Communications", Vol 2, pp 1009-1013, Jun 1995.
- Y. Sun, Y. Zhu, M. Goel, and J. R. Cavallaro, "Configurable and scalable high throughput turbo decoder architecture for multiple 4G wireless [11]. standards," in Proc. IEEE Int. Conf. Appl.-Specific Syst., Arch. Processors (ASAP), 2008, pp. 209-214.
- C.-Y. Chen, C.-H. Lin, and A.-Y. Wu, "High-throughput dual-mode single/double binary MAP processor design for wireless WAN," in Proc. [12]. IEEE Workshop Signal Process. Syst. (SiPS), 2008, pp. 83-87.
- [13]. J. Kaza and C. Chakrabarti, "Design and implementation of low-energy turbo decoders," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., Vol. 12, no. 9, pp. 968-977, Sep. 2004.
- C.-M. Wu, M.-D. Shieh, C.-H. Wu, Y.-T. Hwang, and J.-H. Chen, "VLSI architectural design tradeoffs for sliding-window Log-MAP decoders," [14]. IEEE Trans. Very Large Scale Integr. (VLSI) Syst., Vol. 13, no. 4, pp. 439–447, Apr. 2005. Li F.-M, C.-H. Lin, and A.-Y. Wu, "Unified convolutional/turbo decoder design using tile-based timing analysis of VA/MAP kernel," IEEE
- [15]. Trans. Very Large Scale Integr. (VLSI) Syst., Vol. 16, no. 10, pp. 1358-1371, Oct. 2008.
- [16]. T.-H. T. C.-H. Lin and A.-Y. Wu, "A memory-reduced Log-MAP kernel for turbo decoder," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), 2005, pp. 1032-1035.
- [17]. XiLinx IP Center, San Jose, CA, "Xilinx LogiCORE, IEEE 802.16e CTC Decoder Core," 2006.
- C.-H. Lin, C.-Y. Chen, A.-Y. Wu, and T.-H. Tsai, "Low-power memory-reduced traceback MAP decoding for double-binary Convolutional [18]. turbo decoder," IEEE Trans. Circuits Syst. I, Reg. Papers, Vol. 56, No. 5, pp. 1005-1016, May 2009.
- [19]. C.-H. Tang, C.-C. Wong, C.-L. Chen, C.-C. Lin, and H.-C. Chang, "A 952MS/s max-log MAP decoder chip using radix-4 4 ACS architecture," in Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC), 2006, pp. 79-82.