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Modified 8T Design of Charge Sharing Technique for Dynamic Power Reduction

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ABSTRACT: The main aim of this paper is to present a novel design of charge sharing SRAM which is obtained from SRAM design of inbuilt charge sharing SRAM (10T).As in the existing design we also use the read discharge power is reused. The read as well as write bit line swings are reduced by recycling the read current. The proposed SRAM design reduces the transistor count, which in turn reduces the power consumed when compared to existing designs. The proposed SRAM also reduces the area. The results show the performance of the design.

I. INTRODUCTION

The IRTS roadmap predicts that the 90% of SoC is covered with memory by the year 2K13. Because of the high speed, low power consumption, robustness and ability of integrating with digital logic blocks.so the bigger the size of SRAM larger is the power consumed. We many reasons for using SRAM in system design. Speed, cost, density and features are the main design tradeoffs for selecting SRAM for your design. When speed is considered SRAM has an edge over DRAM.

Due to this many attempts were being made to decrease the power consumption in SRAM which will increase the battery lifetime of the devices which were operated using battery such as PDA's, wireless, cellular phone and low power biomedical devices. For this scaling of supply voltage is an effective method. But due to this the gate delay is increased which reduces the frequency of operations.

This concept charge sharing is used in architectural level, but we are implementing at the cell level of design on the single ended SRAM's.

II EXISTNG WORKS

1. **Conventional 6T SRAM design:** There are many topologies for SRAM in past decades 6T SRAM got its attention for the tolerance capability for noise over another SRAM cell design. The 6T SRAM cell design consists of two access transistors and two cross coupled CMOS inverters. Bit lines are the input/output ports of the cell with high capacitive loading. The operations READ and WRITE are conducted by these bit lines only, we will see how these are carried out.

    - **Read Operation:** Before starting of the read operation, we should charge the bit lines to VDD. When the word line (WL) is enabled, the bit line which connected to the node of the cell containing '0' is discharged through the NMOS transistor.

      By this we can know which node is containing'0' and which is having '1' in it. Using sense amplifiers we can know the node containing 1/0 by sensing the bit lines. The bit line containing '1' means it's connected to the node containing '1' and vice versa.

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- **Write Operation:** For writing 1/0 we should provide the data to the bit line (BL), with respect to the bit line bar ($\overline{BL}$). When the word line (WL) is enabled the data is written into respective node.

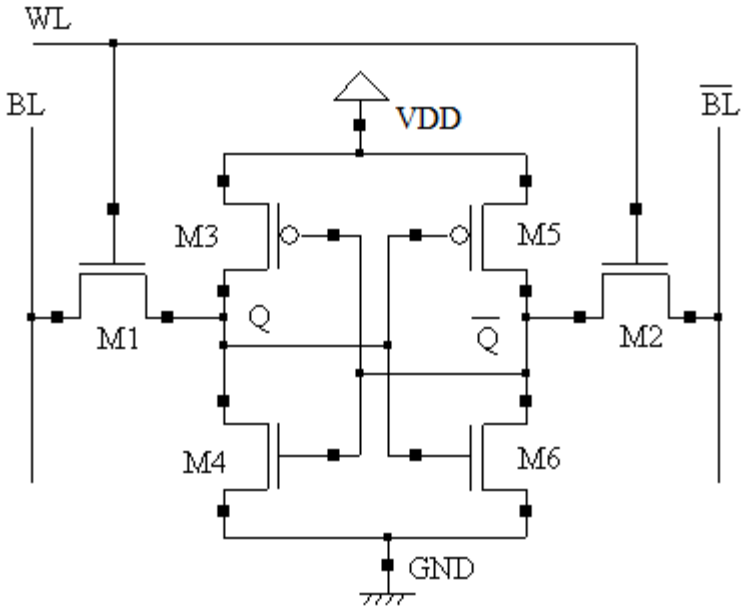

Fig.1 Conventional **6T SRAM**

But the conventional 6T SRAM have stability limitations at low supply voltages. Hence we go for 8T SRAM design. It has the advantage of low power at read '1'operation. As it does not consume power at read '1' cycle.

2. **Single-ended 8T SRAM cell:**In the 8T RSAM, we have the normal 6T SRAM with the read decoupled path consisting of two NMOS transistors. Let us see how read and write operation are carried out.

- **Read operation:** First we should pre-charge the bit lines to full swing after the pre-charge phase is completed we should assert the read word line (RWL) which drives the access transistor M5 ON. The transistor (M6) is ON if the data at node Q is '0', due to which read bit line is grounded through transistors M5 &M6.when the RBL is sensed we have the value in the node '0'. Like this way can do read operation also during which we will have value in RBL as '1' indicating read '1' value due to not having an discharge path .

- **Write operation:** The write operation is same as in the 6T SRAM except the write replaces the pre-charge circuit.

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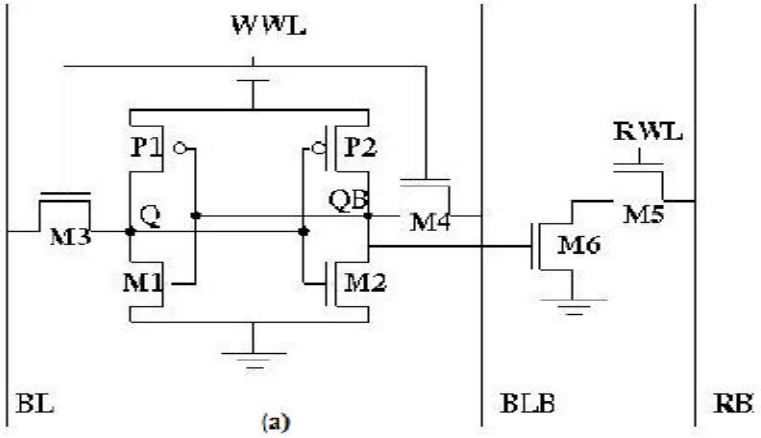

Fig.2 8T SRAM

3. **10T SRAM (charge sharing):** In 10T SRAM is similar to the 8T SRAM with extra transistors are connected to the read decoupled path with bit lines (BL &$\overline{BL}$) to avoid the draining of read current to ground.

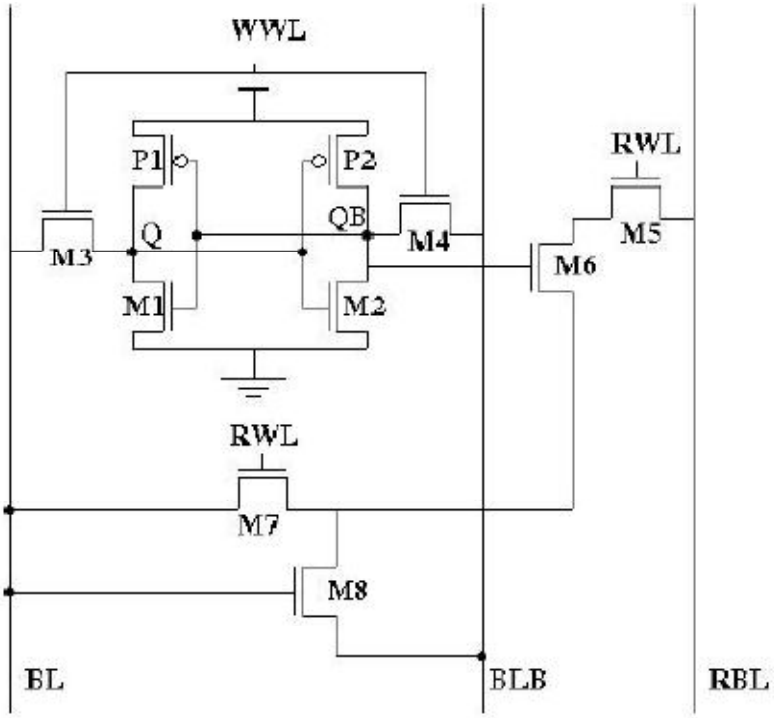

Fig.3 10T SRAM (charge sharing)

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- **Read operation:** Here for read operations are carried depending on the last written data.The last written data is '0' then BLB is high and BL is low, the value read was '0' then the read bit line (RBL) discharges M5,M6 and M7 to BL .
- **Write operation:** If In next cycle we want to write '1'then BL is to be driven from mid-level voltage to full swing as BL is already at mid-level voltage. Likewise we can use the read discharge power for the reduction of write power.

  If in next cycle we want towrite'0' then BL is grounded. As bit lines are at some mid-level voltages they are to be grounded.

III PROPOSED SRAM DESIGN

Here the proposed SRAM design is using the concept of charge sharing from the above 10T SRAM design. But the difference is that the design is done with less number of transistors when compared to the above 10T SRAM which also decreases the area of the design And in the proposed design we also reduced the power consumption when compared with the previous designs.

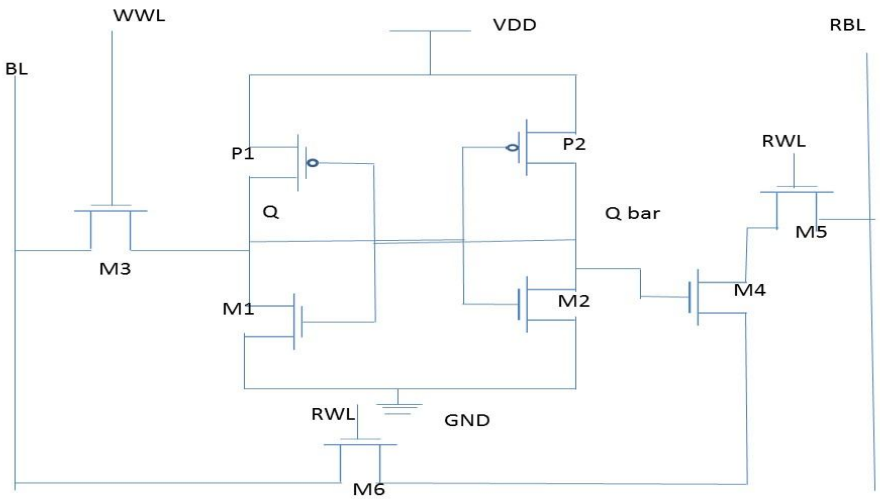

Fig.4 PROPOSED SRAM DESIGN

The proposed SRAM consists of a single ended 7T bit cell which has one bit line (BL) for write operation and one Read Bit cell for read operation.

During the write operation WWL was enabled and RWL was disabled (i.e RWL='0') so M4 M5 M6 are in the off state. The cell acts like single ended 5T SRAM Cell and writes the Bit line data into the cross coupled inverter pair P1 M3 and P2 M2.

During the read operation the bit line disconnected from inverter pair because of WWL='0' during read phase and RWL was enabled so M6 M5 will be in the ON state. For read operation here we are using separate bit line called RBL instead of using same BL. SO during read operation RBL was pre-recharged.

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Read '0': In reading '0' M4 was ON state, so RBL has a discharging path from M4 M5 and M6, the M6 will acts like a charge sharing network, instead of discharging the charge to the ground M6 will charge the bit line (BL) so there will no loss of power to the ground.

Read'1': In reading '1' M4 was OFF state so there will be no discharging path for RBL to discharge maintains the charge and reads the '1'

IV.SIMULATON AND RESULTS

These SRAM designs are designed and simulated using S-edit and T-Spice using TSMC018 technology in Tanner Tools 13.0. The Conventional 8T SRAM, 10T SRAM and Proposed SRAM are simulated with different voltages and there power dissipations are compared and shown in below tables.

Table.1 Comparing Powers at V_{DD}=1.2V for different SRAM designs

Circuit	Write-0	Read-0	Write-1
Existing 8T SRAM	$5.970805*10^{-11}$W	$2.321578*10^{-07}$W	$6.163342*10^{-11}$W
10T SRAM	$3.678532*10^{-11}$W	$6.582594*10^{-08}$W	$3.678532*10^{-11}$W
Proposed 8T SRAM	$1.687015*10^{-11}$ W	$2.359737*10^{-09}$W	$1.92257*10^{-11}$W

Table 1 shows the comparisons of read and write power of the three SRAM circuits are shown with supply voltage 1.2v

Table.2 Comparing Powers at VDD=1.0V for different SRAM designs

Circuit	Write 0	Read-0	Write-1
8T SRAM	$5.402509*10^{-11}$W	$2.428957*10^{-09}$W	$5.479827*10^{-11}$W
10T SRAM	$4.979995*10^{-11}$W	$1.988438*10^{-09}$W	$4.749318*10^{-11}$W
Proposed SRAM	$2.240177*10^{-11}$W	$1.788304*10^{-09}$W	$1.388889*10^{-11}$W

Table 1 shows the comparisons of read and write power of the three SRAM circuits are shown with supply voltage 1.0v

Table.3 Comparing Powers at VDD=0.8V for different SRAM designs

Circuit	Write 0	Read-0	Write-1
8T SRAM	$4.235936*10^{-11}$W	$6.343483*10^{-09}$W	$4.325496*10^{-11}$W
10T SRAM	$3.578484*10^{-11}$W	$3.048031*10^{-09}$W	$3.495926*10^{-11}$W
Proposed SRAM	$8.637696*10^{-12}$W	$2.363708*10^{-09}$W	$7.803598*10^{-11}$W

Table 1 shows the comparisons of read and write power of the three SRAM circuits are shown with supply voltage 0.8v

IV. CONCLUSIONS

Here we have seen a novel approach for designing SRAM for dynamic power reduction. We have used the previous designs of SRAM of charge sharing and designed a design with minimum area and power as well. The proposed design will reduce the both write power and read power.

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