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Multimode Power Gating Architecture And Energy Storage Using Charge Pump Circuit

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ABSTRACT*:* Multithreshold cmos mainly used to reduce the leakage power during long periods of inactivity mode.power gating scheme used to support multiple power off modes and reduce the leakage power at the time of short periods of inactivity.Power gating used to reduce the leakage power,four transistor used to make a power gate structure.In future the leakage power will be stored in charge pump circuit.

KEYWORDS*:* multimode power switches,power gating,multiplxer.

I. INTRODUCTION

Multi-threshold CMOS is an emerging technology that provides high performance and low power operation by utilizing both high and low Vt transistors. By using low Vt transistors in the signal path, the supply voltage can be lowered to reduce switching power dissipation. By reducing Vdd, the switching power can be reduced quadratic ally, but as Vt decreases to maintain performance, the sub threshold leakage current will increase exponentially. For ambitious scaling, the increased leakage power can actually dominate the switching power. Recently, many vendor products in the low power embedded space provide power-gating support in the form of "sleep" modes, typically software control. One of multiple processor cores, in such as system, runs at the maximum operating frequency and the other processor cores can be power-gated off when the operating system detects a long idle loop. The aggressive power-saving strategy above, however, has the following potential problems.

First of all, turning off the nMOS sleep transistor of a gating structure during sleep periods results in charging the virtual ground node of the power gating structure being charged up to a steady-state voltage close to VDD. As a consequence, the data in storage elements is completely lost. A data-recovery process then becomes necessary, significantly degrading system performance. Because of the self-inductance of the off-chip bonding wires and the inherent parasitic inductance of the on-chip power rails, these current surges cause voltage fluctuations in the on-chip power distribution network. Ground bounce is a phenomenon that has often been associated with input/output buffers, internal digital circuitry, and clock gating. Due to the large slew rates of the currents flowing through the bond wires and package pins, the ground and supply voltage seen by the output drivers experience bouncing due to the parasitic [1] associated with the package and connections to the chip. Fluctuations on the supply and ground rails are further increased when output drivers switch simultaneously. A number of researchers have studied the power and ground bounce [1] problem. The bounce noise is the switching noise on the power-supply and ground lines which consists of the resistive IR drop due to bond wire and trace resistances, inductive noise due to the chip-package interface inductance including bond wire self-inductance, trace self inductance, trace-to-trace mutual inductance, and capacitive coupling due to the chip-package interface cross-coupling capacitances. While, due to circuit innovations and device scaling, the speed and accuracy of integrated circuits have steadily increased, the performance of packages, especially for low-cost applications, has not significantly improved.

The scaling of process technologies to nano meter regime has resulted in a rapid increase in leakage power dissipation. Hence, it has become extremely important to develop design techniques to reduce static power dissipation during periods of inactivity. The power reduction must be achieved without trading-off performance which makes it harder to reduce leakage during normal operation. On the other hand, there are several techniques for reducing leakage power in sleep or standby mode. Power gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground .This device is turned-off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance.

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Power gating technique uses high Vt sleep transistors which cut off VDD from a circuit block when the block is not switching. The sleep transistor sizing is an important design parameter. This technique, also known as MTCMOS, (or) Multi-Threshold CMOS reduces stand-by or leakage power, and also enables Id testing. An externally switched power supply is a very basic form of power gating to achieve long term leakage power reduction. To shut off the block for small intervals of time, [1]internal power gating is more suitable. CMOS Switches that provide power to the circuitry are controlled by power gating controllers. Outputs of the power gated block discharge slowly. Hence output voltage levels spend more time in threshold voltage level. This can lead to larger short circuit current. Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby (or) sleep mode. Inserting the sleep transistors splits the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off.

II MULTIMODE POWER GATING ARCHITECTURE

Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. In addition to reducing stand-by or leakage power, power gating has the benefit of enabling Iddq testing

Power gating affects design architecture more than clock gating.It increases time delays, as power gated modes have to be safely entered and exited. Architectural trade-offs exist between designing for the amount of leakage power saving in low power modes and the energy dissipation to enter and exit the low power modes. Shutting down the blocks can be accomplished either by software or hardware. Driver software can schedule the power down operations. Hardware timers can be utilized. A dedicated power management controller is another option.

An externally switched power supply is a very basic form of power gating to achieve long term leakage power reduction. To shut off the block for small intervals of time, internal power gating is more suitable.mos switches that provide power to the circuitry are controlled by power gating controllers. Outputs of the power gated block discharge slowly. Hence output voltage levels spend more time in threshold voltage level. This can lead to larger short circuit current.

Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby or sleep mode. NMOS footer switches can also be used as sleep transistors. Inserting the sleep transistors splits the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off. Typically, high-Vt sleep transistors are used for power gating, in a technique also known as multi-threshold CMOS (MTCMOS). The sleep transistor sizing is an important design parameter.

The quality of this complex power network is critical to the success of a power-gating design. Two of the most critical parameters are the IR-drop and the penalties in silicon area and routing resources. Power gating can be implemented using cell- or cluster-based (or fine grain) approaches or a distributed coarse-grained approach

A.POWER GATING PARAMETERS

Power gating implementation has additional considerations for timing closure implementation. The following parameters need to be considered and their values carefully chosen for a successful implementation of this methodology. Power gate size: The power gate size must be selected to handle the amount of switching current at any given time. The gate must be bigger such that there is no measurable voltage drop due to the gate. As a rule of thumb, the gate size is selected to be around 3 times the switching capacitance. Designers can also choose between header (P-MOS) and footer (N-MOS) gate. Usually footer gates tend to be smaller in area for the same switching current. Dynamic power analysis tools can accurately measure the switching current and also predict the size for the power gate.

1)Gate control slew rate: In power gating, this is an important parameter that determines the power gating efficiency. When the slew rate Sis large, it takes more time to switch off and switch-on the circuit and hence can affect the power gating efficiency. Slew rate is controlled through buffering the gate control signal.

2)Simultaneous switching capacitance: This important constraint refers to the amount of circuit that can be switched simultaneously without affecting the power network integrity. If a large amount of the circuit is switched

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simultaneously, the resulting "rush current" can compromise the power network integrity. The circuit needs to be switched in stages in order to prevent this.

3)Power gate leakage: Since power gates are made of active transistors, leakage reduction is an important consideration to maximize power savings.

III MULTIMODE POWER SWITCHES

An effective and robust multimode power-gating architecture that has none of the above drawbacks. The existing structure requires minimal design effort since it is very simple, and with no analog components. It is considerably smaller than the architecture existing and offers greater power savings for similar wake-up times. The proposed architecture is also more tolerant to process variations; thus its operation is more predictable. A reconfigurable version of the proposed architecture is also proposed, which can tolerate even greater process variations, enabling thus the utilization of the proposed architecture for newer technologies.

The aggregate size of the power switches is not very large due to area constraints, while at the same time power switches are made of low-performing high-Vt transistors in order to minimize the leakage current. As a result, the wakeup time is usually long relative to the circuit clock rate. This limits the applicability of this technique to idle periods that are longer than the wake-up time of the circuit. Consequently, the full leakage-savings potential of this architecture is not fully exploited.

This limits the applicability of this technique to idle periods that are longer than the wake-up time of the circuit. Consequently, the full leakage-savings potential of this architecture is not fully exploited. To overcome this limitation existing the use of an intermediate power-off mode, where the virtual ground node is left charged to an intermediate voltage level. This is achieved through the use of a pMOSs device connected in parallel with the nMOS footer MP. The pMOS is turned on in the intermediate power-off mode, and the virtual ground potential is adjusted to the threshold voltage of the pMOS. Then the virtual ground node requires less time to discharge at the expense of less leakage reduction compared to the complete power-off mode.

It consists of the main power switch transistor MP and two small transistors M0 and M1, each corresponding to an intermediate power-off mode -M0 corresponds to the dream mode and M1 corresponds to the sleep mode. Transistor MP is a high-Vt transistor and it remains on only during the active mode. Transistors M0 and M1 are small low-Vt transistors that are turned on only during the corresponding power-off mode. M0 is turned on during the dream mode and M1 is turned on during the sleep mode.

A . MODULES

Four power-off modes are present. It consists of four footer transistors MP, M0, M1 and M2 that are connected between the core and the ground rail. The main power switch MP is a large high-Vt transistor, and it is implemented using several smaller transistors connected in parallel. Transistors M0, M1 and M2 are very small low-Vt transistors.

1.Active Mode
2.Snore Mode
3.Dream Mode
4.Sleep Mode
5.Nap Mode

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1) SNORE MODE

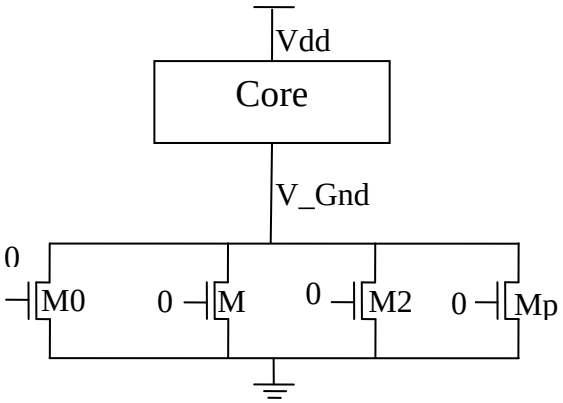

Fig 1 Snore mode

A)The virtual ground rail (V_GND) charges to a voltage level VSnore close to the power-supply.
B)The leakage currents of the transistors of the circuit are suppressed. In this mode the leakage current of the core, ILcore, is equal to the aggregate leakage current flowing through transistors M0, M1, M2, MP (ILcore = ILM0 + ILM1 + ILM2 + ILMP), which is very small.
C)Thus, the voltage level VSnore at virtual ground rail VV_GND approaches Vdd and the circuit consumes a negligible amount of energy.
In order to restore the voltage of the virtual ground rail to its nominal value when the circuit transitions from the power-off mode to the active mode, the parasitic capacitance at the V_GND node has to be completely discharged through the power switch MP which is turned-on again. However, the aggregate size of the transistors comprising the power switch MP is relatively small compared to the size of the core and thus it cannot quickly discharge the V_GND node. Thus the wake-up time can be long relative to circuit clock period, and MP cannot be turned-off during short periods of inactivity.

2) DREAM MODE

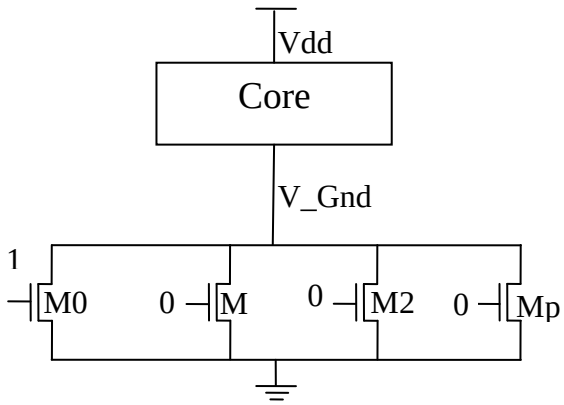

Fig .2 Dream mode

A)The current flowing through transistor M0 increases compared to the snore mode because M0 is on (IM0 > ILM0).
B)The exact value of IM0 depends on the size of transistor M0, and it sets the V_GND node at a voltage level VDream which is lower than that of the snore mode (VDream < VSnore).
C)Thus the static power consumed by the core increases compared to the snore mode, but the wake-up time drops.

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3) SLEEP MODE

A)The sleep mode is implemented by decreasing the voltage level at the virtual ground node.

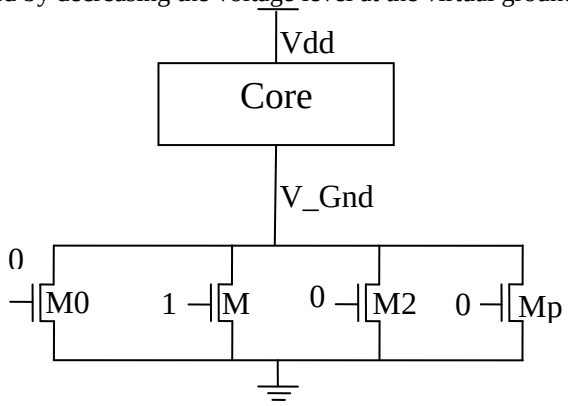

Fig 3 Sleep mode

B)This is achieved by using transistor M1 which has larger aspect ratio than M0 (WM1/LM1 > WM0/LM0).

C)When only M1 is turned-on the aggregate current flowing through M0, M1, and MP increases even more and the voltage level VSleep at the virtual ground node is further reduced compared to the dream mode (VSleep < VDream < VSnore).

D)The wakeup time decreases at the expense of increased static power consumption, which however, remains much lower than the static power of the active mode.

4) NAP MODE

A).The "nap" mode is implemented by further increasing the aspect ratio of the respective power switch (i.e., WM2/LM2 > WM1/LM1 > WM0/LM0).

B)In nap mode the voltage level at V_GND node is set at VNap, where VNap < VSleep < VDream < VSnore.

C)The static power consumption increases and the wake-up time reduce even more.

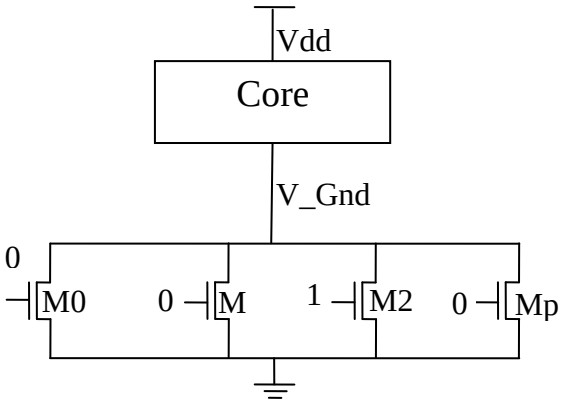

Fig 4 Nap mode

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IV. EVALUATION

The modes are varied with respect to virtual ground,comparison between gating and without gating,the leakage power will be reduced at the use of power gating .without power gating the leakage power is 77mv and it is reduced to 34mv use of power gating architecture.

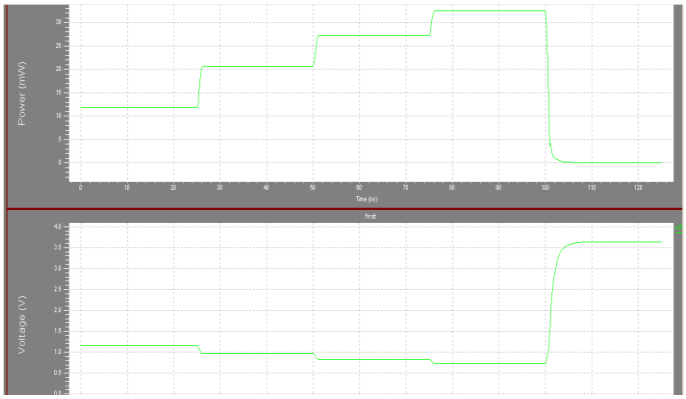

Fig 5 Leakage power output with respect to various voltage

V. CONCLUSION AND FUTURE WORK

A new power-gating scheme that provides multiple power-off modes. The proposed design offered the advantage of simplicity and required minimum design effort. the proposed design is robust to process variations and it is scalable to more than two power off modes. It requires significantly less area and consumes much less power than the previous design. A reconfigurable version of this method can be used to increase the manufacturability and robustness of the proposed design in technologies with larger process variations. The leakage power will be store in charge pump circuit for a reusage.

REFERENCES

[1] S. M. Metev and V. P. Veiko, *Laser Assisted Microtechnology*, 2nd ed., R. M. Osgood, Jr., Ed. Berlin, Germany: Springer-Verlag, 1998.
[2] J. Breckling, Ed., *The Analysis of Directional Time Series: Applications to Wind Speed and Direction*, ser. Lecture Notes in Statistics. Berlin, Germany: Springer, 1989, vol. 61.
[3] S. Zhang, C. Zhu, J. K. O. Sin, and P. K. T. Mok, "A novel ultrathin elevated channel low-temperature poly-Si TFT," *IEEE Electron Device Lett.*, vol. 20, pp. 569–571, Nov. 1999.
[4] M. Wegmuller, J. P. von der Weid, P. Oberson, and N. Gisin, "High resolution fiber distributed measurements with coherent OFDR," in *Proc. ECOC'00*, 2000, paper 11.3.4, p. 109.
[5] R. E. Sorace, V. S. Reinhardt, and S. A. Vaughn, "High-speed digital-to-RF converter," U.S. Patent 5 668 842, Sept. 16, 1997.
[6] (2002) The IEEE website. [Online]. Available: http://www.ieee.org/
[7] M. Shell. (2002) IEEEtran homepage on CTAN. [Online]. Available: http://www.ctan.org/tex-archive/macros/latex/contrib/supported/IEEEtran/
[8] *FLEXChip Signal Processor (MC68175/D)*, Motorola, 1996.
[9] "PDCA12-70 data sheet," Opto Speed SA, Mezzovico, Switzerland.
[10] A. Karnik, "Performance of TCP congestion control with rate feedback: TCP/ABR and rate adaptive TCP/IP," M. Eng. thesis, Indian Institute of Science, Bangalore, India, Jan. 1999.
[11] J. Padhye, V. Firoiu, and D. Towsley, "A stochastic model of TCP Reno congestion avoidance and control," Univ. of Massachusetts, Amherst, MA, CMPSCI Tech. Rep. 99-02, 1999.
[12] *Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specification*, IEEE Std. 802.11, 1997.