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NPC-H Bridge Multilevel Inverter using Third Harmonic Injection

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ABSTRACT: Multilevel inverters (MLI) plays vital role in the field of power electronics and being widely used in many industrial and commercial applications since it possess low electromagnetic interference and the efficiency is considerably high. Neutral point clamped, flying capacitor and cascaded H bridge multilevel inverter are the basic multilevel inverter topologies available. Even though the multilevel inverter plays a vital role, usage of more switches in the conventional configuration poses a limitation to its wide range application. The number of switching devices in the converter system can be reduced by adopting hybrid topology. The topology used here is a three phase seven level hybrid inverter consisting of three level cascaded H- Bridge (CHBMLI) and neutral point clamped multilevel inverter (NPCMLI). Asymmetric dc bus voltage ratio is employed to increase the number of levels of the entire system. The number of levels in line voltage could be increased to 13 levels by third harmonic injection. The main objective of this hybridised structure is to reduce the number of switches with the increase in number of levels. The performance of this hybrid structure with and without third harmonic injection is analyzed in this paper by simulation in MATLAB/SIMULINK. A prototype of single phase topology is also developed.

KEYWORDS: Multilevel Inverter, NPC-HB topology, hybrid, asymmetrical, third harmonic injection

I. INTRODUCTION

Power electronic converters have gained great interest for various industrial applications. Series and parallel connection of switches is adopted as an effective solution to face the limitation of semiconductors current and voltage ratings for high power applications. The output of inverter with stepped waveform has better harmonic spectrum than 2-level waveform in low switching frequencies [1]. Hence, recently multilevel inverters are widely accepted in industry. Different topologies are available which allow us to generate more voltage levels with reduction in number of semiconductors and to increase the output performance and system reliability. In this condition, hybrid topology has attracted a lot of attention both from the customers and from the manufacturers. The topology used in this paper, consists of diode clamped and cascaded H bridge multilevel inverter. Based on this topology, the number of levels could be increased with less number of switches.

II. MULTILEVEL INVERTER

In multilevel inverters, semiconductors and dc voltage sources are arranged so as to generate a staircase output voltage waveform. Multilevel power conversion came into effect 20 years ago which allows converter operating voltage to be increased beyond the limits of classical semiconductors. Multilevel Inverter is an arrangement of power semiconductors and capacitors so as to obtain high-quality load voltage generation. Higher number of semiconductor switches is utilised to perform power conversion in small voltage steps. Multilevel power converters can be considered as voltage synthesizers in which output high voltage is generated from many discrete smaller levels of voltage. The multilevel topologies can be classified into three main categories: the diode clamped, the flying capacitors (FC) and the cascade H-bridge (CHB) converters [2]. With the increase in number of levels with small voltage steps we could obtain the waveforms with high power quality and low electromagnetic interference[3].

III. SIGNIFICANCE OF HYBRID TOPOLOGY

Hybrid topologies are the new multilevel inverter topologies proposed based on the existing topologies so as to achieve some improvements for medium voltage and high power industrial drives. They are widely promoted because

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the harmonic contents of output voltage can be reduced without increasing the number of power devices. The power processing of the entire system is optimised by the use of various DC voltages sources for the hybrid multilevel inverters.

On comparison with a symmetric multilevel inverter, we could obtain different output voltage levels by the addition and subtraction of voltages, with the same number of components. The requirement of output filters can be eliminated [4]. Each power module of this hybrid structure can be operated at a specific DC voltage and switching frequency, so as to achieve the efficiency enhancement and THD compensation characteristics of inverter. For diode clamped and flying capacitor, there is no limitation for the number of levels whereas the cascade H-bridge can possess only odd number of levels; where two levels adds up with the first cell which gives three levels with the addition of each H bridge [5].

IV.NPC-H BRIDGE HYBRID TOPOLOGY

The topology discussed in this paper is a hybrid between the three level NPC and three level H-bridge cells connected in series. The basic circuit diagram for this topology is as shown in fig. 1. Asymmetric (binary) dc bus voltage ratio is used to increase the number of levels [6]. We could optimise the switching losses by this asymmetric ratio. The source voltage which is applied to NPC structure is doubled and is given to the H bridge. HBMLI and DCMLI topologies are hybridized to improve power distribution ratio of cells which results in reduction of semiconductor devices [7].

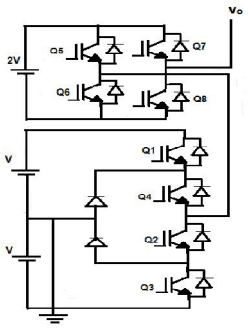

Fig. 1. Circuit Diagram of Hybrid NPC-HB Topology for Single Phase

IV. SWITCHING STATES AND CONTROL SIGNAL

The different switching states of NPC-H bridge topology and the total hybrid converter output voltage that can be generated as different levels is given in table. I. The switching table here indicates the switching sequence for a single phase for the topology shown in fig.1 so as to obtain 3V to -3V. Q1, Q2, Q3 and Q4 are respective switches of NPC structure and Q5, Q6, Q7 and Q8 are that of cascaded H bridge where four of them are compliment of other. The voltage from the NPC structure will be added up with H bridge to achieve higher number of levels. The switching pulses are generated using the Carrier based Sinusoidal Pulse width modulation.

Table I. Switching states of NPC-HB topology

Level	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
-3V	0	1	1	0	0	1	1	0
-2V	0	1	0	1	0	1	1	0
-1V	0	1	1	0	1	0	1	0
0V	0	1	0	1	1	0	1	0
1V	1	0	0	1	1	0	1	0
2V	0	1	0	1	1	0	0	1
3V	1	0	0	1	1	0	0	1

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According to carrier based PWM, to obtain n number of levels, (n-1) number of carriers is required. In this topology, the voltage levels obtained in line to neutral are 7. Hence, six triangular carrier waves are required with the reference sine wave.

Different types of carrier based PWM schemes are available and here Phase Disposition method is adopted. The control pulses generated for the eight switches are according to this control logic. In the Phase disposition (PD) method used here, all carrier waveforms are in phase. The control pulses generated for this topology is as shown in fig. 2.

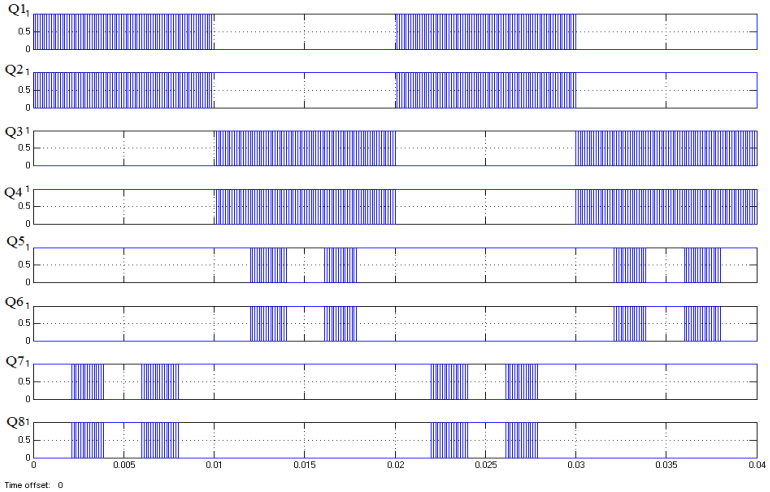

Fig. 2. Control Pulses

The three phase structure based on proposed hybrid topology to which these control pulses are applied is shown in fig. 3.The control pulses for the eight switches in phase A is applied respectively to phase B and C with a phase shift of 120 degree to the corresponding gate terminal.

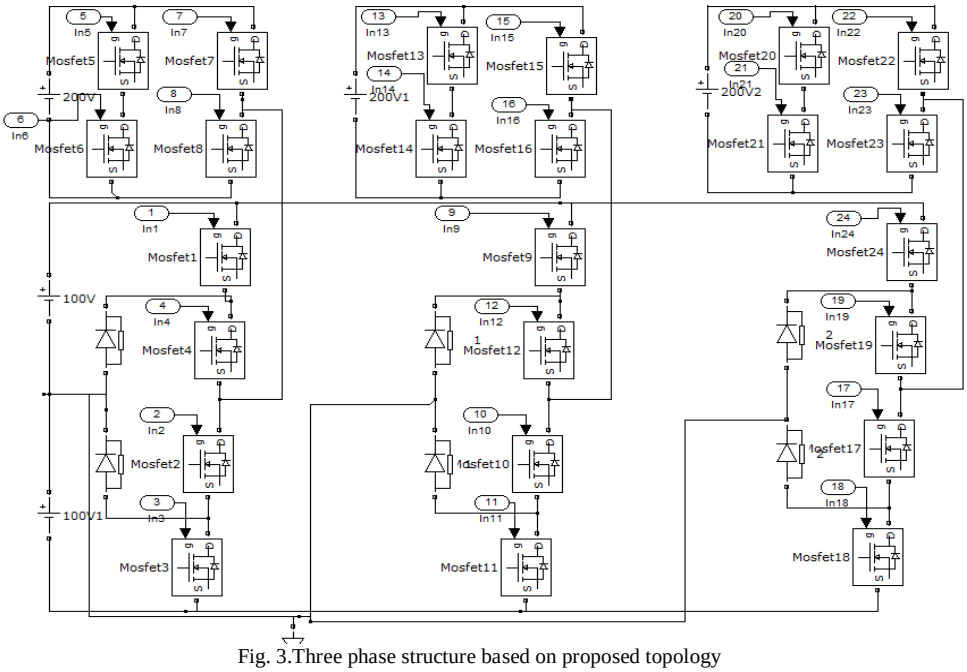

Fig. 3.Three phase structure based on proposed topology

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V. THIRD HARMONIC INJECTION

Third harmonic voltage injection in phase voltage enable increase in the number of levels in line voltage by about 15% . The third harmonic voltage waveform can be generated by modifying the modulating waveform by the addition of one sixth of third harmonics to this waveform. This cause the reduction in the peak value of output waveform by a factor of 0.866 without changing the amplitude of fundamental [8]. This third harmonic generation is shown in Fig.4.

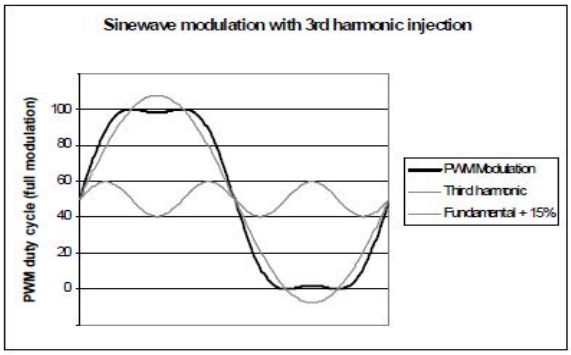

Fig. 4. Effect of third harmonic injection in reference sine wave

The line voltage levels will be $(2^{N+2}-3)$ after third harmonic injection, while it is $\sqrt{3}*(2^{N}-1)*2+1$ without third harmonic injection. Hence, for this inverter the number of voltage levels is 7 in phase to neutral and 11 as number of levels in line to line voltage .By third harmonic injection, this line to line voltage can be increased to 13.

VI. SIMULATION STUDIES

The simulation is carried out using MATLAB/SIMULINK to evaluate the proposed hybrid topology and its control method. 100V and 200V source voltage is given respectively to the Neutral point clamped structure and the Cascaded H bridge respectively. The simulation model to test the operation of seven level inverter in single phase is as shown in fig. 5.

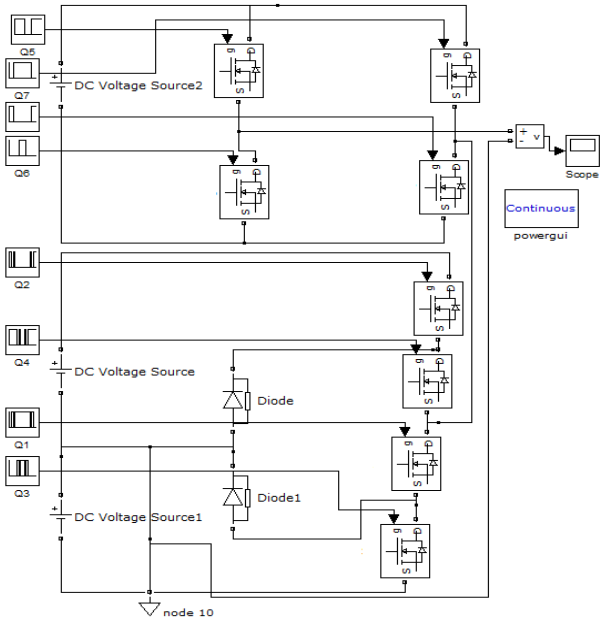

Fig. 5. Simulation Diagram to Test the Operation of 7 Level Inverter in MATLAB/SIMULINK

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The test result of seven level inverter MATLAB/SIMULINK is shown in fig. 6 with voltage levels between -300 V to 300 V.

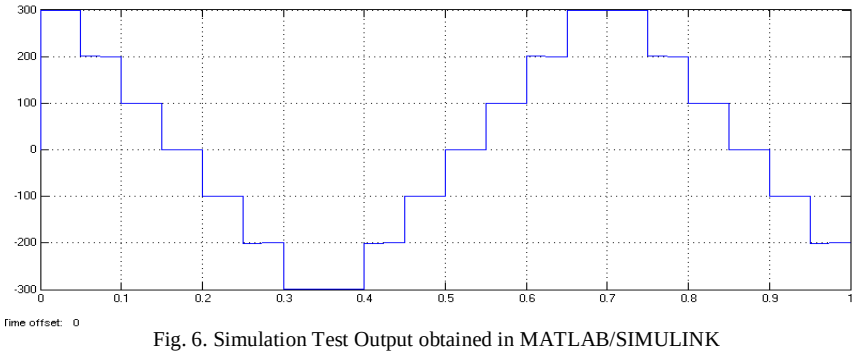

Fig. 6. Simulation Test Output obtained in MATLAB/SIMULINK

The seven level output obtained in three phases after the control pulses are given is as shown in fig. 7.

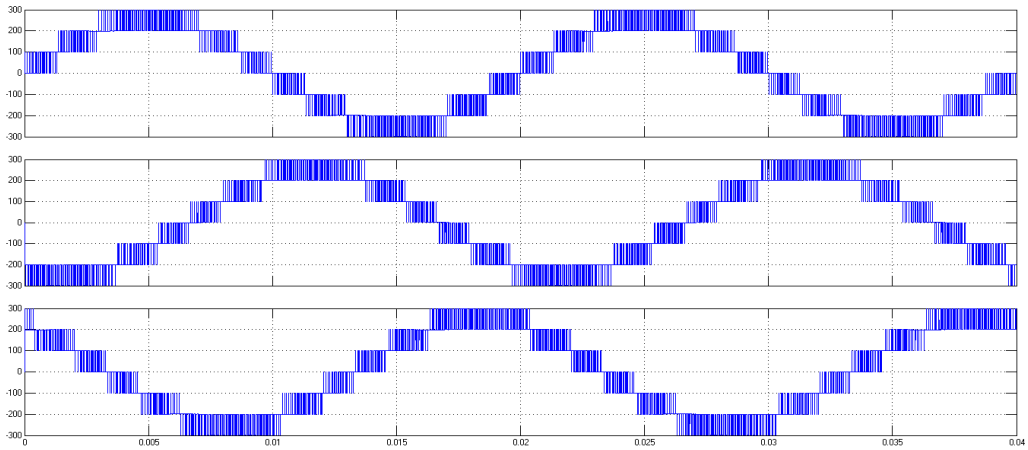

Fig. 7. Seven level output after Control Signals are given in MATLAB/SIMULINK

The line voltage obtained without third harmonic injection for the three phases is as shown in fig. 8. The voltage level of line voltage varies between +500 to -500 V, so that 11 levels of output voltage is obtained.

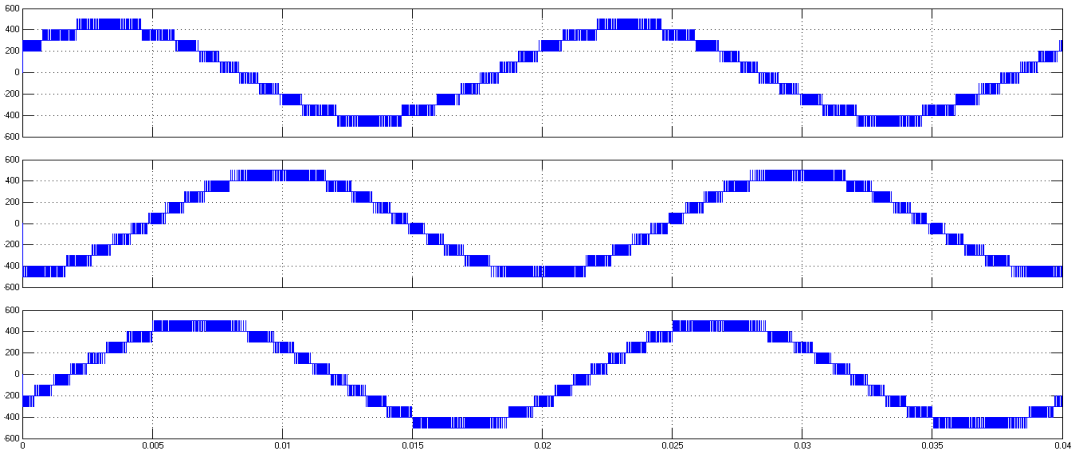

Fig. 8. 11 level line to line voltage without third harmonic injection

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When third harmonic voltage is injected, the number of levels in line voltage can be improved as shown in fig. 9. Here, after the third harmonic injection the line to line voltage is in the range of +600 to -600V, so that the number of levels is increased to 13.

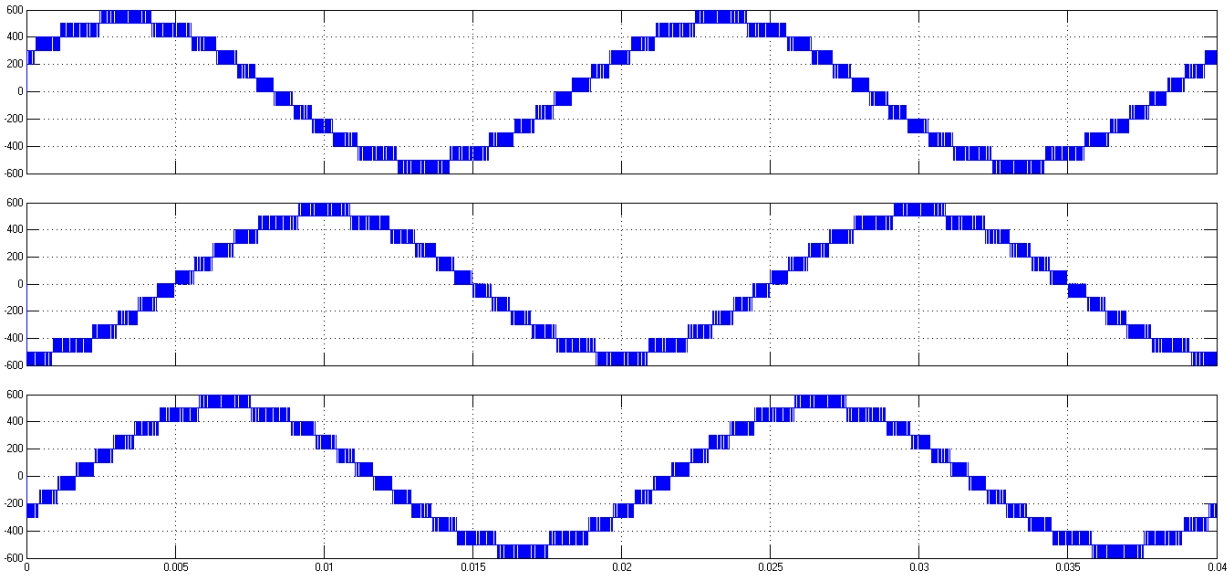

Fig. 9. 13 level line to line voltage with third harmonic injection

VII. FFT ANALYSIS

The spectral analysis of the MATLAB/SIMULINK model of NPC-H bridge hybrid topology is performed. The FFT analysis for the output signal is performed at a fundamental frequency of 50 Hz and the THD analysis for line to line voltage without third harmonic injection is shown in fig. 10.

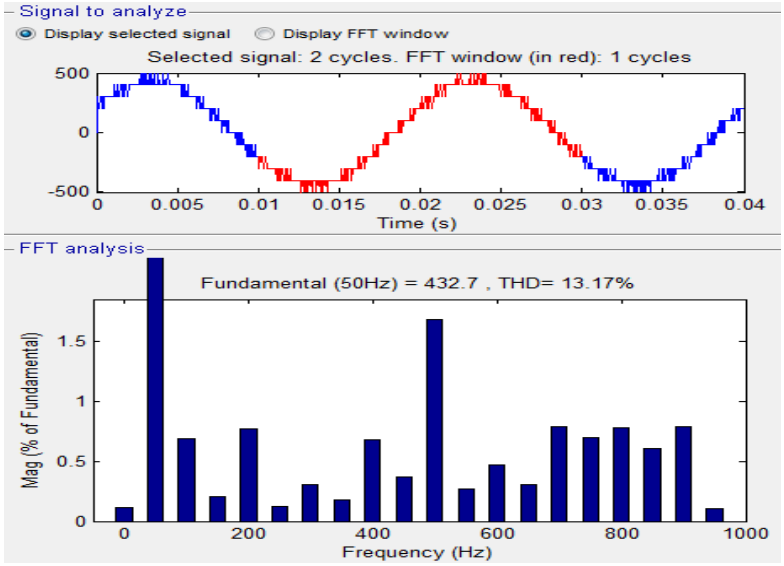

Fig. 10. THD Analysis of line to line voltage without third harmonics injection

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Similarly, the THD analysis result obtained for line voltage after the injection of third harmonic voltage is as shown in fig. 11 and the reduction in total harmonic distortion is observed. Also the higher order harmonics are suppressed using this method.

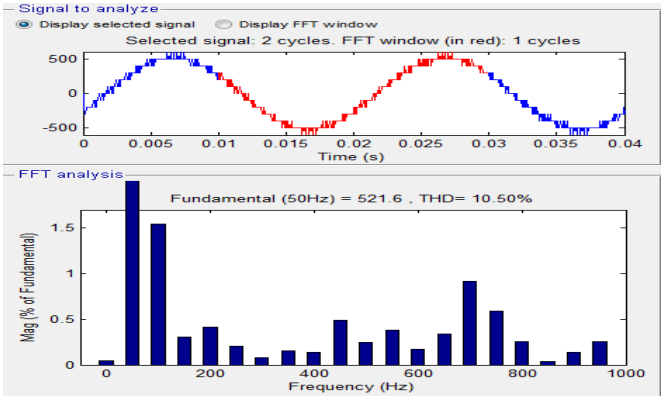

Fig. 11. THD Analysis of line to line voltage without third harmonics injection

IX. HARDWARE SETUP

The hardware structure set up is shown in fig. 12 below. Since asymmetric binary ratio is adopted, the source voltage supplied was 5 V and 10 V respectively for the NPC and cascaded H bridge topology. The hardware is setup using the DAQ interfacing system for the control pulses. MOSFET switches IRF540 and optocoupler MCT2E is used for isolation.

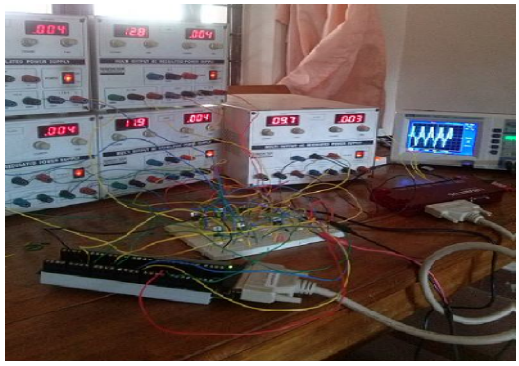

Fig 12: Hardware Set up

The output was observed in DSO as seven levels obtained between -15 V to 15V after control pulses are given to the gate terminal of MOSFET and is shown in fig. 13.

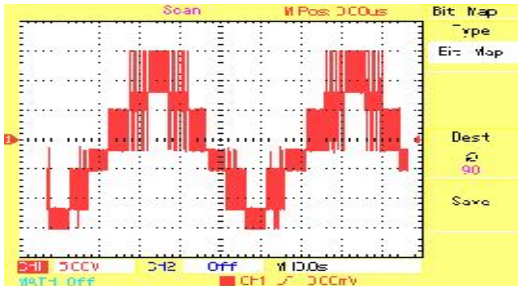

Fig. 13: Seven Level Output Obtained

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X. CONCLUSION

Asymmetric hybrid multilevel inverter is developed. It combines the advantages of three level Neutral point clamped inverter and H bridge. Seven level output is obtained based on the simulation carried out on this hybrid topology in each phase. The Total Harmonic Distortion for the phase voltage is obtained as about 23%. Through this topology, we could reduce the number of switches and hence the switching losses for increased number of levels. Total Harmonic Distortion could be reduced with increase in number of levels. The number of levels could be improved by 15% using third harmonic injection, so that THD in line voltage is reduced to 10.5% from 13.2%. All the other dominating harmonic components in line to line voltage could be reduced by the third harmonic injection. Also the number of levels are increased from 11 to 13 in three phase line voltage. The hardware for the single phase of this topology is set up using MOSFET switches and the control pulses are given through DAQ and the seven level output is obtained.

REFERENCES

[1] Pharne I.D. and Bhosale Y.N., "A Review on Multilevel Inverter Topology," *IEEE Conference on Power,Control and Embedded Systems*, pp.700 703,Feb 2013
[2] Jos Rodrguez, Jih-Sheng Lai, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications", *IEEE Transactions on Industrial Electronics*, 49(4), pp.2703-2712, August 2002.
[3] Muhammad H. Rashid., Power Electronics: Circuits, Devices and Applications, Pearson Education, India, July 2004
[4] P Satheesh Kumar, B Sirisha, "Hybrid topologies of multilevel converter for current waveform improvement", *International journal of inventive engineering and sciences(IJIES)* , 1(4), pp.2319-9598, March 2013.
[5] June seok, Kyo beum, "New modulation techniques for leakage current reduction and a neutral point voltage balance in transformerless pv systems using a three level inverter", *IEEE Transaction Power Electron*. 29(4), April 2014
[6] Juan Dixon, Javier Pereda., "Asymmetrical Multilevel Inverter for Traction Drives Using Only One DC Supply", *IEEE Transactions On Vehicular Technology*, 59(8), pp. 3736-3743, October 2010
[7] S.K.Chattopadhyay, B.C.Pal, " A Hybrid Multilevel Inverter Topology with Third Harmonic Injection for Grid Connected Photovoltaic Central Inverters", *International Symposium on Industrial Electronics*, pp.1736- 1741,May 2012

BIOGRAPHY

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Anish Benny received B. Tech in Electronics &Communication Engineering from College of Engineering, Perumon, and Kerala in 2006. He received the M. Tech degree in Industrial Instrumentation & Control from TKM College of Engineering, Kollam in 2011. He has industrial and teaching experience and has guided UG and PG students for their final projects. He has published papers in various national and international conferences. Currently he is working as Assistant Professor in Electrical and Electronics department, Amal Jyothi College of Engineering. His areas of interest include systems control, instrumentation, sensor systems, modeling and simulation, biomedical instrumentation and mixed circuit design.