Performance Analysis of Various Level Shifters using LECC

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ABSTRACT: A level shifter circuit capable of handling extremely low voltage input. The circuit has a distinctive current generation scheme using a logic error correction circuit that work by detecting the input and output level and it dissipate operating current only when the input signal changes. This proposed circuit shows better performance in term of power consumption. Output level of 3V has been obtained with input pulse of 0.4V, 1kHz.Here we discuss the comparison of the two various level shifter using Logical error correction circuit.

Keywords:LECC (logical error correction circuit), LLECC (Low logic error correction circuit), HLECC (High logic error correction circuit)

I.   INTRODUCTION

With the growing demand of handheld devices like cellular phones, multimedia devices, personal note books etc., low power consumption has become major design consideration for VLSI circuits and system. With increase in power consumption, reliability problem also rises and cost of packaging goes high. Power consumption in VLSI circuit consists of dynamic and static power consumption. [5] Dynamic power has two components i.e. switching power due to the charging and discharging of the load capacitance and the short circuit power due to the non-zero rise and fall time of the input waveforms. The static power of CMOS circuits is determined by the leakage current through each transistor. Power consumption of VLSI circuits can be reduced by scaling supply voltage and capacitance. With the reduction in supply voltage, problems of small voltage swing, insufficient noise margin and leakage currents originate. With the development of technology towards submicron region leakage power has become significant component of total power dissipation. Static power component of power consumption must be given due consideration if current trends of scaling of size and supply voltage need to be sustained.[5]

In System on chip (SoC) design, different parts like digital, analog, passive component are fabricated on a single chip and needs different voltages to achieve optimum performance.[2] Level converters are used to convert the logic signal from one voltage level to other level and are the significant circuit component in VLSI systems. Level shifters are also important circuit component in multi voltage systems and have been used in between core circuits and I/O circuit.

One approach has been to increase the drive current of the level shifter by enlarging the transistor channel width. Another is to use a multi-stage level shifters [5] or inverters with multiple supply voltages. However, these circuits still depend on the supply voltage difference, the circuit configuration is complex, and it requires multiple references voltage. The problem discussed above is thus basically unresolved.

To solve this problem, we presented the logical error correction circuit (LECC) capable of handling extremely low voltage input. The proposed LS circuit can convert extremely low voltage input signal into high voltage output signal.
In this paper, we will first examine the performance of conventional level shifter circuit without LECC and with LECC at very low voltage into high voltage.

II.   CONVENTIONAL LS CIRCUIT

Fig .1 The cross couple PMOS transistors improve the switching speed and output swing by using the positive feedback. [1] When a '1' is applied to IN, INB becomes '0' and OUT is pulled down which turn on MP2 and OUT goes to V_{DDH}. When IN changes to '0', INB rise to V_{DDL} and turns on MN2 which pulls OUT down to 0. However, if sub-threshold logic signal is used for the input to the level converter, due to the low voltage value of logic '1' at INB, the on

current through MN2 is very weak comparing with the on current of MP2. Node OUT cannot be pulled down and the conventional LC will not functional well.
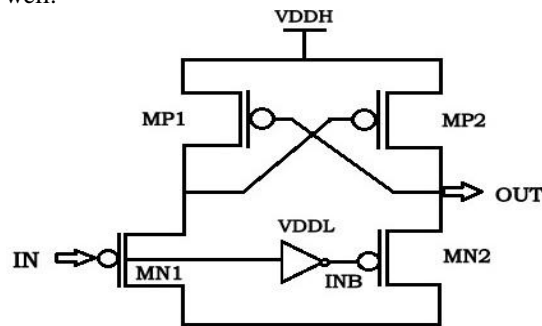

Fig. 1. Conventional LC

III. SUB-THRESHOLD LS CIRCUIT

The sub-threshold level converter we additional PMOS diode (MP3 and MP4) are connected in series with the 2 original cross-coupled PMOS transistors (MP1 and MP2).[3] When the LC is steady state, the $|V_{GS}|$ of the PMOS diode is very small which equals to the diode voltage drop $|V_{PD}|$. At the same, the original pull-up PMOS transistors are either turned on of turn off, depending on the input value. For the cross-couple LC design, the input voltage should be able to activate the LC internal positive feedback in order to make the LC flip its output correctly. [6] When the sub-threshold logic '1' is inputted to the NMOS gate. In power aware systems, supply voltage is varied to match with the weak load of the system. Therefore the circuit performance has to be adaptive with the operating supply voltage. Fig.2.
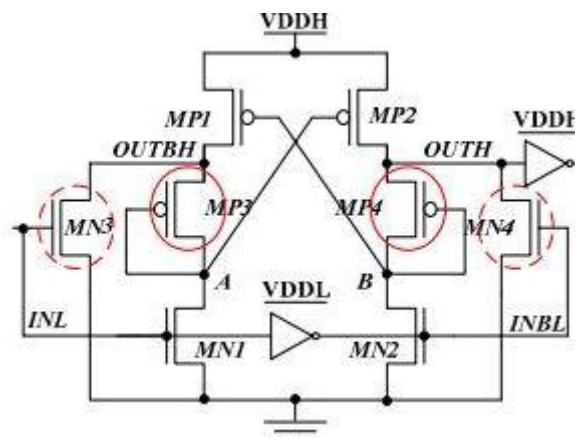

Fig. 2. Sub threshold LC

IV. LECC APPROACH

It consists of a level conversion circuit and a logic error correction circuit (LECC). The complementary input signals (IN and INB) and the output signal (OUT) are applied to the LECC. The LECC supplies the operating current for the level conversion circuit only when the LECC detects a logic error. Fig. 3 shows the complete schematic of the LS circuit. The operation principles of the circuits are described in the following sections.

1) Level Conversion Circuit: The level conversion circuit, which is shown on the right in Fig. 3, is based on a conventional two-stage comparator circuit. The comparator generates output voltage signal, OUT, according to the difference in the voltage of IN and INB. Note that the voltage of OUT is determined by the drive currents of pull-up transistor MP6 and pull-down transistor MN8, and that the currents flowing in MP6 and MN8 depend on current flowing through MP2. Therefore, because both drive currents are determined by the same current, the circuit is free from the limitations discussed in the conventional ones.

In the conventional comparator design, a current reference circuit needs to operate steadily. However, because the current circuit needs to operate steadily. However, because the current reference circuit dissipates static current and increases power dissipation, it cannot be used in our design. Therefore, we developed a logic error correction circuit (LECC) in which the current flowing in the circuit is generated only when the input signal change.

2) Logic Error Correction Circuit (LECC):[4] The LECC, is shown on the left in Fig. 3, consists of two circuit blocks: 1) a low logic error correction circuit (LLECC) and 2) a high logic error correction circuit (HLECC). They are driven by IN, INB, and OUT. The LECC generates an operating current such that IN and OUT correspond to each other. When the output logic level of the LS circuit corresponds to the input logic level, the LECC does not supply current . When they do not correspond, the LECC detects the logic error, and the LLECC or HLECC supplies an operating current. In other words, because the LECC supplies an operating current only when the input and output logic levels do not correspond to each other, the power dissipation of the circuit is minimized. The correction circuit operations are described below.

LLECC: The low logic error correction circuit, LLECC, Consists of two nMOSFETs (MN1 and MN2) connected in series. The LLECC operates only when OUT does not correspond to the "Low" logic of IN. Fig. 4 depicts the waveforms of IN, INB, and OUT. When IN changes from High to Low, or when INB changes from Low to High, there is a period during which OUT does not correspond to IN. During this period, the LLECC generates fall-transition current ___until OUT corresponds to the Low logic of IN

HLECC: The high logic error correction circuit, HLECC, consists of three nMOSFETs (MN3, MN4 and MN5) and a pMOSFETs (MP1). In contrast to the LLECC, the circuit operates only when OUT does not correspond to the "High" logic of IN. Fig. 4 depicts the waveforms of IN and OUT. When IN changes from Low to High, there is a period during which OUT does not correspond to IN. During this period, the HLECC generates rise-transition current until OUT corresponds to the High logic of IN.

. When IN and OUT are High and Low, the output voltage of the first stage are is High because the overdrive voltage of the MP1 is larger than that of MN3. This enables MN4 and MN5 to supply current to the level conversion circuit, and pulls OUT up to V_{DDH}. From the discussion above, current for the level conversion circuit is expressed as

$$I = I_F + I_R$$

Because I_F and I_R are not generated and the LECC does not supply current when the input and output logic levels which correspond,[7]&[8] the power dissipation of the circuit is minimized. The amount of I_F and I_R generated depends on lower supply voltage of VDDL.

When IN and OUT correspond, the LECC does not supply any current to the level conversion circuit. However, in fact, leakage current flows in the circuit.[9] Therefore, because the voltage gain in the level conversion circuit is sufficient to keep the output node, OUT is kept at a voltage, i.e. V_{DDH} or GND
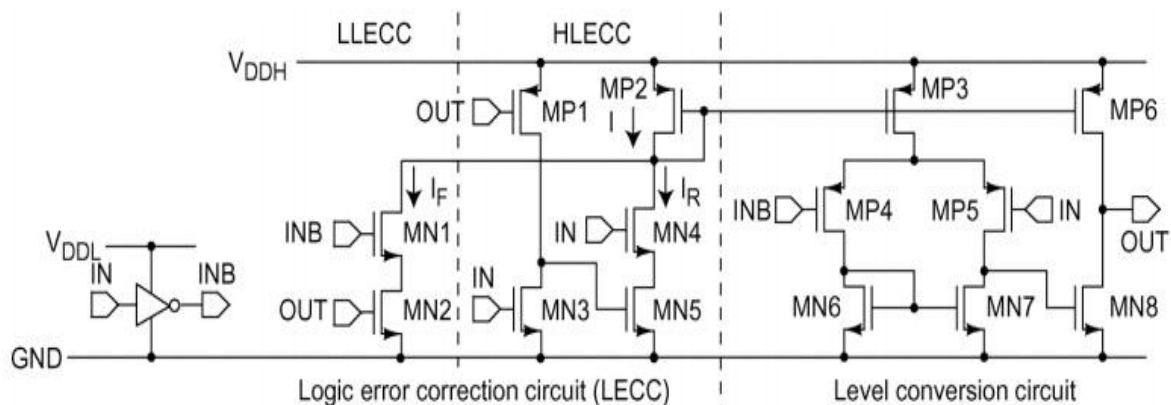

Fig. 2.Schematic of proposed LS circuit.

IV. SIMULATION RESULT

The performance of the proposed LS circuit evaluated using CADENCE with a set of GPDK 180 and GPDK 90 . V_{DDH} was set to 3v[]. We used an inverter as a load circuit of the LS circuit and calculated power dissipation include a charge and discharge current of the load. [11]The amplitude and frequency f_{IN} of the input signal were set to 0.4v and 1Khz input signal was converted into a 3-v output signal fig .4.
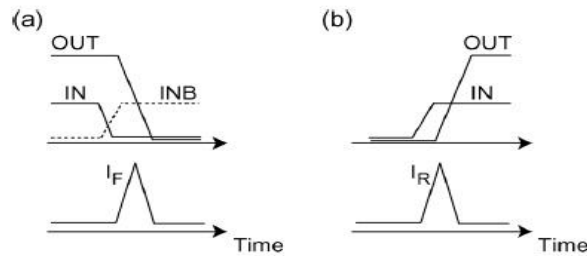
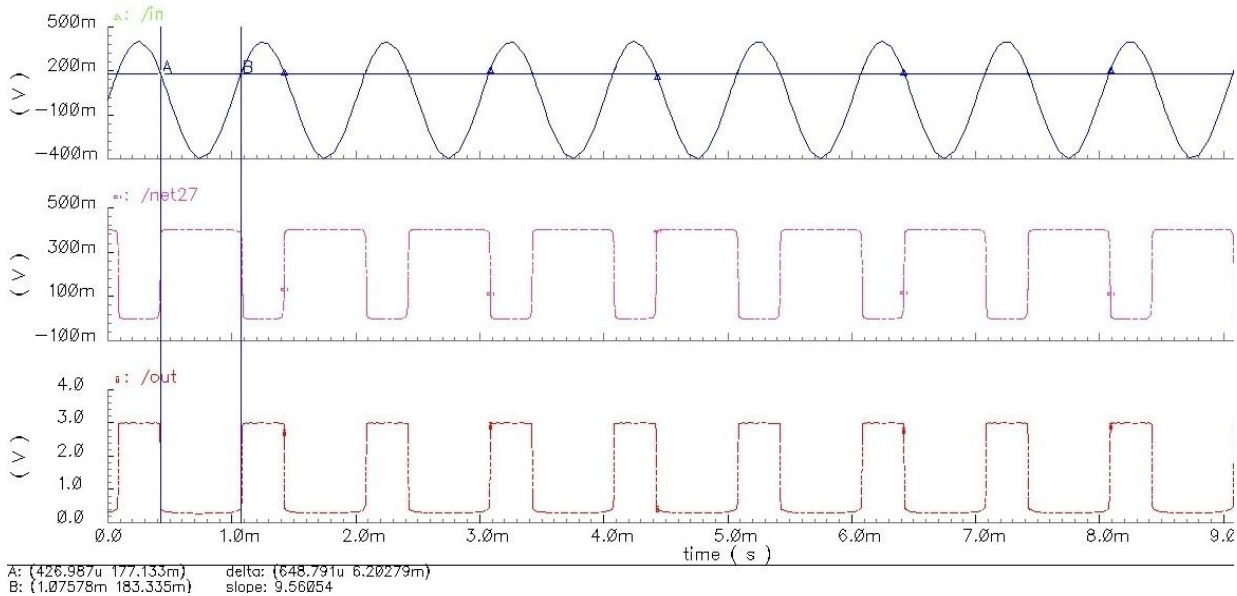Fig. 4.Waveforms (a) when fall-transition current forLS is generated and (b) when rise-transition current for LS

Fig. 5.Measured waveforms of proposed LS for 10-kHz input pulse.

V.CONCLUSION

Here we presented a level shifter circuit for extremely low-voltage. The proposed circuit consists of a conversional level shifter circuit and sub threshold level converter.[10] It can convert low-voltage digital input signals into high-voltage digital output signals and achieve low power operation. I am using CADENCE GPDK 180 AND GPDK 90 CMOS technology file and demonstrated its operation by measurements. The circuit converted a 0.4-V input signal into a 3.-V output signal.

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BIOGRAPHY

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