

(An ISO 3297: 2007 Certified Organization) Vol. 3, Issue 5, May 2014

# Performance Analysis of Various Types of Fault Current Limiters Using PSCAD

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**ABSTRACT-** In this paper the effect of various types of fault current limiters installed in a radial power distribution on the fault current and voltage distortion are analyzed and assessed. The distribution system will be operated under the influence of various types of fault. In this case, the voltage drop (sag) and overvoltage (swell) are severe because of the increased fault current when a fault occurs. The effect of various FCL on the fault current and the voltage distortion are analyzed by its connection in the radial power distribution system. First, resistive type superconducting fault current limiter, solid state fault current limiter and hybrid fault current limiters are designed using PSCAD/EMTDC. Next, a radial power distribution system is designed and the performances of various fault current limiters are analyzed in the basis of fault current limitation and reduction the voltage distortion. The result of SFCL is being analyzed with the result of solid-state and hybrid fault current limiters.

**KEYWORDS:** hybrid fault current limiter, solid-state fault current limiters, superconducting fault current limiters radial power distribution system.

### I. INTRODUCTION

Over the past decades, superconducting technology have been grown in various area. Especially superconducting fault current limiters have been developed. SFCL decreases the fault current and reduces the adverse effect on the power system ultimately this can make the capacity of the circuit breakers small. Moreover, SFCL can provide additional advantage as the improvement of voltage sag [1].Reference [1] presents the assessment method of voltage sag using the Information of Technology Industry Council (ITIC) curve when SFCL is applied to radial power distribution system. Reference [3] and [4] presents the improvement of voltage sag by installing the various fault current limiters. Reference [13] presents the IGCT based solid-state fault current limiters. Reference [14] presents the hybrid fault current limiter based on resonant LC circuit. Voltage sag is evaluated by magnitude and duration. In general the series connected impedance such as SFCL improves the magnitude of sag where as it may worsen the duration of sag because of the delayed trip time of the protective device by the decreased faults current. These effects of various FCL on voltage distortion should be evaluated. In this paper we assess the impact of various types of FCL on voltage distortion occurred by faulty current is explained and fault current magnitude is also analyzed. In section III the voltage distortion occurred by faulty current is explained and fault current magnitude is also analyzed. In section IV we evaluate the voltage distortion magnitude using various FCL even we evaluate the fault current magnitude using various FCL even we evaluate the fault current magnitude using various fault current limiters.

#### **II. LITERATURE REVIEW**

In this paper we design the resistive type superconducting fault current limiter based on [1], [5]-[10]. The impedance of SFCL according to time (t) is given in (1). Where  $R_n$  and  $t_f$  represents the impedance being saturated at normal temperature and time constant respectively. In addition to  $t_1$ ,  $t_2$  represent quench start time, the first recovery time and second recovery time



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$$R(t) = \begin{cases} 0 & (t < t_0) \\ R_n [1 - \exp\left(-\frac{t - t_0}{t_f}\right)]^{\frac{1}{2}} & (t_0 \le t < t_1) \\ a_1 (t - t_1) + b_1 & (t_1 \le t \le t_2) \\ a_2 (t - t_2) + b_2 & (t \ge t_2) \end{cases}$$
(1)

The solid state fault current limiters developed by wanmin [13] consist of diodes, reactor and self turned- off igct switches by optimizing the size of the inductor and with the introduction of switches that can handle high power, this type of FCL can be made relatively compact in size. the author in [13] provides a good overview of the technical detail involved in the model. the hybrid fault current limiter developed by h.arai [14] is based on the resonance characteristics exhibited when an inductor and capacitor are in series with each other. the performance of various types of fault current limiters are being analyzed on the basis of fault current limitation as well as limitation in the voltage distortion during the occurrence of fault. the result of superconducting fault current limiter is being analyzed with solid state as well as hybrid fault current limiters

#### **III. VOLTAGE DISTORTION AND FAULT CURRENT MAGNITUDE**

When fault occurs in a power distribution system the automatic reclosure or circuit breaker with over current relay (OCR) and reclosing relay will open to clear the fault and automatically reclose after a time delay. This reclosure behavior can take place several times in an effort to establish a continuous service when a temporary fault occurs [11].Fig. 1 depicts the IEEE standard 6- bus system in PSCAD



Fig. 1. IEEE standard 6- bus system in PSCAD

This IEEE model is stimulated in the PSCAD with the above mentioned specification as prescribed in the table and various results are being analyzed Fig. 2 depicts the various fault current at various phases during the occurrence of fault. Fig. 2 (a) depicts fault current in phase A, likewise Fig. 2 (b) depicts fault current in phases B and Fig. 2 (c) depicts fault current in phase C



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Fig. 2. Fault current magnitude at various phases. (a) Fault current at phase A. (b) Fault current at phase B. (c) Fault current at phase C.

When a fault occurs, the customer at each feeder experiences different magnitude of voltage according to various factors such as line impedance, fault location and so on. Generally, a voltage magnitude at the bus near to the secondary side of the main transformer during fault can be represented by the equation (2), ignoring the fault impedance and a three phase fault is applied. The source voltage is at 1.0 p.u.

$$V_{DMS} = \frac{z_{Img}}{z_{source} - z_{Mtr} + z_{Img}}$$
(2)

Where  $Z_{source}$ ,  $Z_{Mtr}$  and  $Z_{line}$  are the source, line, transformer impedance from source to fault location respectively. Equation (2) can also approximately represent the voltage magnitude at the customer on all the neighboring bus. In this paper voltage magnitude is focused than duration.

#### IV. ASSESSMENT OF IMPACT OF VARIOUS FCL

#### A. Superconducting Fault Current Limiters

If SFCL is installed to the power distribution system, the equation (2) is changed to equation (3) during fault. The voltage distortion is reduced than in the case without SFCL.

$$V_{bus} = \frac{Z_{ling} + Z_{SFCL}}{Z_{sourcg} + Z_{Mtr} + Z_{ling} + Z_{SFCL}}$$
(3)

The following segment explains the output waveforms obtained by the placement of various fault current limiters at the optimal location in order to reduce the fault current as well as reduction in the voltage distortion that is caused during the occurrence of fault. The current section discuss the performance of superconducting fault current limiter followed by the performance analysis of other two types of fault current limiter i.e. Solid State fault current limiter and Hybrid fault current limiter. The Fig. 4 and Fig. 5 depict the result obtained using superconducting fault current limiter. Fig. 4 depicts the reduction in fault current in each phase under the influence of SFCL. Fig. 3 (a) depicts

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fault current in phase A, likewise Fig.3 (b) depicts fault current in phases B and Fig. 3 (c) depicts fault current in phase C.



Fig. 3. Fault current magnitude at various phases under the influence of SFCL. (a) Depicts fault current in phase A. (b) Depicts fault current in phase B. (c) Depicts fault current in phase C

#### B. Solid-State Fault Current limiters

The Fig 4 depict the impact of solid state fault current limiter on the fault current and the voltage distortion. Fig. 6 depicts the fault current in each phase under the influence of solid state FCL. Fig. 4 (a) depicts fault current in phase A, likewise Fig. 4 (b) depicts fault current in phases B and Fig.4 (c) depicts fault current in phase C.





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Fig.4. Fault current magnitude at various phases under the influence of Solid State FCL. (a) Depicts fault current in phase A. (b) Depicts fault current in phase B. (c) Depicts fault current in phase C

C. Hybrid Fault current limiter

The Fig.5 and depicts the impact of hybrid fault current limiter on the fault current and the voltage distortion. FCL. Fig. 5 (a) depicts fault current in phase A, likewise Fig.5 (b) depicts fault current in phases B and Fig. 5 (c) depicts fault current in phase C



Fig.5. Fault current magnitude at various phases under the influence of Hybrid FCL. (a) Depicts fault current in phase A. (b) Depicts fault current in phase B. (c) Depicts fault current in phase C



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### V. CONCLUSION

In this paper, a comprehensive up-to- date review of various types of fault current limiters are analyzed and the behavior of each fault current limiters on the voltage distortion and the fault current limiting are also analyzed. From the above discussion we conclude that SFCL is more efficient on the basis of both fault current limitation as well as reducing the distortion in the voltage profile when comparing its performance with other two fault current limiters.

	TYPE OF	$I_{FAULT}$			HYBRID
	FAULT	(KA)	SFCL	SS FCL	FCL
	A-G	I <sub>FA</sub> =7.0	$I_{FA} = 1.5$	I <sub>FA</sub> =1.5	I <sub>FA</sub> =2.0
GROUND	B-G	I <sub>FB</sub> = 1.5	I <sub>FB</sub> =0.5	I <sub>FB</sub> =1.5	I <sub>FB</sub> =2.0
FAULT	C-G	$I_{FC} = 1.5$	I <sub>FC</sub> =0.5	I <sub>FC</sub> =1.7	I <sub>FC</sub> =2.0
		$I_{FA} = 2.0$	I <sub>FA</sub> =1.5	I <sub>FA</sub> =1.5	I <sub>FA</sub> =5.5
	AB-G	$I_{FB}{=}0.50$	I <sub>FB</sub> =0.5	I <sub>FB</sub> =1.5	I <sub>FB</sub> =4.5
		$I_{FB} = 2.0$	I <sub>FB</sub> =0.5	I <sub>FB</sub> =1.5	I <sub>FB</sub> =4.5
PHASE	BC-G	I <sub>FC</sub> = 1.0	I <sub>FC</sub> =0.5	I <sub>FC</sub> =1.2	I <sub>FC</sub> =4.0
FAULT	CA-G	I <sub>FC</sub> = 2.0	I <sub>FC</sub> =0.5	I <sub>FC</sub> =1.7	I <sub>FC</sub> =4.0
		I <sub>FA</sub> =0.5	I <sub>FA</sub> =0.5	I <sub>FA</sub> =1.5	I <sub>FA</sub> =6.0
	ABC-G	I <sub>FA</sub> =6.0	I <sub>FA</sub> =1.5	I <sub>FA</sub> =1.5	I <sub>FA</sub> =6.0
		I <sub>FB</sub> =2.0	I <sub>FB</sub> =0.5	I <sub>FB</sub> =2.0	I <sub>FB</sub> =2.0
		$I_{FC} = 1.0$	I <sub>FC</sub> =0.5	I <sub>FC</sub> =1.7	I <sub>FC</sub> =1.0

### Table 1: RESULT OF VARIOUS FAULT CURRENT LITERS



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#### Table 2: OVERALL PERFORMANCE ANALYSIS

TYPE OF	I <sub>FAULT</sub>	V <sub>LOAD</sub>		
FCL	LIMITATION	RESTORING		
SFCL	Excellent	Excellent		
SS FCL	Poor	Poor		
HYBRID FCL	Poor	Poor		

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