



Performance Evaluation of Canonical Switching Cell Converter Fed BLDC Motor Drive for Power Quality Improvement

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ABSTRACT: This paper presents a performance of the canonical switching cell (CSC) converter fed brushless DC (BLDC) motor drive for power quality (PQ) improvement. The use of CSC not only controlled the DC link voltage but also make the inverter to operate at low frequency so that switching losses are minimized. Moreover the use of front end CSC improves the power factor at AC mains. The system needs only a single voltage sensor for the DC bus voltage sensing; hence the system cost is reduced. The performance was analyzed on the basis of PQ terms of the proposed system under steady state and dynamic conditions. The performance graph has been plotted for the total harmonic distortion (THD) and the power factor (PF). The results show that the system gives a good PF and the supply current THD as per PQ standard IEC 61000-3-2 for wide range of the motor speed and the supply voltage. The performance has been evaluated using MatLab-Simulink.

KEYWORDS: Canonical Switching Cell, Power Factor, THD, Brushless DC Motor, IEC 61000-3-2.

I. INTRODUCTION

In recent years the BLDC motor is widely used in many low and medium power applications, because of its high energy density, high torque /inertia ratio, high efficiency and low maintenance due to the absence of the commutator and brush assembly. The BLDC motors are used in household appliances like washing machine, water pumping and air conditioning etc. and also in industries like robotics and industrial tools and motion control equipment. In the BLDC motor the commutation is done by using the electronic commutation; it involves hall-effect sensors to sense the rotor position and energizes the corresponding phase windings in the proper sequence by using the voltage source inverter (VSI) [1]. In the conventional scheme the BLDC motor drive system is fed by a diode bridge rectifier (DBR) which draws a current from ac mains with higher harmonic levels, also the power factor has been affected and it is not satisfies the PQ standard IEC 61000-3-2, so the power factor correction (PFC) is required for attaining good PQ parameter. The boost converter is widely used in the BLDC motor drives, in which the DC link voltage is maintained constant and the speed is controlled by controlling the PWM pulses of the VSI. This system has a drawback for the higher amount of the switching losses in the VSI switches due to higher level of the switching frequency at the inverter switches and the higher current levels [2-5]. In the sepic and cuk converter fed BLDC motor drive the speed of the motor is controlled by controlling the DC link voltage, hence the switching losses associated with the VSI switches are reduced, but it has a problem of using two sensors, which increases the system cost [6-7]. The CSC converter based system presents a single voltage sensor based BLDC motor drive system, which is a cost effective solution of the low power applications.

II. CANONICAL SWITCHING CELL CONVERTER FED BLDC MOTOR DRIVE

Fig. 1 shows the CSC converter fed BLDC motor drive consists of the front end CSC converter. It is operated at low switching frequency, so that the near unity power factor is achieved at ac mains. The speed of the BLDC motor is controlled by controlling the DC link voltage of the CSC converter. Moreover low frequency operation of VSI reduces the switching losses. The system shown in Fig. 1 gives a near unity power factor at ac mains for a wide range of the speed and the supply voltage.

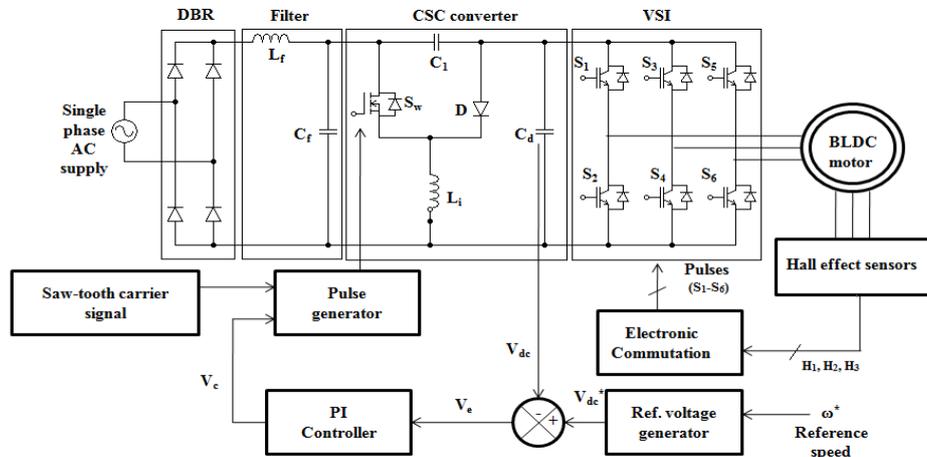


Fig. 1 Block diagram of the Canonical Switching Cell converter fed BLDC motor drive

The CSC [8] converter is operated in discontinuous inductor current mode (DICM) Fig. 2 shows the discontinuous inductor current. The converter is operated in three different modes [8] in every switching period, these as follows:

Mode I: In this mode the CSC converter switch is ON, the inductor charges the input current and the capacitor C_1 discharges the energy to the DC link capacitor, the DC link capacitor is charging as well as supplies a energy to the BLDC motor drive, so the DC link capacitor is fixed to the higher value for supplying a continuous energy to the motor drive.

Mode II: In this mode the CSC converter switch is going into OFF state, then the inductor L_i discharges the stored energy to the DC link capacitor through diode D. In that time the capacitor C_1 charges the DC voltage comes from the diode bridge rectifier (DBR).

Mode III: This mode starts when the inductor current is going to be zero, automatically a diode D goes into the reverse biased condition, the capacitor C_1 continues to charging, then the DC link capacitor discharges the energy to the VSI fed BLDC motor drive.

III. DESIGN OF CANONICAL SWITCHING CELL CONVERTER AND CONTROLLER

The designing of the CSC converter depends on the rating of the motor to be interfaced with it, the 950 W of the CSC converter is designed for the 850 W BLDC motor considering the losses in the system. The design equations are given through (1) – (6). The voltage at the output of the DBR is as follows,

$$V_i = \frac{2\sqrt{2}V_s}{\Pi} \quad (1)$$

where V_s is the input supply voltage. A duty ratio of the converter is as follows,

$$d_n = \frac{V_{dcn}}{V_{dcn} + V_i} \quad (2)$$

where V_{dcn} is the DC link voltage. The critical value of the inductance is

$$L_i = \frac{V_{in} d_n}{2i_{in} f_s} \quad (3)$$

The inductor value of the CSC converter is taken as follows for support a DCIM mode is



International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 2, February 2015

$$L < \frac{L_i}{10} \tag{4}$$

The value of the capacitor C_1 is chosen as follows,

$$C_1 = \frac{V_{dc} d_n}{f_s R_{load} \Delta V_{c1}} \tag{5}$$

The design of the DC link capacitor as follows,

$$C_d = \frac{I_d}{2\omega_L \Delta V_{dc}} \tag{6}$$

Where f_s is the switching frequency, R_{load} is the resistance of the motor and ΔV_{dc} is the ripple in the DC link voltage. The determined values of the CSC converter parameters for 850 W motor are $L=40 \mu H$, $C_1=379 \mu F$ and $C_d=2100.58 \mu F$. These values are designed for the supply voltage (V_s) of 230 V, range of the DC link voltage of 30-90 V and the switching frequency (f_s) is 4 KHZ.

The CSC converter is controlled by using the PWM signals to the converter switch, which maintains the desired voltage level across the DC link capacitor. The DC link voltage is measured using single voltage sensor (V_{dc}) and the reference DC link voltage is generated as follows,

$$V_{dc}^* = k_b \omega^* \tag{7}$$

where k_b is the motor voltage constant and ω^* is the reference speed of the motor.

The reference DC link voltage is compared with the measured DC link voltage and gives a error signal $V_e(t)$ to the proportional integral (PI) controller as,

$$V_e(t) = V_{dc}^*(t) - V_{dc}(t) \tag{8}$$

The PI controller generates a controlled signal $V_c(t)$ as,

$$V_c(t) = K_p V_e(t) + \int K_i V_{dc}(t) \tag{9}$$

Where K_p and K_i are the gain values of PI controller, The initial values of the controller are obtained using Ziegler-Nichols tuning method and then fine-tuned. The obtained values are $K_p = 0.9$ and $K_i = 27.9792$ respectively. This controlled signal is given to the PWM modulator to produce proper gating signals to the converter. The proper operation of the BLDC motor is attained only when the electronic commutation works properly. The electronic commutation is to switch the DC voltage to proper phase winding of the motor, based on the rotor position signal. The rotor position signals are obtained using Hall Effect sensors, based on this position signals the corresponding phase windings to be energized which is shown in Table 1. The equivalent circuit of the BLDC motor comprises of resistance (R_n), inductance (L_n), back emf (E_n) in each phase and its design is discussed in [9-10].

Table 1. 120° commutation table of the BLDC motor

Hall Signals			Motor Phases		
H _a	H _b	H _c	Phase A	Phase B	Phase C
1	0	1	+V _{dc}	Gnd	NC
0	0	1	+V _{dc}	NC	Gnd
0	1	1	NC	+V _{dc}	Gnd
0	1	0	Gnd	+V _{dc}	NC
1	1	0	Gnd	NC	+V _{dc}
1	0	0	NC	Gnd	+V _{dc}

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 2, February 2015

IV.SIMULATION RESULTS AND DISCUSSION

The performance of the system shown in Fig. 1 with designed parameters discussed in Section III is analyzed under steady state and dynamic condition. The performance parameters taken into considerations are the supply voltage (V_s), supply current (i_s), DC link voltage (V_{dc}), motor speed (ω), electromagnetic torque (T_e), motor phase current (i_a), voltage and current stress of the switch (V_{sw} , i_{sw}) and PQ terms like supply current THD, displacement power factor (DPF), power factor (PF). Fig.2 shows the MatLab-Simulink model of the system and the motor parameters are listed in Table 2.

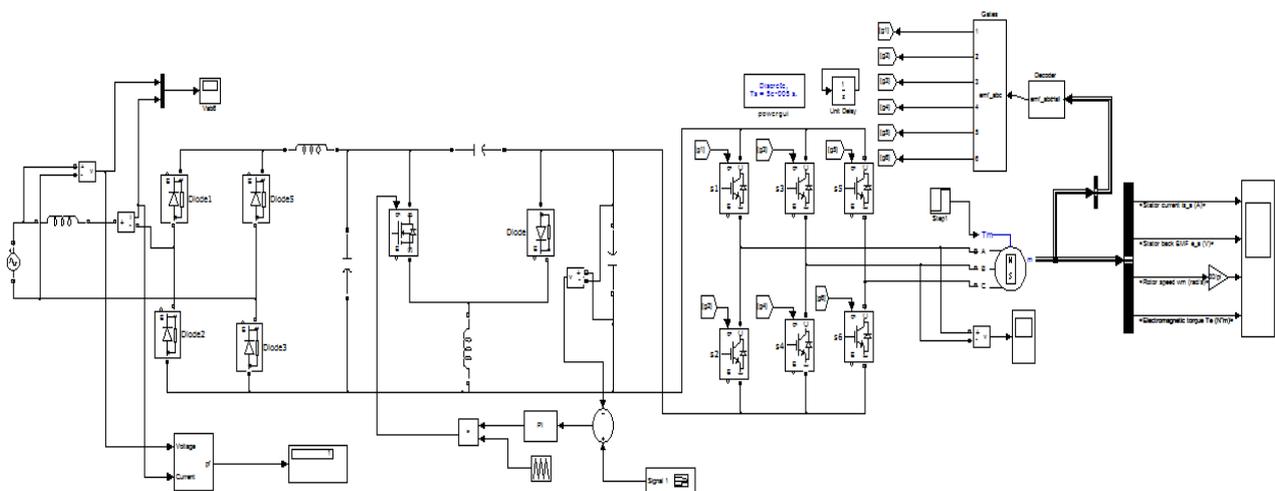


Fig. 2 MatLab-Simulink model of the CSC converter fed BLDC motor drive

Table 2. BLDC motor parameters

Motor Parameters	Values
Input Voltage, V_{dc}	130 V
Stator phase resistance (r_s)	2.68 Ω
Stator phase inductance (L_s)	5.31 mH
Voltage constant	33.5103 Vpeak/kRPM
Torque constant	0.32 Nm/A
Pole pairs	4
Load Torque	2.2 N-m

4.1 STEADY STATE RESPONSES OF THE CANONICAL SWITCHING CELL CONVERTER FED BLDC MOTOR DRIVE

Fig. 3 shows the steady state responses of the drive. BLDC motor is loaded at the rated load torque of 1 N-m, supply voltage of 220 V. A sinusoidal current is drawn at AC mains with the DC link voltage of 60 V and it is in-phase with the supply voltage gives the near unity power factor. The voltage and current stress of the proposed converter switch is obtained as 400 V and 7 A.

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 2, February 2015

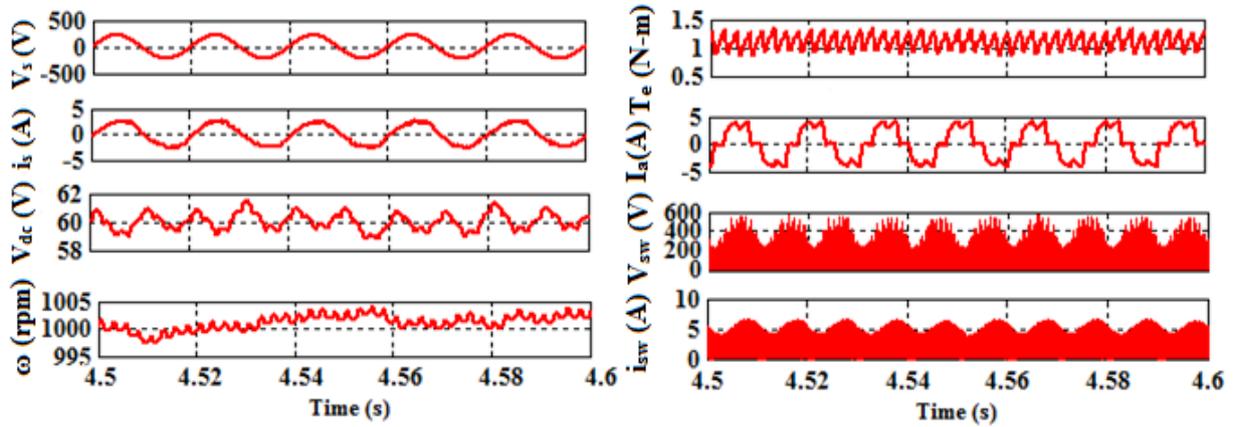


Fig. 3 Steady state responses of the CSC converter fed BLDC motor drive

The THD of the supply currents under steady state with different DC link bus voltage of 30 V and 60 V is obtained as 14.78% and 6.67%, this are the acceptable range by referring the PQ standard IEC 61000-3-2 [11], the corresponding harmonic spectra with the supply current are shown in Fig. 4 and Fig. 5 respectively. It is observed that the THD of the supply current is improved at higher DC link voltage levels.

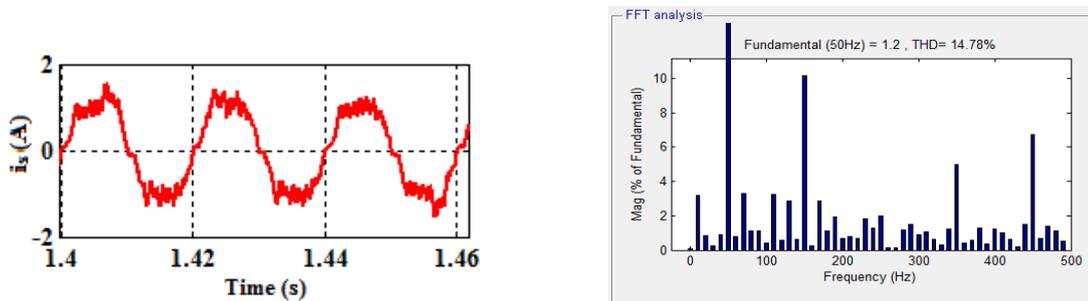


Fig. 4 Supply current and its THD window of the proposed system at the DC link voltage of 30 V

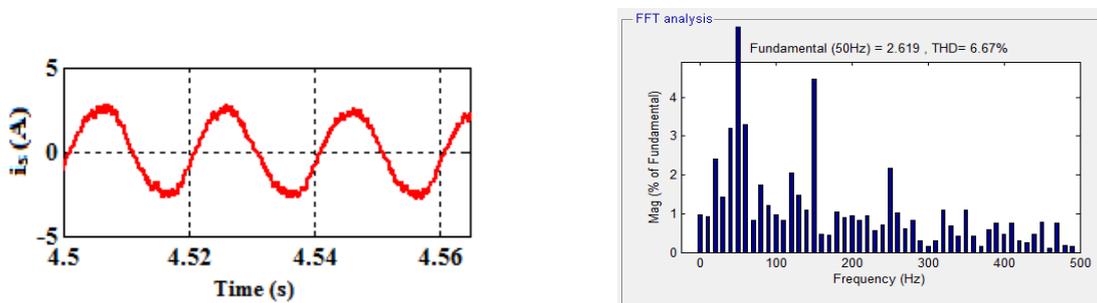


Fig. 5 Supply current and its THD window of the system at the DC link voltage of 60 V

4.2.DYNAMIC RESPONSES OF THE CANONICAL SWITCHING CELL CONVERTER FED BLDC MOTOR DRIVE

To analyse the dynamic response of the system, dynamics are introduced in terms of step change in DC link voltage, change in the motor loading, and change in the supply voltage.

4.2.1 PERFORMANCES UNDER CHANGE IN DC LINK VOLTAGE

Fig. 6 shows the responses of the proposed BLDC motor drive for the change in DC link voltage with the motor loaded at the rated condition and the supply voltage of 220 V. The DC link voltage is changed from 30 V to 60 V at the time of 1 s and in the motor speed the smooth transition has been takes place from the speed of 330 rpm to 1000 rpm with minimum overshoot in the motor speed.

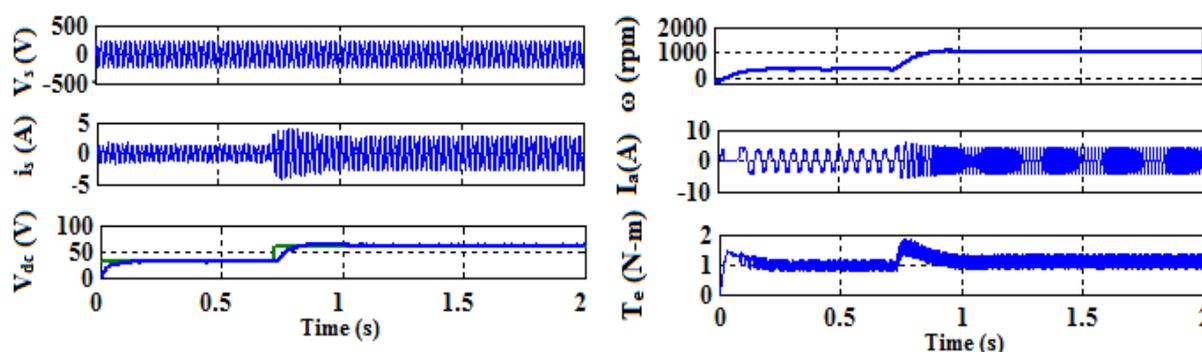


Fig. 6 Dynamic responses of the drive under the change in DC link voltage

The starting inrush current and the transition current also been reduced for both supply and motor phase current within the permissible level, these values has been tabulated in Table 3. This table comprises of the THD, DPF and PF for different values of DC link voltages, these values are the acceptable ranges by referring the PQ standard IEC 61000-3-2.

Table 3. Performance parameters of the system under the change in the DC link voltage

V_{dc} (V)	Motor Speed (rpm)	THD (%)	DPF	PF	i_s (A)
30	320	14.72	0.9999	0.9999	1.3
35	435	15.87	0.9999	1	1.5
50	780	6.93	0.9999	0.9998	2
70	1215	5.02	0.9999	0.9996	3.2
100	1810	4.33	0.9999	0.9997	5

Fig. 7 shows the harmonic spectra with the corresponding supply current under the condition for change in DC link voltage. Fig. 8 shows the plot for THD and PF under different values of the DC link voltage V_{dc} .

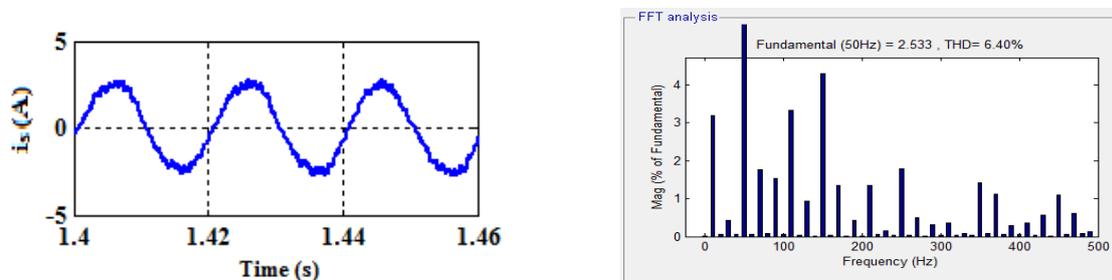


Fig. 7 Supply current and its THD window of the system under dynamic condition for the change in DC link voltage

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 2, February 2015

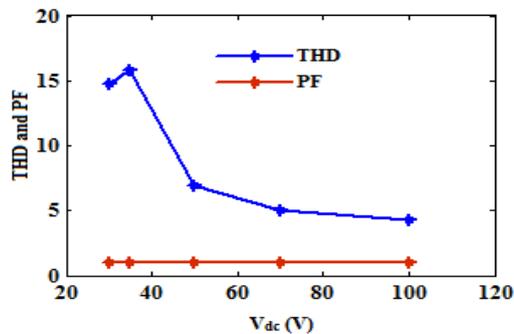


Fig. 8 Performance plot under the change in the DC link voltage

The THD under this condition is 6.40 % is obtained and it is acceptable range by referring the PQ standard IEC 61000-3-2.

4.2.2 PERFORMANCE UNDER CHANGE IN SUPPLY VOLTAGE

Fig. 9 shows the performances of the motor drive under the condition for variations in the magnitude of the supply voltage from 190 V to 240 V the current drawn from the supply is reduced lower voltage level to the higher voltage level. A small disturbance occurs in the motor speed, DC link voltage, motor phase current and motor torque at the time of the supply voltage changes, but it recovers at very short time using PI controller. In this condition the power factor is obtained about 5.91 % which is an acceptable limit by referring to the PQ standard IEC 61000-3-2.

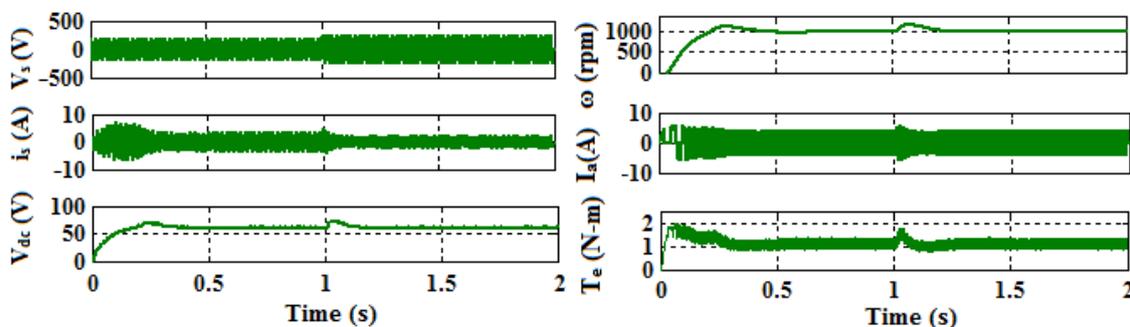


Fig. 9 Dynamic responses of the drive under the change in supply voltage

Fig. 10 shows the supply current and its harmonic spectra for change in the supply voltage, it gives the acceptable THD value for supply current about 5.91 % as per the PQ standard of IEC 61000-3-2. Table 3 shows the Performance of the proposed drive in terms of the supply current THD , power factor, displacement power factor and motor speed for varying the supply voltage from 150 V to 240 V and corresponding plot is shown in Fig. 11.

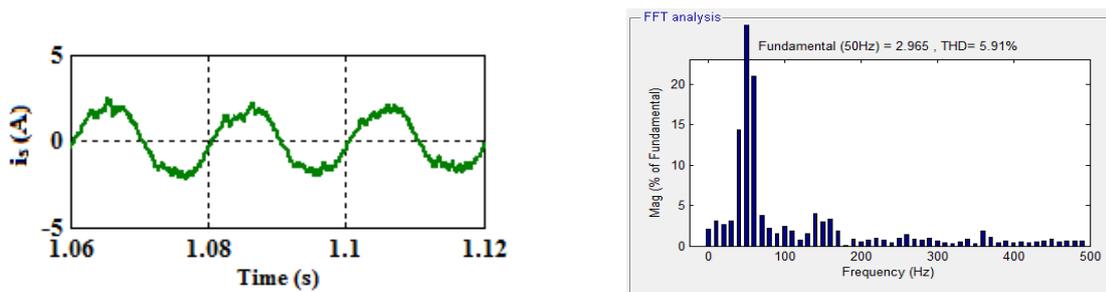


Fig. 10 Supply current and its THD window of the system under dynamic condition for the change in supply voltage

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 2, February 2015

Table 3. Performance parameters of the system under the change in the supply voltage

V_s (V)	THD (%)	DPF	PF	I_s (A)
150	4.06	0.9998	0.9999	4
180	4.17	0.9999	0.9998	3.5
200	4.59	0.9999	0.9994	2.8
220	6.98	0.9999	0.9992	2.4
240	8.81	0.9999	0.9988	2.2

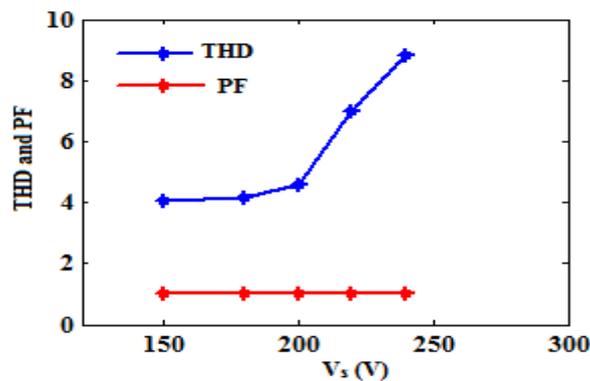


Fig. 11 Performance plot under the change in the supply voltage

4.2.3 PERFORMANCE UNDER THE CHANGE IN MOTOR LOADING CONDITION

Fig. 12 shows the performances of the motor drive under the condition for variations in the motor loading condition. Initially the motor starts at the load torque of 0.5 N-m and at the time of 1 s the load torque is changed to 1 N-m, the corresponding speed is changed from 1200 rpm to 1000 rpm. The supply and motor currents has been changed smoothly under these conditions.

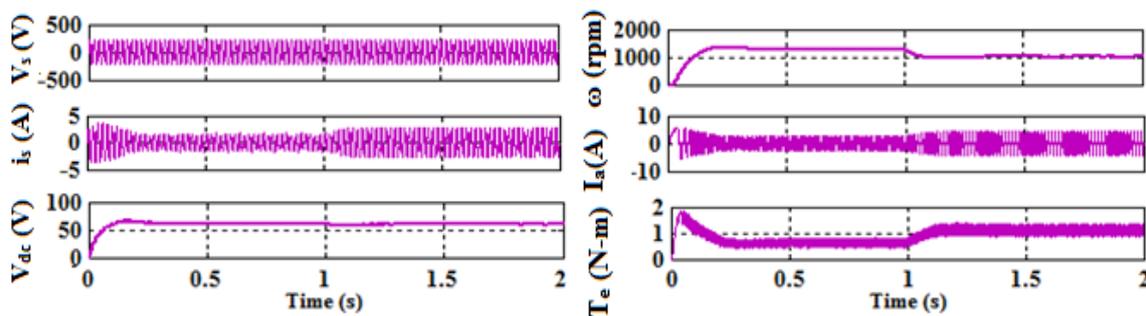


Fig. 12 Dynamic responses of the proposed drive under the change in motor load

Fig. 13 shows the harmonic spectra and the supply current for the change in motor load condition. The supply current THD has been obtained about 6.07 %. Apart from the above analyses, the voltage and current stresses of the CSC converter switch is tested under different loading conditions and shown in Table 4.

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 2, February 2015

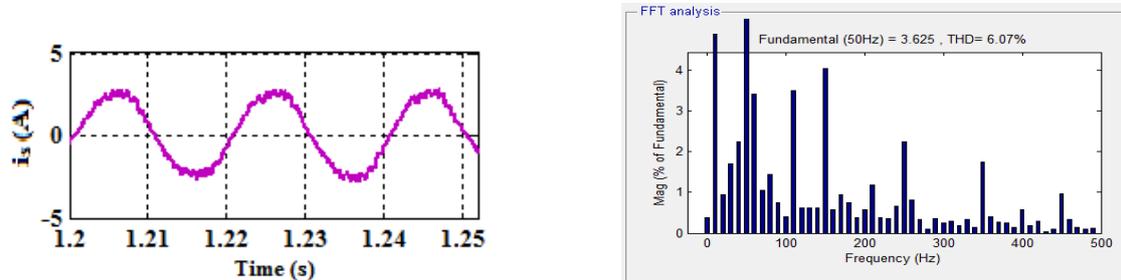


Fig. 13 Supply current and its THD window of the system under dynamic condition for the change in motor load

Table 4. Voltage and current stresses of the CSC converter switch at different motor loading

Load (%)	V _{sw} (V)	i _{sw} (A)	i _s (A)
20	400	3	0.8
40	400	4	1.5
60	400	5.3	2
80	400	6.2	2.4
100	400	7.8	3.2

Table shows that the voltage stress of the switching device is about 400 V at any loading condition. The maximum current stress of the switching device is 7.8 A at 100 % loading.

V.CONCLUSION

In this paper the steady state and dynamic conditions were checked for CSC converter fed BLDC motor drive for the improvement in terms of power quality. This converter claims the major advantages of using one sensor, low THD high PF at AC mains, low switching losses due to low frequency operation. The supply current THD was obtained below 7% under the wide range of the motor speed and the supply voltage where those values are recommended by the PQ standard IEC 61000-3-2, hence it is well suited for low power applications. This work can be further improved by using advanced controllers.

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