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Realization of Low Power Sensor Node Processor for Error Detection and Correction in Wireless Sensor Networks

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ABSTRACT: Nowadays wireless sensors Networks are used in wide applications. In a large wireless sensor network it consists of sensor nodes .The function of sensor node is sensing, processing and communicating the informations.At the time it consumes dominant power of the total power. In this project design a sensor node with long time operating capability and efficient energy management. Wireless Sensor Networks have potential ability to monitor and interact with our environment. Fault tolerant operation is critical to the success of WSNs.. Noise and other disturbances are the two methods that degrade the system performance. Fault-tolerant mechanism in wireless sensor networks is very important for construction and deployment characteristics of low powered sensing devices. . In this paper we focus our work on implemented with low complexity error detection technique which can be low data redundancy and efficient energy consuming in wireless sensor node. In the sensor node within a single chip has been developed and implemented on a performance Model Sim. Xilinx ISE Simulator has been used to Design the Power Analysis in Using VHDL Coding. An Efficient Sleep scheduling with a Synchronized timer and algorithm to Achieve optimum Power Efficiency.

KEYWORDS: Fault-Tolerant,Modelsim,Sensor Nodes, sleep scheduling,VHDL,WSN,XILINX.

I .INTRODUCTION

In a large wireless sensor networks hundreds/thousands of sensor nodes are deployed in a regular or random manner. These sensor nodes are capable of sensing, processing and communication. They must be cheap they must be low power and long lasting's is a new direction to researchers to provide more energy efficient, reliable and low cost. Prolonging network lifetime for this sensor networks is a critical issue. Sleep scheduling for sensor network is another key factor which controls the energy management. In a sensor network wakeup timer is used which activates the sensor node when it receives a signal and it start processing. It enters in to sleep mode again after processing until it receives a next wake up signal

II.RELATED WORK

In some recent research ,we find the research works for developing low power sensor nodes for large wireless sensor network.in the work of Gu and Stankovic,a radio triggered hardware had been used to wake-up a sleeping node. The hardware harvest energy from the signal received from transmitter and a significant level of power can be saved. But in this system, the range must be very low and applicable for limited nodes.

Liang et. al.developed a low power sensor node in their research work using wake-up radio ATA5283 fabricated by ATMEL. The working frequency is about 125 KHz only in the year of 2007.In recent year's technology has been developed and more advanced sensor nodes are implemented.

Van Der Doom et.al,has developed a sensor node consists of wake-up timer circuit in order to having a power saving approach. They have presented their work with 868MHz frequency of timer circuit and used a microcontroller PIC 12F683 to detect the wake-up signal. Another microcontroller ATMEGA 128 has been used as a node processor which becomes activated in its low power mode receiving the wake-up signal.

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Renyan Zhou et.al.Presented VLSI design of single chip processor architecture of sensor node using 8051 microcontroller. The system clock frequency is about 16MHz and power dissipation is the order of 60mW.
Aki Happonen et.al. explained the low power optimization for a single chip sensor node using a reference design OKI's ML7051 for ARM 7TDMI processor

III.DESIGN METRICES

For a power efficient wireless sensor networks, the design of sensor nodes faces many challenges like it requires large memory and more bandwidth. The sensor node must have high computational capability and low power consumption.
To design a low power sensor node some important design metrices are following

•The design protocols should be keep as small as possible to maintain power consumption.
•Minimum hardware should be involved in this design in order to minimize the power consumption, size and cost. Hence design should be optimized.
•Reduction of circuit complexity is another challenging requirement.
•Sensor node must be cheap.
To meet all these challenges and requirements, an approach has been attempted here.
Beacon performs the centralized control. When data packet is transmitted from beacon the function of beacon is it first searches the sensor node within its range and check if the node responds or not.Because usually sensor node may be lost or damaged or demolished by any reason. So response is checked before transmission. If beacon receives ACK from neighbor node it starts transmission of data packet in specific format.
This network has a rearrange able property that can realize all possible permutations between its input and outputs. The choice of the three stage in the network with a modest number of middle-stage switches is to minimize cost implementation, whereas it still enables a rearrange able property for the network.

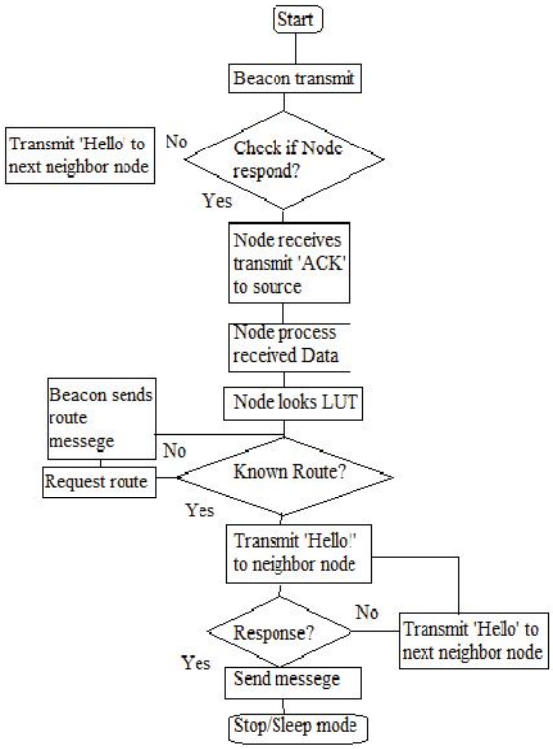

Fig 1.Flow chart for the basic node functions

Figure 1.describes the operational functional flow chart for a typical sensor node within a wireless sensor networks For any reason the path is changed it request the beacon to send the routing information for itself to avoid delay.Following example gives idea about node deployment and routing path for data packet from source to destination within a sensor

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network. In this example beacon B1 has two sensor nodes (B1 & B2). The circular boundary is within its transmission range. If the node B2 is not respond or dead only it receives from B1.If the routing information is lost the modified routing should be send by Beacon. Before transmitting the data packet every sensor node request the acknowledgement from neighbor node to check whether the node is active mode or not.

IV.DESIGN AND IMPLEMENTATION

In the sensor node within a single chip has been developed and implemented on a performance Model Sim. Xilinx ISE Simulator has been used to Design the Power Analysis in Using VHDL Coding. An Efficient Sleep scheduling with a Synchronized timer and algorithm to Achieve optimum Power Efficiency. For Real time applications it can be implemented in high performance FPGA kit

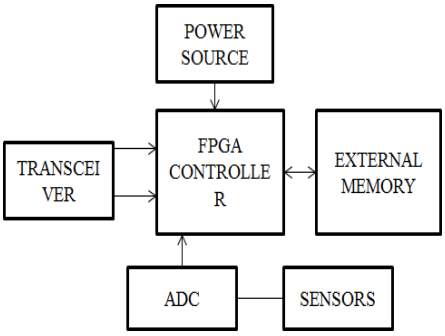

Fig.2 Architectural diagram of a typical sensor node.

Fig .2 shows the architectural diagram of a typical sensor node for real time applications it will be implemented in FPGA kit.

V.PROPOSED WORK

1.1 ERROR DETECTION & CORRECTION IN WIRELESS SENSOR NETWORKS:

The Realization of Low Power Sensor Node system is also useful in error detection and correction. This is apparent, given the independence of digits in a residue number representation: an error in one digit does not corrupt any other digits. In general, the use of redundant moduli, i.e. extra moduli that play no role in determining the dynamic range, facilitates both error detection and correction. But even without redundant moduli, fault-tolerance is possible, since computation can still continue after the isolation of faulty digit-positions, provided that a smaller dynamic range is acceptable. Realization has techniques to error detection and correction that this ability can be used in wireless sensor network to decrease renewed data sending via occur error in data packets. It is also of very low complexity, thus good for energy constrained sensors. Fig. shows the structure of circuit error detection.

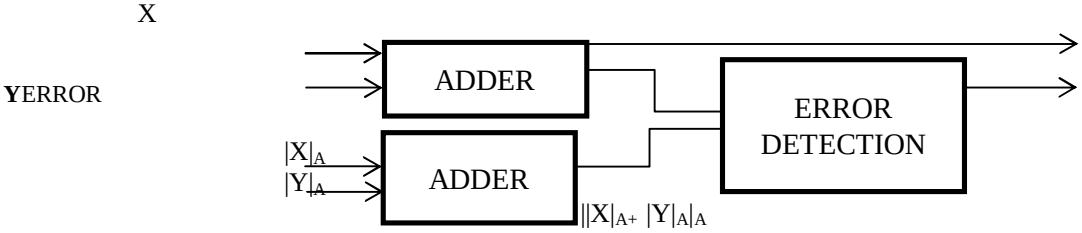

Fig.3 ERROR DETECTION AND CORRECTION

Fig.3 showsthe error correction and detection block diagram for wireless sensor networks for detecting and correcting errors.

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HAMMING CODE

Hamming code is a set of error-correction code s that can be used to detect and correct bit errors that can occur when computer data is moved or stored.

General algorithm

The general algorithm generates a single-error correcting (SEC) code for number of bits.
1.The bits are numbered starting from bit 5,4,3,2,1 in LSB, etc.
2.Write the bit numbers in binary: 101, 100, 11, 100,1, etc.
3.All bit positions that are powers of two (have one 1 bit in the binary form of their position) are parity bits
4.All other bit positions, in the binary form of their position, are in data bits.
5.Each data bit in a unique set of two or many parity bits, verified by the binary form of its bit position.

VI.SIMULATION RESULTS AND DISCUSSIONS

The simulation result determines the design of low power sensor nodes in VHDL code using sleep scheduling algorithm. It consists of three nodes(node2,node4,node5) and show how the data transfers**.**

OUTPUT WAVEFORM FOR NODE 2 DATA TRANSFER

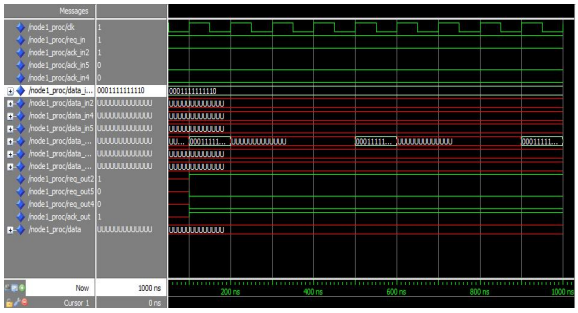

Fig.4This Simulation Result Shows The How The Node2 Transfers Data.

SIMULATION RESULT DESCRIPTION

Node1_Proc/Clk-Clock Signal
Node1_Proc/Reg_In- Request Signal
Node1_Proc/Ack_In2- Node 2 ->Wakeup Mode(Active)
Node1_Proc/Ack_In2- Node 5 -> Sleep Mode (Inactive)
Node1_Proc/Ack_In2- Node 4-> Sleep Mode (Inactive**)**

OUTPUT WAVEFORM FOR NODE 5 TRANSFER

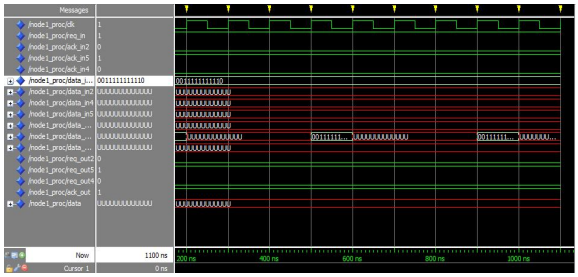

Fig.5 This Simulation Result Shows The How The Node5 Transfers Data

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Node1_Proc/Ack_In2- Node 5 ->Wakeup Mode(Active)
Node1_Proc/Ack_In2- Node 2 -> Sleep Mode (Inactive)
Node1_Proc/Ack_In2- Node 4-> Sleep Mode (Inactive)

OUTPUT WAVEFORM FOR NODE 4 TRANSFER

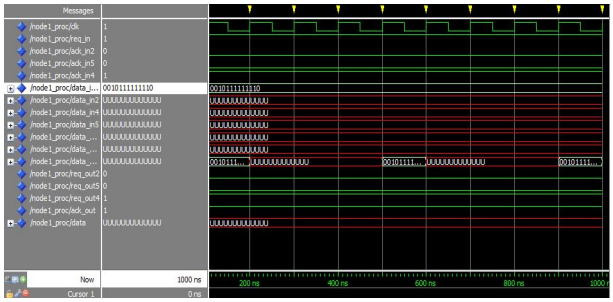

Fig.6 This Simulation Result Shows The How The Node5 Transfers Data

Node1_Proc/Ack_In2- Node 4 ->Wakeup Mode(Active)
Node1_Proc/Ack_In2- Node 2 -> Sleep Mode (Inactive)
Node1_Proc/Ack_In2- Node 4-> Sleep Mode (Inactive).
Fig.4.fig.5,fig.6 simulation results shows how the sensor node transfers data using sleep scheduling algorithm.

VII. CONCLUSION

In this paper, first, we consider some of problems in wireless sensor networks such as: errors in transmitted data and consumed energy of nodes. The Overall Performance, Power Dissipation and hardware Requirement has been Described with a details Comparison of previous Works.In this design a low power sensor node using VHDL coding and sleep scheduling algorithm is adopted for this design. In this processing Speed is Very High as circuit complexity. In power Consumption is of the order of 13 mw . Network Design Efficient Output for the Data bit detect and correct errors in data with the using minimum redundancy. Also, by reducing the processing power lower computing energy is consumed for error detection in network. In this paper, we use of these advantages to error detection and correction in wireless sensor networks

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