

# Reducing Energy in a Ternary Cam Using Charge Sharing Technique

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**ABSTRACT :**The ternary content addressable memory uses a match line sensing scheme. Here a selective precharge is combined with charge sharing technique to reduce the match line energy consumption. This technique improves speed. Unlike many existing scheme this scheme uses number of control signals need to be generated off-chip. A new match line sensing scheme for ternary content addressable memory (TCAM) is presented in this paper. A Match line sense amplifiers are used here in order to sense the match line which is high, when the data is matched. The Match line sense amplifier (MLSA) consists of Charging unit, Sensing unit and Differential amplifier. The differential amplifier compares the voltages and resulting the output depending on the data match and mismatch. The charge in one segment can shared with the next segment and hence reducing the energy consumption.

**Keywords-** MLSA, Charge sharing, ML segment, energy consumption, selective precharge, content addressable memory, ternary.

## I.INTRODUCTION

In this paper, Ternary content addressable memory (TCAM) offers the hardware based solution for the application requiring high speed parallel search operation. Hardware based solution is faster than the software based solution. So, TCAM has become an attractive choice for applications such as internet protocol (IP) packet forwarding and classifications performed in network routers and switches. The name 'ternary' means it can store three states such as '0' (01), '1' (10) and don't care state or mask 'X' (00). The ability to store the don't care states allows search within a range and can result in multiple matches. A priority encoder is used to select the match with the least number of don't care states i.e. match with the longest prefix [1]. A TCAM cell consists of two SRAM cells and a comparison logic. A TCAM word is a collection of multiple TCAM cells connected to common match line (ML) as shown in fig.1. The search word is provided through search lines (SLs). During parallel search operation, frequent switching of the highly capacitive MLs and SLs cause large energy consumption. This reduces the speed advantage of TCAM so, energy reduction is a key issue for the TCAM designer.

ML sensing scheme precharges MLs to high and SLs to ground before starting the search operation. If a TCAM word matches the search word then the corresponding ML remains disconnected from the ground and hence retains its voltage. In case of mismatch, the ML has conducting path to ground through NOR type comparison logic. So, it discharges to zero voltage. The match line sense amplifier (MLSA) senses the ML voltage and produces high output for a matched ML or low output for a mismatched ML.

In this paper, A Current race type sensing scheme combined with charge sharing and selective precharge is used. In current race technique, the Match line (MLs) are pre discharged to ground. During search operation they are charged to high. Search line (SLs) need not to be pre discharged to ground. This reduces the switching activity and thus saves the SL energy. For a fully matched words the corresponding MLs get quickly charged to a threshold causing the sense amplifier to output

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high. For mismatched words, MLs have discharging path to ground. Charge sharing techniques use either a separate capacitor or segment of the ML to store charge in the precharge or partial comparison phase. In the next phase this charge is shared with the ML or remaining ML segments. Selective precharge scheme divides ML into two or more segments and performs comparison segment by segment. Selective precharge has been implemented by partitioning the MLs in a way to maximize the mismatch detection in the first segment comparison. IP version 4 (IPV4) uses 32 bit long IP address. If the most significant 8 bits (the first segment) of the destination addresses of the IP packets are used in the initial comparison then 98% of the mismatched words can be identified [3] and for these MLs comparison of the remaining 24 bits is not required. Only in case of full match in the first segment, the second segment is activated. Instead of charging the second segment in this phase, the charge stored during the first phase in the matched first segment is distributed among both the segments. This will cause greater energy saving than the charge shared MLSA proposed in [4]. The resulting ML voltage is used for making match decision. Here Dummy Match line is used to control the charging duration of the first segment and to deactivate the second segment MLSA. Figure 2 is a TCAM with two SRAM cell and a comparison logic.

By referring to [1], provides a fast data search function by accessing data by its content rather than its memory location indicated by an address. CAM also support search operations as compared to RAM. CAM can be used in wide variety of applications such as parametric curve extraction, Huffman coding/decoding, data base access, pattern matching and networking IP address lookup etc. Now a day main application of TCAM is to classify and forward IP packets in network routers. The disadvantage of CAM are high power dissipation and high area cost.

By referring to [3], provides if the data comparison is done with the first segment then most of the case the data is matched, if so then the next segment is activated and compared with remaining data. So if there is a mismatch in the early stage lot of energy is saved for further charging the remaining matchlines.

By referring to [4], Selective precharge performs a match operation on the first few bits of a word before activating the search of the remaining bits. For example, in a 144-bit word, selective precharge initially searches only the first 3 bits and then searches the remaining 141 bits only for words that matched in the first 3 bits. Assuming a uniform random data distribution, the initial 3-bit search should allow only  $\frac{1}{2}$  words to survive to the second stage saving about 88% of the matchline power. In practice, there are two sources of overhead that limit the power saving. First, to maintain speed, the initial match implementation may draw a higher power per bit than the search operation on the remaining bits. Second, an application may have a data distribution that is not uniform, and, in the worst-case scenario, the initial match bits are identical among all words in the CAM, eliminating any power saving.

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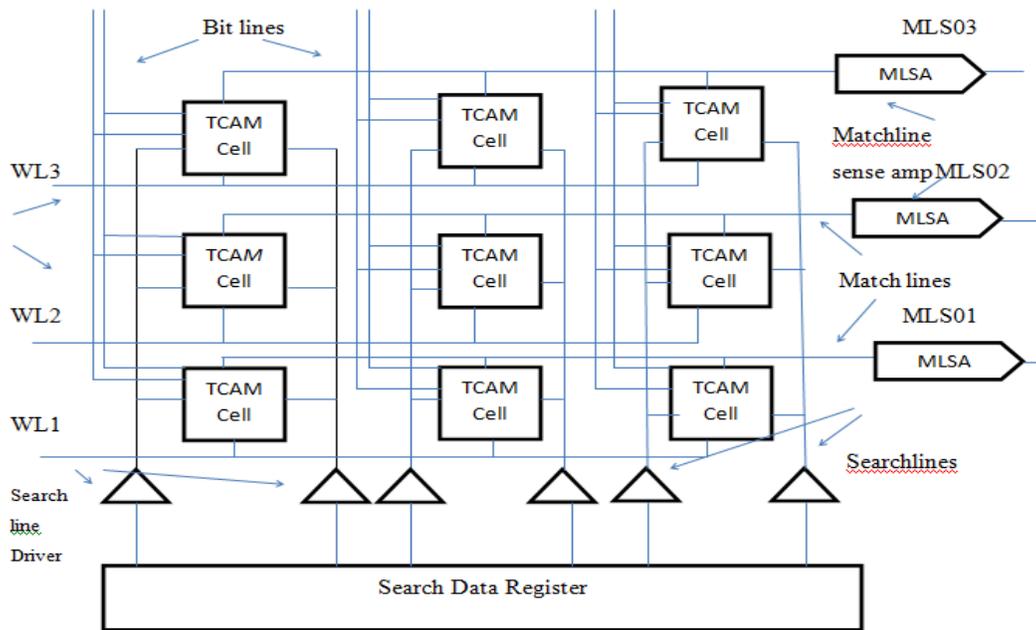


Figure.1 Block diagram of a 3x3 TCAM array. Each row constitutes a TCAM word. Each word consists of multiple TCAM cells

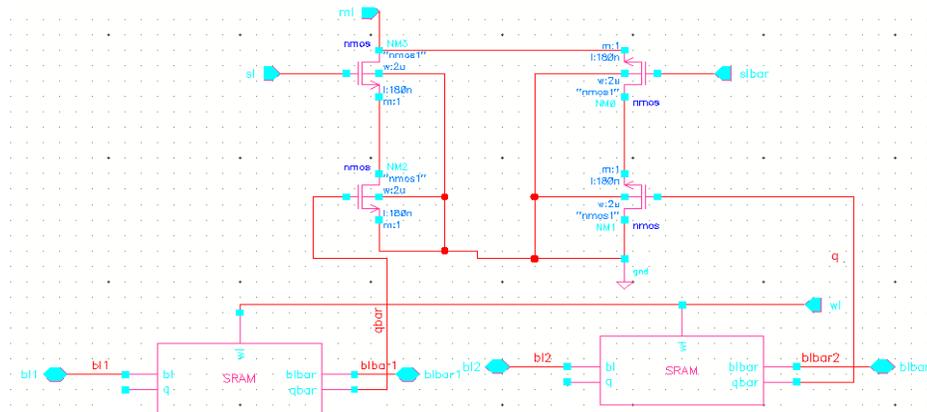


Figure.2 16T TCAM

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## II. PROPOSED SCHEME

Figure.3 shows one TCAM word and the Dummy word in the proposed scheme. In this the first segment Match line sense amplifier (MLSA), it consists of charging unit and a sensing unit. The second segment MLSA consists of a differential amplifier and a second charging unit. The Dummy word is fully matched because it stores mask bits in all the TCAM cells.

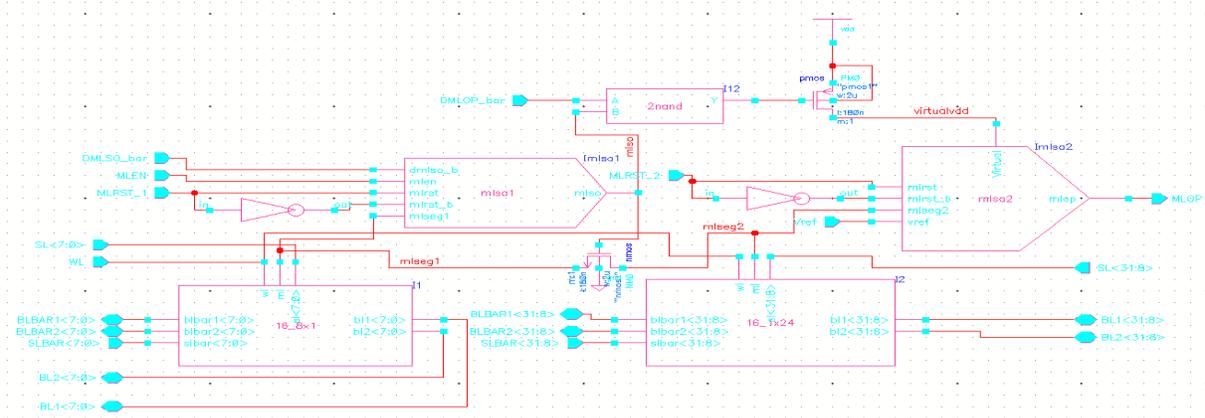


Figure.3 TCAM word with MLSAs

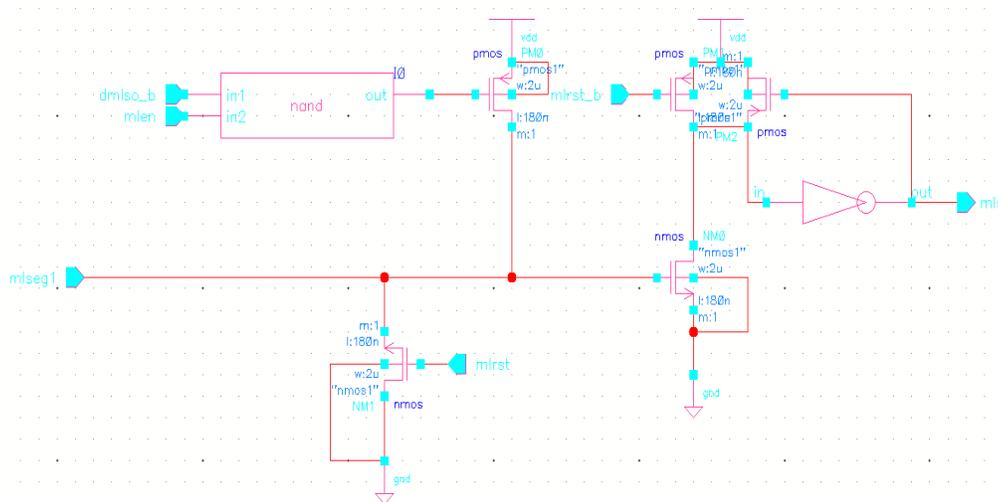


Figure.4 MLSA 1 with charging and sensing unit 1

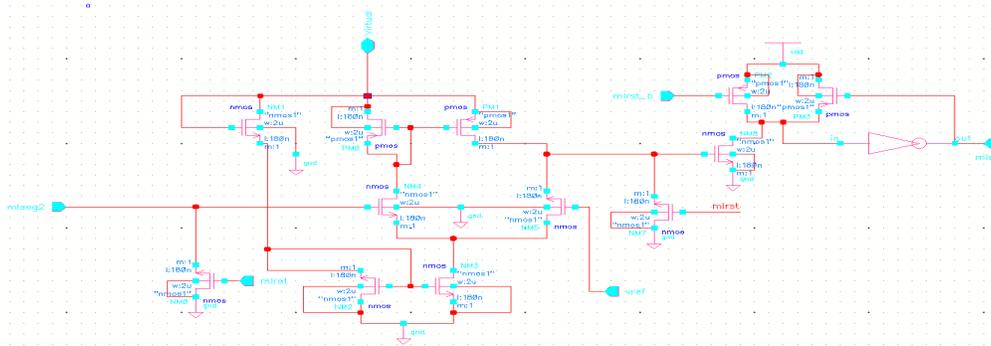


Figure.5 MLSA 2 with differential amplifier and sensing unit 2

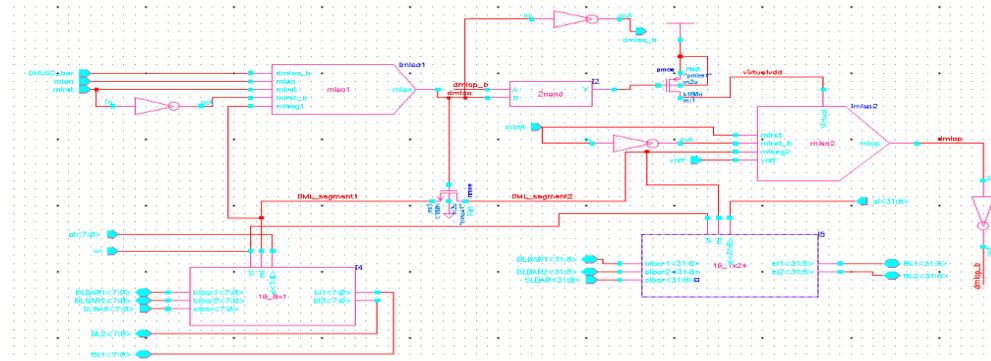


Figure.6 Dummy TCAM word

The Match line reset signal (MLRST) resets all the ML segment voltages, differential amplifier outputs (DAOP) and ML segments outputs i.e. MLSO, MLOP, DMLSO, DMLOP to zero. Then MLEN signal initiates the search operation. In the first the first 8 bits of all TCAM word are compared with the corresponding 8 bits of the search word. Charging current is supplied through the transistor M1. In case of a full match in the first segment the segment 1 charges quickly to the threshold voltage of N1 and the sensing unit 1 produces a high ML segment output (MLSO). DML segment will work in the same way as a matched ML segment 1. As soon as the DML segment output DMLSO goes high transistor M1 is off to stop the further charging of all MLs and the DML. In case of mismatch the MLs have discharging path(s) to ground. So, their first segment voltages remain below the sensing threshold of the sensing units. Hence MLSOs for those MLs remain low. For these MLs, the pass transistor (Npass) remain off and the second segment remain inactive maintaining a low ML output at MLOP.

In case of full match in the first segment the output of MLSA 1 (MLSO) turn on the pass transistor Npass to allow charge stored in the first segment to be shared by the second segment. MLSO also activates the differential amplifier circuit by turning on the transistor Mg. If second segment is fully matched, the charge sharing cause a built up of voltage in that segment. The final voltage is determined by the capacitance ratio of the ML segments and the initial first segment voltage. The differential amplifier compares this final voltage with a zero going voltage Vref and its output DAOP can become sufficiently high to trigger the sensing unit which gives a high output at MLOP. But if there is a single mismatch, charge

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can leak to ground from segment 2. So voltage of the second segment rises momentarily after the pass transistor turns on but eventually goes back to zero. DAOP in this case is small and is not sufficient to trigger the sensing unit and the MLOP remains low.

### III.SIMULATION RESULTS

We have simulated 64 word x 32 bit TCAM arrays in our proposed scheme and the CR scheme using 45nm 1V CMOS logic.

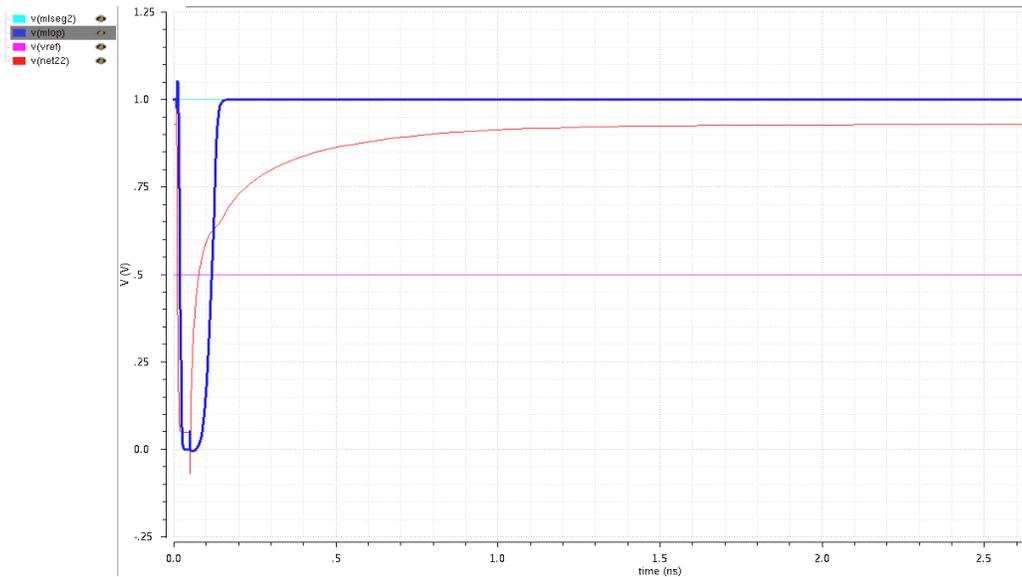


Figure.7 output when data is matched

Fig. 7 shows the variations of voltages in mlseg1 and mlseg2, if the data in the first segment and second segment is matched. As soon as the data applied to the search lines, if these data are matched with the TCAM word then the mlseg1 charges quickly and hence the graph shows that mlseg1 increases, outputs high MLSO. And this charge will activate the second segment by turning on the pass transistor and also activates the differential amplifier. If the data in the second segment is fully matched with the TCAM word then mlseg2 is also high and hence the output MLOP is high. If there is any single bit mismatch then the output is low i.e. both MLSO and MLOP is low. If it is a match then the dummy match line output (DMLOP) will turn off the transistor M1 for further charging of the first segments of all MLs and DMLs. For mismatch there is a discharging path to ground. So their first segment voltages remain below the sensing threshold of the sensing unit. Hence MLSOs for those MLs remain low. If this is the case the second segment remains inactive and hence the output MLOP is low. The output for the mismatch match condition is shown in figure 8 and 9. In which if there is a mismatch in first segment then MLSO is zero and the MLOP is also zero. The below table shows the voltage variations and the temperature variations.

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Voltage Variation for Match case

Voltage(V)	Current(A)	Power(W)
0.9V	$1.0901 \times 10^{-4}$ A	$98.109 \times 10^{-6}$ W
1V	$2.9684 \times 10^{-4}$ A	$296.84 \times 10^{-6}$ W
1.1V	$7.9533 \times 10^{-4}$ A	$874.83 \times 10^{-6}$ W

Temperature Variation

Voltage(V)	Temperature	Current (A)	Power(W)
1V	-25	$2.2614 \times 10^{-4}$ A	$2.2614 \times 10^{-4}$ W
1V	0	$2.9684 \times 10^{-4}$ A	$2.9684 \times 10^{-4}$ W
1V	25	$3.7719 \times 10^{-4}$ A	$3.7719 \times 10^{-4}$ W
1V	125	$7.8685 \times 10^{-4}$ A	$7.8685 \times 10^{-4}$ W

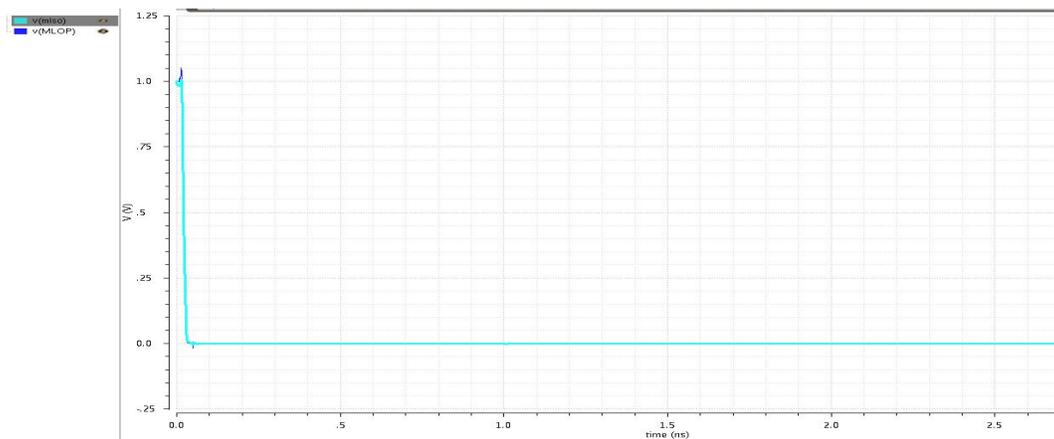


Figure 8. Output of MLSO if mismatch in first segment

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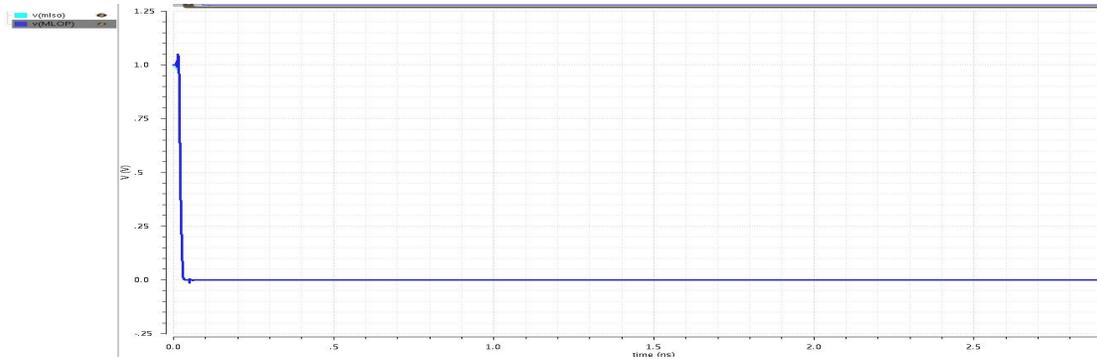


Figure.9 output of MLOP if mismatch in first segment

## IV CONCLUSION

In this paper, presented a low energy match line sensing scheme using CR type MLSA combined with selective precharge and charge sharing. The same ML segment used in the first phase of selective precharge was used for storing charge, which was shared by the second segment during next phase. Here I have used 45nm technology for simulation so that we could safely ignore the leakage power in the SRAM cells and consider the total energy consumption during the search as the dynamic energy consumption. For larger word size (TPv6 addresses) the segment sizes have to be chosen carefully to maintain a trade-off between speed and energy. Too small first segment will cause low voltage in the second segment and will degrade the speed. It may also cause more number of second segments to get activated and thus reduce the energy reduction advantage. Too large first segment will also degrade the energy saving as more capacitance has to be charged in the initial comparison phase.

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